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Arbitrary Density Pattern (ADP) Based Reduction of Testing Time in Scan-BIST VLSI Circuits

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***Abstract*— Test power reduction done by Arbitrary Density Patterns (ADP) in which the dynamic usage of the WRP and TDP under adaptive switching of clock is used. Weighted random patterns (WRP) and transition density patterns (TDP) can be efficiently used to decrease test length with increased fault coverage in scan-BIST circuits. New test pattern generator is designed to generate weighted random patterns and controlled transition density patterns to enable efficient scan-BIST applications. We attain decrease in test time without sacrificing fault coverage while preserving test power limits by dynamically adjusting the scan clock, which is provided by a built-in hardware monitor of transition density in the scan register.**

***Keywords*— ADP, TDP, WRP, BIST, inactivity monitor**

I. INTRODUCTION

With the growth in size, the number of test vectors required to test them has also improved. The time taken to test a chip is the product of the number of test vectors used and the time required to apply each vector in the CUT. As the number of test vectors rises, the time for applying them also increases. Since classy ATE is used to examine these chips, the cost per chip is increased with increase in test time. There is therefore increasing concern about the time essential to apply these test vectors. Due to progression of technological expertise circuit size has increased which naturally entitles longer test time. On the other hand, the test process results in greater power dissipation in the circuits compared to the power dissipated in the standard mode of the circuit.

ADP consists of WRP and TDP. Weighted random patterns (WRP) have been used before to reduce test length for combinational circuits. Proper range of the input probability can raise the effectiveness of test vectors in spotting faults, causing test time reduction. Complete scan proposal is a common plan for testability (DFT) method in which flip-flops in the circuit are connected together such that input vectors are shifted in and circuit responses are shifted out serially through the scan chains. The flip-flops serve as sockets of controllability and observability, thus accumulating the fault coverage.

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Transition density patterns (TDP) are largely used for sinking the power consumption during test. Transition density for a signal or a circuit was initially defined for assessing the dynamic power as the number of signal transitions per unit time.

II. OBJECTIVE

Analyse the effect of ADP on fault coverage. (Arbitrary density pattern = Weighted random pattern + Arbitrary density pattern). Organize an effective test generation process using the information from the analysis. Adjust the scan frequency to the transition density for power constrained testing. New test pattern generator with the capability of producing ADP has to be done. Adjust the scan frequency according to the transition density for a scan-BIST circuit to boost up the test in multiple scan chains. Deployment of an adaptable transition density test pattern generator in a BIST circuit that is capable of producing pre-designated transition density vectors. Reduction of test application time is attained by adapting the scan clock to the pre-selected transition density.

III. BACKGROUND

A. Scan Design

Sequential circuits are tougher to test than combinational circuits. This is because the existence of memory elements such as flip-flops, as shown in Figure 1, which creates internal states during circuit operation. An exhaustive test would involve application of all probable input vectors at all possible states of the memory elements.

If a circuit has n inputs there will be 2n possible input combinations. As n increases the number of possible input vectors increases exponentially. This type of occurrence is even more severe for sequential circuits. The DFT technique that improves testability of sequential circuits is designed as a scan design or its partial scan dissimilarities. Here the sequential circuit is newly designed so that it can operate in test mode separately. When the circuit is in test mode, the flip-flops in the circuit are chained together to form one or more shift registers. The shift registers so formed is also called as scan path. The scan path is responsible for the circuit switching activity. The flip-flops serve as a point of controllability and observability.

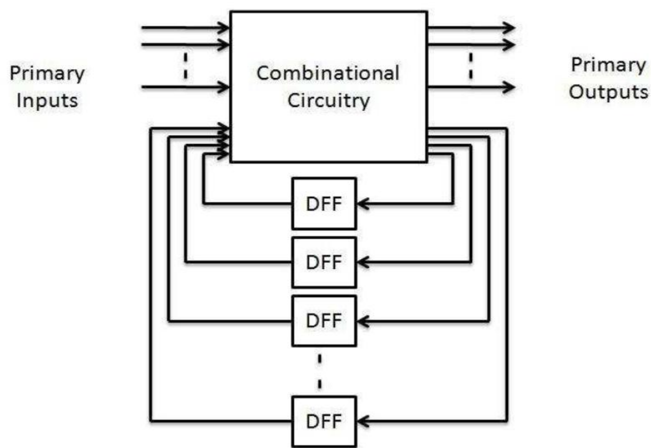

Fig 1: Design of a sequential circuit.

B. Built-In Self-Test (BIST)

BIST is a DFT technique in which supplementary hardware is added to the circuit to be tested so that it can test itself. The basic BIST circuitry is shown in Figure 2. Among them, the use of a Linear Feedback Shift Register (LFSR) that produces pseudorandom pattern sets is most common.

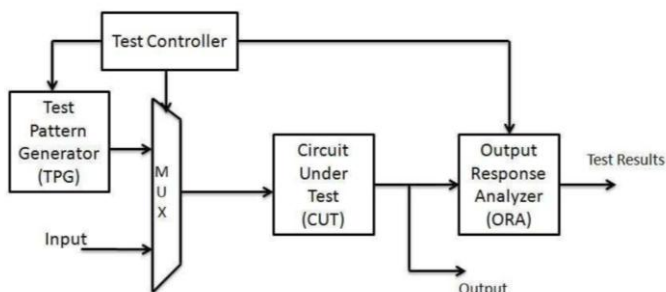

Fig. 2: Simple BIST circuitry.

A numerous outputs are received from the CUT. It is necessary to store the correct values of all those bits without adding a lot of additional hardware. This in turn calls for some more design techniques. A LFSR, most commonly known as Signature Analysis Register (SAR) or Multiple Input Signature Register (MISR) is used for this purpose.

1) *Test-Per-Clock BIST Systems:* In this type of system, a test is applied to the CUT every clock cycle. This type of system has little pattern lengths. A major concern for BIST is the simulation time required to compute good circuit behaviour will be small. It is therefore beneficial to have short pattern lengths".

2) *Test-Per-Scan BIST Systems:* In test-per-scan BIST, each test contains scan-in of one input vector, one clock to conduct the test in the CUT and scan-out of output responses.

As the size of the circuit increases, test complexity also rises. Their internal nodes become harder to test. Circuits are therefore modified so that they can be tested well.

IV. LITERATURE SURVEY

Numerous techniques have been used to lessen the power and testing time during testing of VLSI circuits. Reducing these parameters will contribute to the low cost of the circuits. More number of techniques has been used in the past to reduce the test power and the test application time [9]. The assessment in the field of reducing the test power was performed.

First, an experimental method for generating large-scale integration (LSI) test patterns with weighted random pattern is studied. In specific, this method presents a technique for generating random pattern sequences to test complex logic circuits [20]. Here path sensitizing method is used between inputs and outputs. Fault-oriented and path-oriented path sensitizations were performed. In its primary stage, purely random patterns were measured. At later phases, some intelligence was introduced by allocating weights to the primary inputs in proportion to their relative importance. The main drawback of this concept was high fault coverage was attained only for small circuits.

LFSR (Linear Feedback Shift Register) is used to produce pseudo-random patterns [19]. Exhaustive testing uses all probable combinations of inputs and estimate the cost of all patterns were calculated .This takes a day, week or even a lifetime to test. Next method was to convert the test patterns into weight sets [18]. The deterministic test sets was less appropriate for weight generation. Two main causes for difficult generation of test patterns were the test sets may contain redundant information and they may contain differing information. Differing information mainly contributes to a larger hamming distance. Several conflicts in weight consignment for the input patterns will arise [18]. Best Primary Input Change (BPIC) technique increases the correlation between continuous states but it is not suitable for System on chip (SOC) [14].

V. TRANSITION DENSITY AND ITS EFFECTS

A. Weighted Random Pattern

Weighted random patterns (WRP) in which the probability of 1, p1, instead of being 0.5, can be set to any value in the range [0, 1] have certain benefits. Low power test using weighted random and other reduced activity patterns was already designed. The power dissipation of scan patterns is linked with the transitions they yield in the scan register. For low activity patterns the fault coverage rises slowly and for the same required coverage numerous patterns are needed. Thus, a reduced power test may take longer time. The main purpose of WRP is to raise the rate of fault finding and reduce the test time. They are also used to reduce power consumption.

B. Transition density Patterns

Ratio of no. of transitions to the no. of unit intervals in a serial data stream is in figure 3. Many Serial communication test signals ratio approaches to 0.5. If bits are generated randomly, the probabilities of generating a 1 or a 0 are equal. For example, the transition density of the bit stream is 0.5. To generate a transition density higher or lower than 0.5, bits must be created with negative or positive correlation, respectively. Therefore, the bit stream will contain small number of consecutive 1s or 0s for a transition density higher than 0.5 and large number of consecutive 1s or 0s for a transition density lower than 0.5.

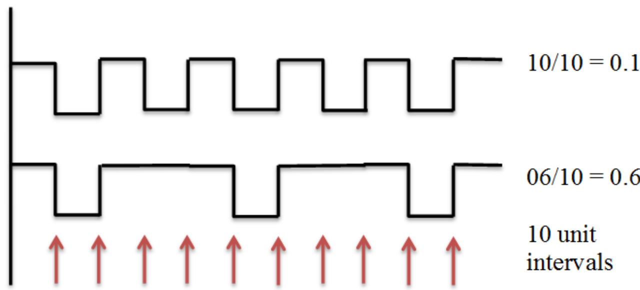

Fig. 3: Transition density in a signal line

A Matlab program was written to create test vector sets, each set containing n vectors but with different transition densities. The range of transition density was from 0.1 to 0.95, with 0.05 intervals. The vector set created for 0.1 transition density has large number of 1s and 0s in consecutive bit positions. Likewise the vector set having transition density of 0.95 has very small number of 1s and 0s in consecutive bit positions.

If bits are generated arbitrarily, the probabilities of generating a 1 or a 0 are equal, i.e., p0 = p1 = 0.5. Hence the transition density of the sequence is also 0.5.

To create a transition density higher or lower than 0.5, bits must be minted with negative or positive correlation, respectively. Therefore, the bit stream will contain small number of consecutive 1s or 0s for a transition density higher than 0.5 and large number of successive 1s or 0s for a transition density lower than 0.5.

VI. EXISTING SYSTEM

A. Test Pattern Generator

Weighted random patterns have been used to reduce test length for combinational circuits. Proper selection of the input probability can increase the effectiveness of test vectors in detecting faults, resulting in reduced test time. Therefore, weighted pseudo random patterns are used to attain greater fault coverage with smaller test lengths.

Weighted random patterns (WRP) in which the probability of 1, p1, instead of being 0.5, can be set to any value in the range [0, 1] have certain gains. The figure 4 contains a 28-bit external linear feedback shift register (LFSR) using the polynomial: $p(x) = x^{28}+x^{3}+1$.

The Scan Bit Generator block contains of AND gates, inverters, an 8-to-1 MUX to select from eight different probabilities of a bit being 1, and a toggle flip-flop. A simple Finite State Machine provides the select inputs to the MUX in the TPG. The Scan Bit Generator produces eight different weighted random bit sequences.

The weights are constructed by AND-ing two or more outputs from non-adjacent cells of the LFSR.

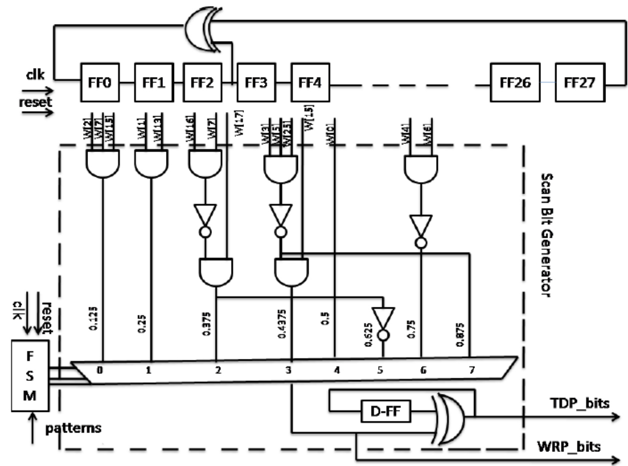

Fig. 4 Test pattern generator (TPG) of a 28bit LFSR

B. Dynamic Control of Scan Clock in a BIST Circuit

The circuit model selected for the analysis is the test-per-scan multiple scan chain based BIST model. To implement this model, flip-flops are added to primary inputs and primary outputs of the circuit under test (CUT).

All flip-flops are converted into scan flip-flops and partitioned into multiple scan chains. A test pattern generator (TPG), a multiple input signature registers (MISR) and a BIST controller is also added. A frequency divider module is added, which delivers either the scan clock or the system clock, based on the mode of operation of the Circuit under Test (CUT). If the circuit is in the system mode, the BIST circuitry that consists of TPG, MISR and BIST controller are kept idle and the circuit runs with the system clock provided by the control clock select block.

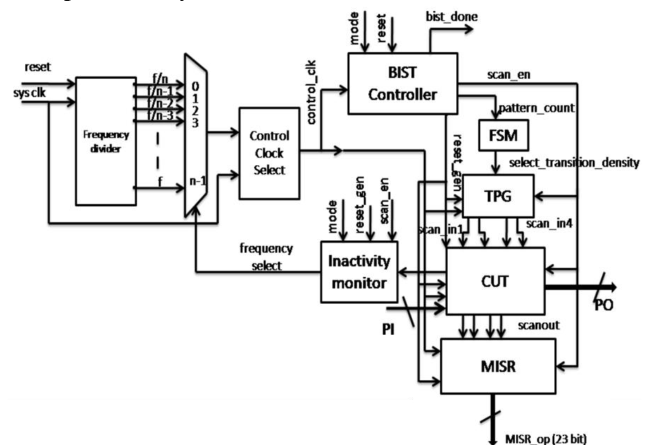

Fig. 5: Dynamic scan clock scheme with TPG

Similarly if the circuit is in test mode then the BIST circuitry is active and the control clock selects the scan clock. Here the frequency of the scan clock is determined by the peak power consumption of the circuit.

A larger frequency divider splits the system clock into n different frequencies, where the fastest clock is the system clock and the slowest frequency is the test clock, based on the peak power consumption as described earlier. An n:1 multiplexer MUX is also added to select from the range of frequencies generated by the frequency divider block.

VII. INACTIVITY MONITOR

The inactivity monitors are simple XNOR gates that produce a 1 whenever inactivity enters the attached scan chain and produces a 0 when an activity enters the scan chain. We feed the output of all monitors to a counter. Depending on the number of lines that are logic 1 at the output of the XNOR gates counter adds from 0 to n (number of scan chains) per clock. Hence all the inactivity that has entered the entire scan chains per clock has been accounted for. If no inactivity enters any of the scan chains, then the counter stays in its previous state by adding 0. If inactivity enters one of the scan chains, the counter counts up by 1, and so on.

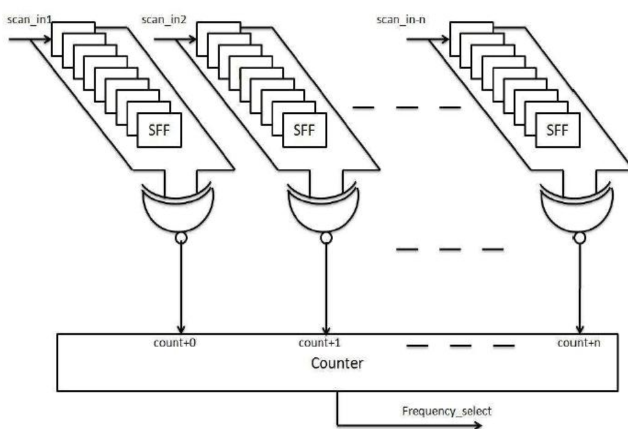

Fig. 6: An inactivity monitor operation with monitors attached to the first scan flip-flop of each chain.

Figure 6 shows the working of the inactivity monitors. Therefore, if inactivity enters every one of the n scan chains, the counter adds n to the prior count. While counting up, if the counter reaches a certain threshold it signals the frequency selector MUX to deploy a higher frequency and hence dynamically adapts the scan frequency according to the inactivity in the chain. The actual hardware consists of an adder, a combinational block with a register and a MUX. At every clock, if a non-activity enters a scan chain, the inactivity monitor attached to the first flip-flop of the scan chain becomes high. The inactivity monitor from every scan chain feeds to a combinational block.

The output of the combinational block is connected to a separate select line of a MUX. The inputs of the MUX are 0, 1, 2... n, where n is the sum of scan chains in the design. The inputs to the adder are the earlier state of the register and the output from the MUX.

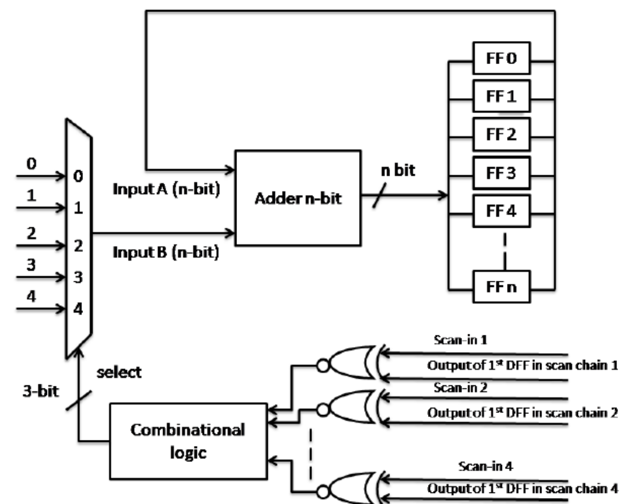

Fig. 7: The inactivity monitor - Hardware implementation

If 1 output of the inactivity monitor is high, the output of the combinational block will be 01 (assuming the number of scan chains in the design to be 4). The first input to the adder is the present state of the register and the second input to adder is the output to the mux. For our example, 1 will be added to the present contents of the register. Hence, at every clock the contents of the register will be reorganized according to the number of inactivity that entered the scan chains.

Likewise, If 1 inactivity enters in each of the scan chains, i.e., if the total number of inactivity is 4, then the combinational circuit output will be 11. This in turn will choose the second input of the adder to be 4. Hence, 4 will be added to the current state of the register. However, if no inactivity enters in any of the scan chains, the combinational circuit will produce 00 outputs. Hence, 0 will be added to the current state of the register.

VIII. PROPOSED SYSTEM

This chapter proposes a new method of implementation of the transition density based vector generation by a BIST-TPG. The first section describes the hardware used to implement the pattern generator, the second section estimates the randomness of the generated vectors and the last section describes the implementation of the TPG in the adaptive scan clock scheme described earlier.

A. BIST-TPG Circuit for Arbitrary Density Patterns

The test pattern generator (TPG) chosen for the analysis is a 28 bit external LFSR using the polynomial $p(x) = x^{28} + x^3 + 1$.

The combinational part consists of only AND gates and inverters, an eight input MUX to select from eight different probability of a bit being 1, a simple Finite State Machine (FSM) to control the MUX, and a toggle flip-flop. Figure 7 shows the circuitry for the test pattern generator. The combinational network generates eight different weighted random bit sequences.

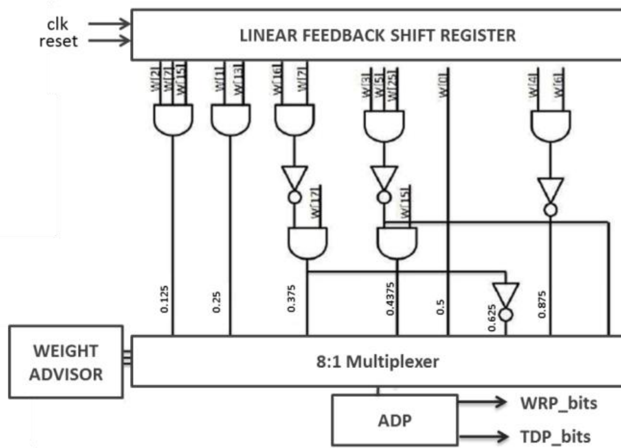

Fig. 8: Block Diagram of TPG.

The weights are made by the logical function of AND of two or more cells of the LFSR. Here it is to be noted that two cells in an n-bit LFSR are adjacent if the output of one cell feeds the input of the second directly, without an intervening XOR gate.

As shown in Figure 7.1, eight weights for the probability of a bit being 1 are 0.125, 0.25, 0.375, 0.4375, 0.5, 0.625, 0.75 and 0.875, respectively. The probability of a bit being 1 or 0 at the output of any cell of the TPG is 0.5. This weight is directly fed to one of the inputs of the MUX. Two outputs from two non-adjacent cells were ANDed to produce a weight of 0.25, three outputs from three non-adjacent cells were ANDed to produce a weight of 0.125, and inverting the

For generating weight of 0.375, weight 0.75 is again ANDed with another cell output that is not adjacent to any of those two cells that are used in creating the 0.75 weight. Similarly for generating weight of 0.4375, weight 0.875 is ANDed with another non-adjacent cell output. Finally, to construct a weight of 0.625, weight 0.375 is inverted.se two weights we get weights of 0.75 and 0.875, respectively

A toggle generating flip-flop constructed with a D-flip-flop and an XOR gate is added to produce the required transition density in the vectors that are to be fed to scan chain. Through the select lines of the MUX a weight is selected and the bit sequence fed to one of the inputs of the XOR gate; the other input line of the XOR gate is the output of the D flip-flop. Once a weight is selected, the corresponding bit sequence will then control the transition at the output of the XOR gate.

A 1 in the bit sequence will produce a transition at the output of the XOR gate and a 0 will produce no transition. Thus the resulting transition density in the bit stream at the output of the XOR gate will have the same weight (i.e., the probability of a transition to occur) as the weight selected from the MUX.

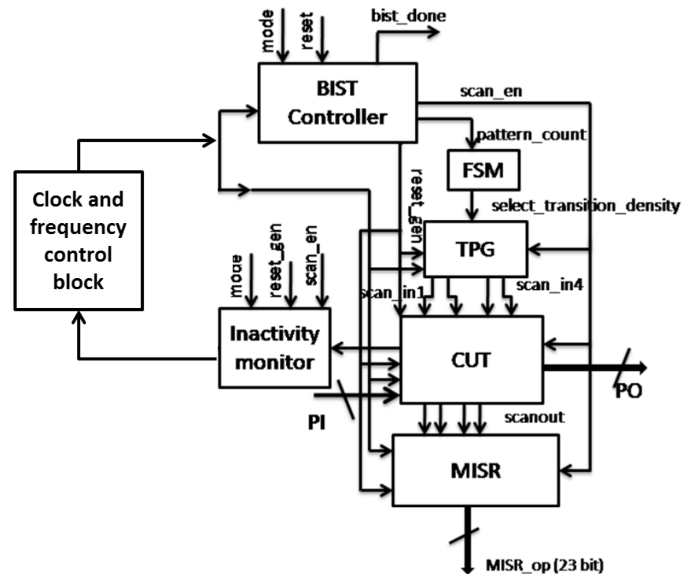

Fig. 9: Implementation of one test per scan vector

IX. Design of Sloth Monitor

The sloth monitor is the major unit which is used to measure the circuit activity during scanning. The input bits are taken parallel form to the sloth monitor. The sloth monitor is built by a novel algorithm based approach by avoiding the logic gates as in the existing system.

A. *Novel algorithm for sloth monitor*

Step 1: Start the sloth monitor
Step 2: Initialize the input variables and count
Step 3: Fix the threshold value for the count in the counter
Step 4: Analyze the parallel input bits from the CUT
Step 5: Separate the bits in according to their position
Step 6: Select a starting frequency
Step 7: Check for inactivity in each successive two bits i, j
Step 8: If two bits are equal, increment the count
Step 9: The count once reaches the threshold, the counter resets to 0 and the frequency is increased by value say 10
Step 10: Continue the same process for entire sequence
Step 11: If 2 bits are unequal count and frequency remains the same
Step 12: Check if all bits in the sequence are scanned
Step 13: Stop the program

The sloth monitor is capable of counting the inactivity and after attaining a particular threshold of count, the frequency is increased to a particular extent. The time period is reduced so that it could test the CUT with the faster frequency. Once the frequency is increased the count value in the counter resets to zero. The frequency is selected from the frequency divider and it is given to the clock select block. This block in turn provides the clock to the other blocks.

B. *Working of Sloth monitor*

The counter states at which the clock is sped up and establishes correlation between the circuit activity and scan chain activity. If each transition in the scan chain causes a

large number of transitions in the circuit, power consumption reaches large values for low scan chain transition numbers. Thus, a large number of scan chain nontransitions should be counted before the scan clock frequency is stepped up. Similarly, if a transition in the scan chain has a small effect on the circuit activity, then only a few nontransitions in the scan chain are sufficient to increase the scan clock frequency.

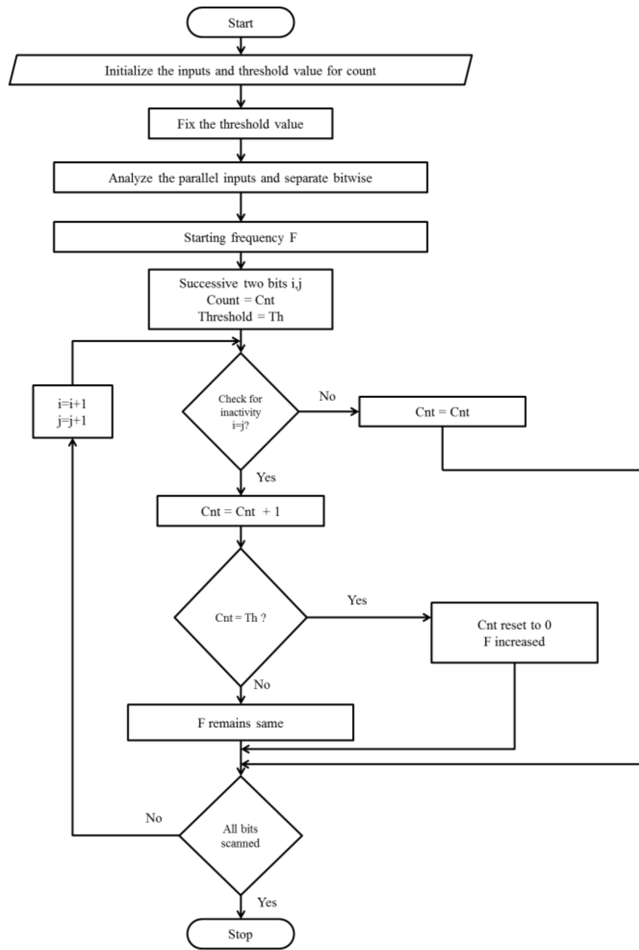

Fig. 10: Flowchart chart for novel algorithm of sloth monitor

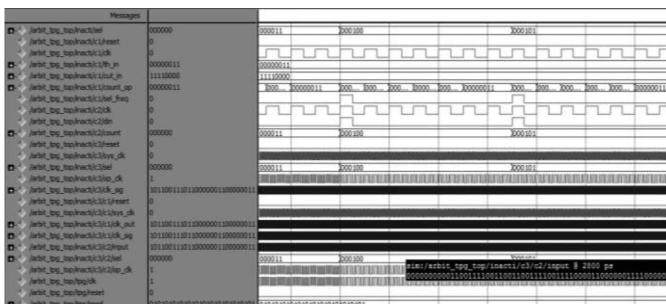

Fig. 11: Sloth Monitor output

Clearly, a bit stream with fewer transitions will be scanned in faster than one with many transitions.

X. MODIFIED TPG USING HAMMING DISTANCE CALCULATOR

A new test pattern generator was designed using ADP (Arbitrary Density Patterns). This ADP uses two types of patterns WRP and TDP.

Weighted random pattern is created by providing the certain weights of probability to the primary inputs of the circuit under test. The weights introduced were useful in giving particular priority to the primary inputs. This type of test patterns if used in testing they reduce the test time by using the probability imparted to the primary inputs.

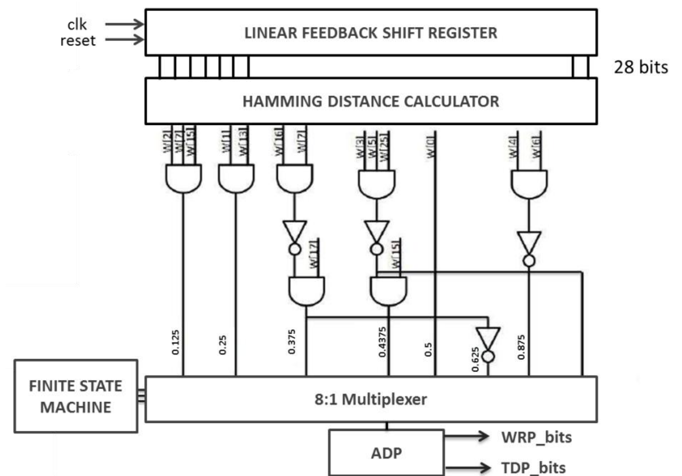

Fig. 12: Modified test pattern generator using HDC

The scan bit generator is the main block which creates weights from the LFSR of the desired polynomial value. Older methods use random sequences to create the arbitrary density patterns. Test pattern generator circuit is modified as to increase the correlation between the samples for creating the weight samples. In order to increase the correlation between samples hamming distance calculator is used. Hamming distance calculator is used to select the LFSR bits with minimum hamming distance. By using low hamming distance the correlation increases thereby reduces the switching activity inside the circuit. This will result in reduced testing vectors and the testing time. Hence low power is consumed for the test power.

XI. RESULTS

A. Circuit parameters

- Family of FPGA board : Cyclone II
- Device inside FPGA : EP2C5T144c6
- Total logic elements : 393
- Total registers : 174
- Chip size : 31
- Total fan-out : 1511

B. Power parameters

- Total thermal power dissipation : 32.62 mW
- Static thermal power dissipation : 18.01 mW
- I/O thermal power dissipation : 14.60 mW

C. Timing parameters

- Worst case timing : 5.701 ns
- Clock setup : 250.13 MHz

- Period : 3.988 ns
- Total CPU time (all processors) : 00:00:02 s

XII. CONCLUSIONS

For testing in scan-BIST circuits, test cost and the quality of the test mainly depends on the test power and testing time. This proposal strikes a balance between test power and test time. This method mainly reduces test application time as much as possible without losing the fault coverage. The lower transition density based vectors needs more number of vectors. More number of test vectors is used to test the CUT. Thus smaller transition density value had to be chosen deterministically to reach that partial coverage while speeding up the scan clock without crossing the power limits.

In the future, more randomization methods for obtaining the transition density mixing in the vector set is used from LFSR (such as Hamming distance or linear programming method). The CUT can be inspected concurrently to reduce the test time and test power more efficiently. Fault coverage for S298 benchmark circuit and the dynamic power for different input test pattern are to be measured.

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TABLE I RESULTS OF SLOTH MONITOR AFTER TESTING THE CUT (S298 BENCHMARK CIRCUIT - 14 FLIP FLOPS) FOR THRESHOLD VALUE OF COUNT 3

PI test pattern	Time period of starting frequency	Time period after scanning the sequence	Time (ns)	System time (s)	Transition count	Nontransitions count
00001111000000	80ns	50ns	860	0.02	2	11
11001100110011	80ns	60ns	940	0.02	6	7
00110011111100	80ns	60ns	920	0.02	4	9
11111111111111	80ns	40ns	820	0.02	0	13