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A REVIEW ON MICROPROCESSOR AND MICROPROCESSOR SPECIFICATION

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Abstract: The evolution of microprocessor architecture depends upon the changing aspects of technology. As die density and speed increase, memory and program behaviour become increasingly important in defining architecture tradeoffs. While technology enables increasingly complex processor implementations, there are physical and program behaviour limits to the usefulness of this complexity. Physical limits include device limits as well as practical limits on power and cost. Program behaviour limits resultfrom unpredictable events occurring during execution. Architectures and implementations that span these limits are vital to the continued evolution of the microprocessor.This paper illustrates architecture techniques used by Intel in the family of processors to maintain this leadership position.

Keywords: microprocessor architecture, specification ,computer,microprocessor history

I.INTRODUCTION

Computer: It is electronics programmable logic system. Which consists of CPU memory and I/O interfaces in which with the help of memory and I/O interfaces CPU executes the programme to performs basic various arithmetic and logical operation and digital data world to meet specific task .

Microprocessor: An integrated circuit that contain all the function of CPU of computer .

Everyone who works in the computer industry is well familiar with Moore's Law and the doubling of the number of transistors (an approximate measure of computer processing power) every 18 to 24 months. Until recently, overall microprocessor performance was often described in terms of processor clockspeeds, expressed in megahertz (MHz) or gigahertz (GHz).Today there's far more than clock speed to consider when you're evaluating how a given processor will perform for a given application and where it fits on the performance scale. Microprocessor designers today are more focused on methods that leverage the latest silicon production processes and designs that minimize microprocessor footprint size, power consumption and heat generation.

Designers are also concerned with microarchitecture optimization, multiprocessing parallelism, reliability, designed-in security features, memory structure efficiency and better synergy between the hardware and accompanying software tools, such as compilers. The more attention that a designer devotes to refining the efficiency of the software code rather than making the hardware responsible for dynamic optimization, the higher the ultimate system performance will be.

As an example, the Intel® Itanium® processor family has been designed around small footprint cores that are remarkably compact in terms of transistor count, especially when one considers the amount of processing work that theyaccomplish. Itanium has taken instruction level parallelism to a new level, and this can be used in conjunction with thread level parallelism to leverage more processor cores and more threads per core to produce higher performance.

Some microprocessor designs of the past have been overly complex and have relied on out-of-order logic to reshuffle and optimize software instructions. Going forward, microprocessor designers will continue to deliver better and bettersoftware tools, higher software optimization and better compilers.Because it is so efficient and so small and doesn't depend on out-of-order logic, the latest generation Itanium processor can deliver higher performance without creating thermal generation problems. This makes Itanium a very simple yet efficient and refined engine that enables more consistent long-term improvement in code execution via small improvements in software, thus reducing the need for significant advancements in hardware. These are becoming more and moredifficult to accomplish as, even Gordon Moore believes, the exponential upward curve in microprocessor hardware advancements “can’t continue forever.”

Successful microprocessor implementations depend upon the processor architect's ability to predict trends and advances in both technology and user behaviour. Selecting an approach for a microprocessor implementation depends on the architect's ability to correctly model the effect of new technologies, new applications, and new software and CAD tools. Themost successful microprocessor implementations depend not simply on the use of the current state of the art in hardware algorithms, but more importantly in bringing together the knowledge of these algorithms together with projected advances in the technology and user state of the art.

II. THE HISTORY OF THE MICROPROCESSOR

The microprocessor, which evolved from the inventions of the transistor and the integrated circuit (IC), is today an icon of the information age. The per-vasiveness of the microprocessor in this age goes far beyond the wildest imagination at the time of the firstmicroprocessor. From the fastest computers to the simplest toys, the microprocessor continues to find new applications. The microprocessor today represents the most complex application of the transistor, with well over 10 million transistors on some of the most powerful microprocessors. In fact, throughout its history, the microprocessor has always pushed the technology of the day. The desire for ever-increasing performance has led to the rapid improvements in technology that have enabled more complex microprocessors.As trace the history of the microprocessor, will explore its evolution and the drivingforces behind this evolution. In the earliest stages, microprocessors filled the needs of embedded applications. It was not long, however before advances in microprocessors and computers drove the capabilities and needs of both.[4][8]

A Leading Role for the Microprocessor

The early to mid-1980s marked the period when microprocessors, through desktop systems came to be known to a wider public than the micro-computer hobbyists and embedded system developers. Desktop systems such as PCs and workstations prominently featured their microprocessors. The microcontrollers contained in a myriad of embedded applications were largely anonymous. This period saw a shakeout in the microprocessor industry. Critical markets, such as the PC market, quickly established dominant vendors. However, by the end of this period, new processor architectures werechallenging the established players. Significant developments in OSs and software, which would greatly change the microprocessor landscape in the future, occurred at this time.

By the late 1970s, many of the early microprocessors were already fading from the centre stage. Many semiconductor manufacturers had developed 4-bit and 8-bit microprocessors. Many of these devices were profitable in embedded applications none had the impact of later 16-bit devices from Intel and Motorola. Early embedded applications such as watches and calculators offered ever-decreasing profits as these markets matured. A recession from 1981 to 1984 did not help either, forcing retrenchment by most large and small microprocessor vendors. The rise of desktop computers offered a market that, like embedded applications, consumed high volumes, but also offered high profit margins.

III. INTERNAL ARCHITECTURE OF 8085 MICROPROCESSOR

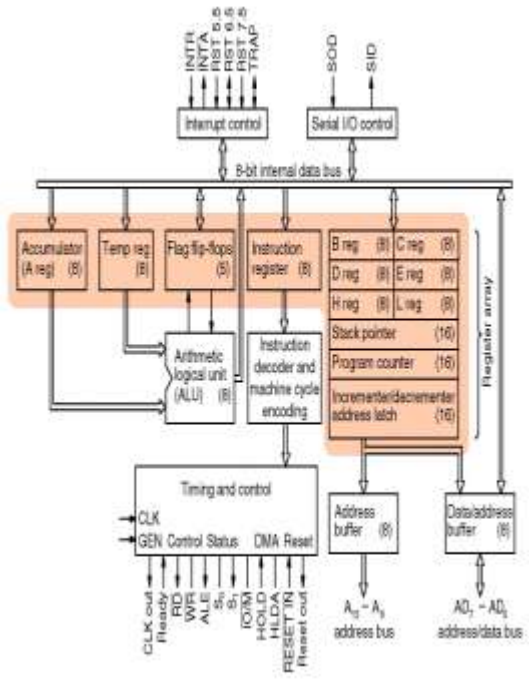

Fig.1. Internal Architecture Of 8085 Microprocessor

Control Unit

Generates signals within uP to carry out the instruction, which has been decoded. Inreality causes certain connections between blocks of the uP to be opened or closed, sothat data goes where it is required, and so that ALU operations occur.

Arithmetic Logic Unit

The ALU performs the actual numerical and logic operation such as ‘add’, ‘subtract’,‘AND’, ‘OR’, etc. Uses datafrom memory and from Accumulator to performarithmetic. Always stores result of operation in Accumulator

Registers

The 8085/8080A-programming model includes six registers, one accumulator, andone flag register, as shown in Figure. In addition, it has two 16-bit registers: the stackpointer and the program counter. They are described briefly as follows.The 8085/8080A has six general-purpose registers to store 8-bit data; these areidentified as B,C,D,E,H, and L as shown in the figure. They can be combined asregister pairs - BC, DE, and HL - to perform some 16-bit operations. Theprogrammer can use these registers to store or copy data into the registers by usingdata copy instructions.

Accumulator

The accumulator is an 8-bit register that is a part of arithmetic/logic unit (ALU). Thisregister is used to store 8-bit data and to perform arithmetic and logical

operations.The result of an operation is stored in the accumulator. The accumulator is alsoidentified as register A.

Flags

The ALU includes five flip-flops, which are set or reset after an operation accordingto data conditions of the result in the accumulator and other registers. They are calledZero(Z), Carry (CY), Sign (S), Parity (P), and Auxiliary Carry (AC) flags; they arelisted in the Table and their bit positions in the flag register are shown in the Figure The most commonly used flags are Zero, Carry, and Sign.

The microprocessoruses these flags to test data conditions.For example, after an addition of two numbers, if the sum in the accumulator id largerthan eight bits, the flip-flop uses to indicate a carry -- called the Carry flag (CY) – isset to one. When an arithmetic operation results in zero, the flip-flop called theZero(Z) flag is set to one. The first Figure shows an 8-bit register, called the flagregister, adjacent to the accumulator. However, it is not used as a register; five bitpositions out of eight are used to store the outputs of the five flip-flops. The flags arestored in the 8-bit register so that the programmer can examine these flags (dataconditions) by accessing the register through an instruction.These flags have critical importance in the decision-making process of the microprocessor.The conditions (set or reset) of the flags are tested through the softwareinstructions. For example, the instruction JC (Jump on Carry) is implemented tochange the sequence of a program when CY flag is set. The thorough understandingof flag is essential in writing assembly language programs.

Program Counter (PC)

This 16-bit register deals with sequencing the execution of instructions. This registeris a memory pointer. Memory locations have 16-bit addresses, and that is why this is a16-bit register.The microprocessor uses this register to sequence the execution of the instructions.The function of the program counter is to point to the memory address from which thenext byte is to be fetched. When a byte (machine code) is being fetched, the programcounter is incremented by one to point to the next memory location.

Stack Pointer (SP)

The stack pointer is also a 16-bit register used as a memory pointer. It points to amemory location in R/W memory, called the stack. The beginning of the stack isdefined by loading 16-bit address in the stack pointer. The stack concept is explainedin the chapter "Stack and Subroutines."

Instruction Register/Decoder

Temporary store for the current instruction of a program. Latest instruction sent herefrom memory prior to execution. Decoder then takes instruction and 'decodes' orinterprets the instruction. Decoded instruction then passed to next stage.Memory Address RegisterHolds address, received from PC, of next program instruction. Feeds the address bus
with addresses of location of the program under execution.

Control Generator

Generates signals within uP to carry out the instruction which has been decoded. Inreality causes certain connections between blocks of the uP to be opened or closed, sothat data goes where it is required, and so that ALU operations occur.Register SelectorThis block controls the use of the register stack in the example. Just a logic circuit
which switches between different registers in the set will receive instructions fromControl Unit.

General Purpose Registers

uP requires extra registers for versatility. Can be used to store additional data during a
program. More complex processors may have a variety of differently named registers.

Microprogramming

How does the µP knows what an instruction means, especially when it is only a
binary number? The microprogram in a uP/uC is written by the chip designer and tells
theuP/uC the meaning of each instruction uP/uC can then carry out operation.[1]

IV PAST EFFORTS TO INCREASE EFFICIENCY

From the introduction of Intel‟s 8086 through the Pentium 4 an increase in performance, from one generation to the next, was seen as an increase in processor frequency. For ex-ample, the Pentium 4 ranged in speed (frequency) from 1.3 to 3.8 GHz over its 8 year lifetime. The physical size of chips decreased while the number of transistors per chip increased; clock speeds in-creased which boosted the heat dissipation across the chip to a dangerous level.

To gain performance within a single core many techniques are used. Superscalar processors with the ability to issue multiple instructions concur-rently are the standard. In these pipelines, instruc-tions are pre-fetched, split into sub-components and executed out-of-order. A major focus of computer architects is the branch instruction. Branch instructions are the equivalent of a fork in the road; the processor has to gather all neces-saryinformation before making a decision. In order to speed up this process, the processor pre-dicts which path

will be taken; if the wrong path is chosen the processor must throw out any data computed while taking the wrong path and backtrack to take the correct path. Often even when an incorrect branch is taken the effect is equivalent to having waited to take the correct path. Branches are also removed using loop unrolling and sophisticated neural network-based predic-tors are used to minimize the misprediction rate. Other techniques used for performance en-hancement include register renaming, trace caches, reorder buffers, dynamic/software schedul-ing, and data value prediction. There have also been advances in power- and temperature-aware architectures. There are two flavors of power-sensitive architectures: low-power and power-aware designs. Low-power ar-chitectures minimize power consumption while satisfying performance constraints, e.g. embed-ded systems where low-power and real-time performance are vital. Power-aware architectures maximize performance parameters while satisfying power constraints. Temperature-aware design uses simulation to determine where hot spots lie on the chips and revises the architecture to decrease the number and effect of hot spots.[2][6]

V TECHNICAL SPECIFICATIONS OF DIFFERENT PROCESSOR

4004:[4 bit]

- Maximum clock speed was 740 kHz
- Instruction cycle time: 10.8 µ (8 clock cycles / instruction cycle)
- Instruction execution time 1 or 2 instruction cycles (10.8 or 21.6 µs), 46300 to 92600 instructions per second
- Separate program and data storage. Contrary to Harvard architecture designs, however, which use separate buses, the 4004, with its need to keep pin count down, used a single multiplexed 4-bit bus for transferring:
  - 12-bit addresses
  - 8-bit instructions
  - 4-bit data words
- Instruction set contained 46 instructions (of which 41 were 8 bits wide and 5 were 16 bits wide)
- Register set contained 16 registers of 4 bits each
- Internal subroutinestack 3 levels deep.

8008[8bit]

- Clock rate 500 kHz (8008–1: 800 kHz)
- 0.05 MIPS
- Bus Width 8 bits (multiplexed address/data due to limited pins)
- Enhancement load PMOS logic
- Number of Transistors 3,500 at 10 µm
- Addressable memory 16 KB
- Typical in early 8-bit microcomputers, dumb terminals, general calculators, bottling machines
- Developed in tandem with 4004
- Originally intended for use in the Datapoint 2200 microcomputer
- Key volume deployment in Texas Instruments 742 microcomputer in >3,000 Ford dealerships

8085[8 bit]

- Clock rate 3 MHz
- 0.37 MIPS
- Bus Width 8 bits data, 16 bits address
- Depletion load NMOS logic
- Number of Transistors 6,500 at 3 µm
- Binary compatible downwards with the 8080.
- Used in Toledo scales. Also was used as a computer peripheral controller – modems, hard disks, printers, etc.
- CMOS 80C85 in Mars Sojourner, Radio Shack Model 100 portable.
- High level of integration, operating for the first time on a single 5-volt power supply, from 12 volts previously. Also featured serial I/O, 3 maskable interrupts, 1 non-maskable interrupt, 1 externally expandable interrupt w/[8259], status, DMA.
- MCS-85 family contains processors and peripherals

8086[16 bit]

- Introduced June 8, 1978
- Clock rates:
- 5 MHz with 0.33 MIPS
- 8 MHz with 0.66 MIPS
- 10 MHz with 0.75 MIPS
- The memory is divided into odd and even banks; it accesses both banks concurrently to read 16 bits of data in one clock cycle
- Bus Width 16 bits data, 20 bits address
- Number of Transistors 29,000 at 3 µm
- Addressable memory 1 megabyte
- Up to 10X the performance of 8080
- Used in portable computing, and in the IBMPS/2 Model 25 and Model 30. Also used in the AT&T PC6300 / Olivetti M24, a popular IBM PC-compatible (predating the IBM PS/2 line).
- Used segment registers to access more than 64 KB of data at once, which many programmers complained made their work excessively difficult

iAPX 432 [32 bit]

- Multi-chip CPU; Intel's first 32-bit microprocessor
- Object/capability architecture

- Microcoded operating system primitives
- One terabyte virtual address space
- Hardware support for fault tolerance
- Two-chip General Data Processor (GDP), consists of 43201 and 43202
- 43203 Interface Processor (IP) interfaces to I/O subsystem
- 43204 Bus Interface Unit (BIU) simplifies building multiprocessor systems
- 43205 Memory Control Unit (MCU)
- Architecture and execution unit internal data base paths 32 bit
- Clock rates:
  - 5 MHz
  - 7 MHz
  - 8 MHz

80386 [32 bit]

- Clock rates:
  - 16 MHz with 5 MIPS
  - 20 MHz with 6 to 7 MIPS, introduced February 16, 1987
  - 25 MHz with 7.5 MIPS, introduced April 4, 1988
  - 33 MHz with 9.9 MIPS (9.4 SPECint92 on Compaq/i 16K L2), introduced April 10, 1989
- Bus Width 32 bits data, 32 bits address
- Number of Transistors 275,000 at 1 µm
- Addressable memory 4 GB
- Virtual memory 64 TB
- First x86 chip to handle 32-bit data sets
- Reworked and expanded memory protection support including paged virtual memory and virtual-86 mode, features required at the time by Xenix and Unix. This memory capability spurred the development and availability of OS/2 and is a fundamental requirement for modern operating systems like Linux, Windows, and Mac OS.
- Used in desktop computing

P5 [32 bit]

- Bus width 64 bits
- System bus clock rate 60 or 66 MHz
- Address bus 32 bits
- Addressable Memory 4 GB
- Virtual Memory 64 TB
- Superscalar architecture
- Runs on 5 volts
- Used in desktops
- 8 KB of instruction cache
- 8 KB of data cache
- P5 – 0.8 µm process technology
  - Number of transistors 3.1 million
  - Socket 4 273 pin PGA processor package
  - Package dimensions 2.16" × 2.16"
  - Family 5 model 1
  - Variants
    - 60 MHz with 100 MIPS (70.4 SPECint92, 55.1 SPECfp92 on Xpress 256 KB L2)
    - 66 MHz with 112 MIPS (77.9 SPECint92, 63.6 SPECfp92 on Xpress 256 KB L2)

Pentium II [32 bit]

- Pentium Pro with MMX and improved 16-bit performance
- 242-pin Slot 1 (SEC) processor package
- Slot 1
- Number of transistors 7.5 million
- 32 KB L1 cache
- 512 KB ½ bandwidth external L2 cache
- The only Pentium II that did not have the L2 cache at ½ bandwidth of the core was the Pentium II 450 PE.

Xeon[64 bit]

- Server and Workstation CPU (SMP support for dual CPU system)
- Introduced June 26, 2006
- Dual-Core
- Intel VT-x, multiple OS support
- EIST (Enhanced Intel SpeedStep Technology) in 5140, 5148LV, 5150, 5160
- Execute Disable Bit
- TXT, enhanced security hardware extensions
- SSSE3SIMD instructions
- iAMT2 (Intel Active Management Technology), remotely manage computers
- Variants
  - Xeon 5160 – 3.00 GHz (4 MB L2, 1333 MHz FSB, 80 W)

Core i3

- **Clarkdale** – 32 nm process technology
  - 2 physical cores/4 threads
  - 64 Kb L1 cache
  - 512 Kb L2 cache
  - 4 MB L3 cache
  - Introduced January, 2010
  - Socket 1156 LGA
  - 2-channel DDR3
  - Integrated HD GPU

Celeron[64 bit]

Sandy Bridge – 32 nm process technology

- 2 physical cores/2 threads (500 series), 1 physical core/1 thread (model G440) or 1 physical core/2 threads (models G460 & G465)

- 2 MB L3 cache (500 series), 1 MB (model G440) or 1.5 MB (models G460 & G465)
- Introduced 3rd quarter, 2011
- Socket 1155 LGA
- 2-channel DDR3-1066
- 400 series has max TDP of 35 W
- 500-series variants ending in 'T' have a peak TDP of 35 W, others – 65 W
- Integrated GPU
    - All variants have peak GPU turbo frequencies of 1 GHz
    - Variants in the 400 series have GPUs running at a base frequency of 650 MHz
    - Variants in the 500 series ending in 'T' have GPUs running at a base frequency of 650 MHz; others at 850 MHz
    - All variants have 6 GPU execution units[9]

CONCLUSIONS:

A microprocessor is a single chip integrating all the functions of a central processing unit (CPU) of a computer. It includes all the logical functions, data storage, timing functions and interaction with other peripheral devices. In some cases, the terms 'CPU' and 'microprocessor' are used interchangeably to denote the same device. Like every genuine engineering marvel, the microprocessor too has evolved through a series of improvements throughout the 20th century. With the development of microprocessor the number of transistor, clock rate width of bus, Addressable memory increases. According to the applications appropriate processor will be select

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