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Performance Evaluation of Booth Encoded Multipliers for High Accuracy DWT Applications

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***Abstract*--In this momentary, a booth encoded multiplier is projected. The proposed booth encoded multiplier is derived from theoretical computation, instead of exhaustive simulation and heuristic compensation strategies that tend to introduce curve fitting errors. Consequently the proposed system provides reduced area, leakage power with the existing work. The booth encoded multiplier in turn improves the peak signal to noise ratio and the accuracy gets improved when compared with the existing method. The booth encoded multiplier is proposed for Digital Wavelet Transform (DWT). The DWT in turn provides good location in both time and spatial frequency. It also provides better identification of which data is relevant for higher compression than the existing system of DCT applications.**

In the proposal the booth encoded Wallace tree multiplier is projected in order to increase the accuracy and also to deduce the total power consumption and the leakage power could also be reduced. The proposed system in turn provides an improvement in peak signal to noise ratio (PSNR) values with the reduced area penalty.

***Index terms*: Digital Wavelet Transform (DWT), Booth encoder, probabilistic analysis, fixed width booth multiplier and Wallace Tree Multiplier.**

1. INTRODUCTION

The booth encoded multipliers generate an output with the increased accuracy and high performance. They are widely used in digital signal processing systems, such as Discrete Wavelet Transform (DWT), finite-impulse-response filter, and fast Fourier transform. The computation error is introduced if the least significant (LS) half part is directly truncated. To reduce the computation error there are many compensation techniques were presented for array multipliers. The compensation works have been focused on reducing the truncation error on the Booth multiplier for the DWT applications. In this paper Statistical and linear regression analysis developed to reduce the hardware complexity. The truncation error was partly depressed because the estimating information that came from the truncated part is limited. Exhaustive simulations and heuristic compensation strategies may introduce curve fitting errors. However these circuits consume more hardware overhead.

This study proposes a probabilistic estimation bias (PEB) method for reducing the truncation error in a fixed-width Booth multiplier in DWT applications. The probabilistic estimation bias (PEB) formula is derived from the probabilistic analysis in the partial product array after the Booth encoder. The low-error and area-efficient PEB circuit is obtained based on the simple and systematic procedure. The time-consuming exhaustive simulation and the heuristic design process of the compensation circuit can be avoided. The DWT can probably increase the compression time and better identification of relevant information in higher compression techniques

II. FIXED WIDTH BOOTH MULTIPLIER

A probabilistic estimation bias (PEB) circuit for a fixed-width two's-complement Booth multiplier. The existing PEB circuit is derived from theoretical computation is used instead of exhaustive simulations and heuristic compensation strategies that tend to introduce curve-fitting errors and exponential-grown simulation time.

Consequently, the PEB circuit provides a smaller area and a lower truncation error compared with the previous works. Implemented in an 8 × 8 2-D discrete cosine transform (DCT) core, the DCT core using the PEB Booth multiplier improves the peak signal-to-noise ratio by 17 dB with only a 2% area penalty compared with the direct-truncation method.

The fixed-width multiplier is attractive to many multimedia and digital signal processing systems which are desirable to maintain a fixed format and allow a little accuracy loss to output data. In addition, a simple compensation circuit mainly composed of the simplified sorting network is also used.

Probabilistic estimation bias (PEB) method for reducing the truncation error in a fixed-width Booth multiplier. In this the PEB formula is derived from the probabilistic analysis in the partial product array after the Booth encoder. The low-error and area-efficient PEB circuit is obtained based on the simple and systematic procedure. Reduces the area and truncation errors. Fixed width modified booth multipliers are used to reduce the area.

The disadvantages of the existing techniques are:

1. Leakage power
2. Total power
3. Accuracy
4. Peak-signal to Noise ratio(PSNR)

A. Existing System Block Diagram

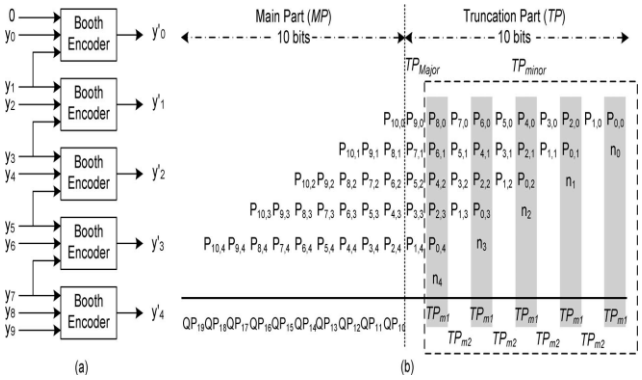


Fig 2.1 Example of 10 × 10 Booth multiplier. (a) Booth encoder. (b) Partial product array: MP and TP.

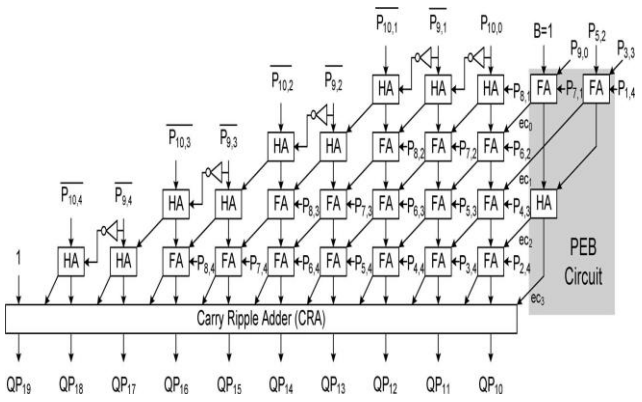


Fig 2.2 Fixed-width 10-bit multiplier with the proposed PEB circuit.

Modified Booth encoding is popular to reduce the number of partial products [16]. Two L-bit inputs X and Y , and a 2L-bit standard product SP (without truncation error) can be expressed in two's complement representation as follows:

$$SP=X*Y \qquad (1)$$

The modified Booth encoder maps three concatenated inputs y2i-1, y2i-1, and y2i-1 into yi',where P{ yi'} stands for the probability of yi'. After encoding, there are Q = L/2 rows in the partial product array with an even width L. The corresponding partial products, where the last column ni stands for the sign of each partial product. According to The partial product array can be divided into two parts: the main part (MP), which includes ten most significant columns (MSCs), and the truncation part (TP), which includes ten LS columns (LSCs). The SP can be rewritten as follows:

$$SP = MP + TP. \qquad (2)$$

In the fixed-width multiplication, TP can be estimated and the quantized product QP can be defined as

$$QP = MP + \sigma \bullet 2L \qquad (3)$$

where σ representing the estimation bias (EB) from TP can be further decomposed into TPMajor (MSC of TP) and TPminor (LSCs of TP) parts as

$$\sigma = \text{Round}((1/2)TPMajor + TPminor) \qquad (4)$$

$$TPMajor = PL{-}1{-}2j,j \qquad (5)$$

$$TPminor = TPm1 + TPm2 \qquad (6)$$

Where Round (k) is rounding k to the nearest integer. In Fig. 1, because TPMajor affects more than TPminor while contributing toward the EB σ, the σ value can be obtained by calculating TPMajor and estimating TPminor in order to reduce truncation errors. In our analysis of estimation, expected values on all elements including ni in TPminor are derived. It is straightforward to compute the expected value of P0,i ($i \neq 0$) to be

$$E[P0,i] = \sum_{k=\{1,-1,2,-2\}} P\{P0,i = 1 \mid yi' = k\} \bullet P\{yi' = k\}$$

$$=12(2/8)+12(2/8)+ 0\ (1/8)+ 1(1/8)$$
$$=3/8. \qquad (7)$$

Similarly, the expected value E[ni] is equal to 3/8. Second,when we calculate the expected values of E[P0,0] and E[n0] in the LSC of TPminor, only four conditions marked as gray rows in Table I occur. The expected value E[P0,0] can be derived as follows:

$$E[P0,0] = \sum_{k=\{1,-1,-2\}} P\{P0,0 = 1 \mid yi' = k\} \bullet P\{yi' = k\}$$

$$=1/2\bullet\ 1/4+1/2\bullet\ 1/4+ 1(1/4)$$

$$=1/2. \qquad (8)$$

Similarly, the expected value E[n0] is 1/2 as well. Hence, the expected values of all Elements (including ni) in TPminor are obtained as follows:

Case 1: Elements in the LSC

$$E[P0,0] =1/2= E[n0]. \qquad (9)$$

Case 2: Other elements

$$E[Pj,i] =3/8= E[ni]. \qquad (10)$$

III. WAVELET COMPRESSION

They compared the quality of JPEG compressed images against the quality of images compressed with a variety of wavelet filters, in terms of the SNR and the subjective image quality. They looked at 3 important classes of images: 4 natural images, 3 synthetic images and 4 textual images were used. While the DCT-based image coders perform very well at moderate bit rates at higher compression ratios, image quality degrades because of

the artifacts resulting from the block-based DCT scheme. Wavelet based coding on the other hand provides substantial improvement in picture quality at low bit rates because of overlapping basis functions and better energy compaction property of wavelet transforms. Because of the inherent multi resolution nature, wavelet-based coders facilitate progressive transmission of images thereby allowing variable bit rates. The upcoming JPEG-2000 standard will incorporate many of these research works and will address many important aspects in image coding for the next millennium. The current data compression methods might be far away from the ultimate limits imposed by the underlying structure of specific data sources such as images. Interesting issues like obtaining accurate models of images, optimal representations of such models, and rapidly computing such optimal representations are the "Grand Challenges" facing the data compression community. Interaction of harmonic analysis with data compression, joint source-channel coding, image coding based on models of human perception, scalability, robustness, error resilience and complexity are a few of the many outstanding challenges in image coding to be fully resolved and may affect image data compression performance in the years to come. The images were all 256 by 256 in size.

Figure 3.1 Top to Bottom:Lena, Barabara,

3.1. Advantages of DWT over DCT

It provides higher compression ratios & avoids blocking artefacts. Allows good localization both in spatial & frequency domain. Transformation of the whole image introduces inherent scaling. Better identification of which data is relevant to human perception, higher compression ratio.

IV. OVERVIEW OF WALLACE TREE MULTIPLICATION

Wallace tree reduction is an well-organized technique, easy for hardware manufacturing,which is derived by an Australian Computer Scientist Chris Wallace. To carry out the unsigned multiplication, the shifted copies of the multiplicand are added to generate the result. The entire procedure is divided into three steps: partial product (PP) generation, partial product grouping & reduction, and final addition.

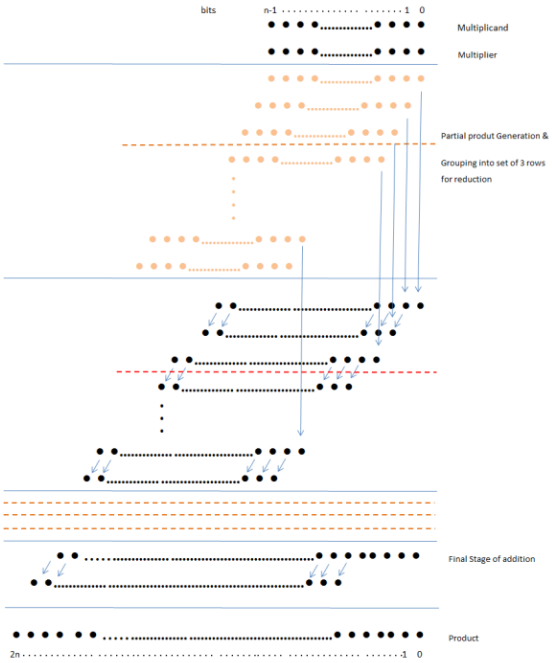
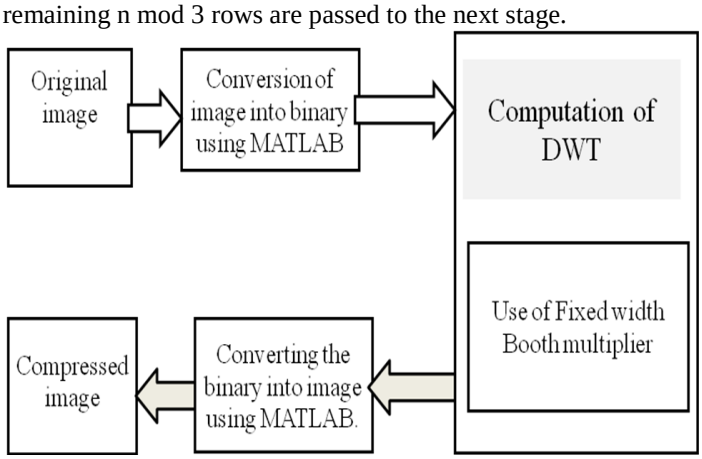


Fig. 4.1. n*n Conventional Wallace tree multiplier

The principle of Wallace tree multiplication [8] is shown in Fig. 4.1. It is clear from the figure that for an n x n multiplication there are n^2 partial products are generated that must be added with respective adders to form a result. The Initial step in the algorithm is to generate the partial products which involve grouping the partial products into sets of 3. For example, if there are _n' rows of partial products, 3*[n/3] rows are grouped and the remaining n mod 3 rows are passed to the next stage.



Therefore in the Fig. 4.1, three rows of generated partial products are grouped together initially. Then these 3 rows are summed using adders and if there are 2 dots in a single column then half adders are used. The sum and carry signals generated from the adders are passed to the next stage. The process is repeated till the entire n partial products are added using respective adders. The sum and carry out of the final stage is added using a carry propagation adder.

V. APPLICATION OF WALLACE TREE MULTIPLIER IN IMAGE PROCESSING

They have implemented our proposed Wallace tree multiplier with ETA (m=8) for image smoothening. They represented the image pixel values in integer with each pixel representing a color on gray scale. To compare the performance of the proposed error tolerant Wallace tree multiplier, They fed the integer matrix of camera man image to an averaging filter implemented with our multiplier and conventional array multiplier. The matrix output was then transformed back to image.

a)

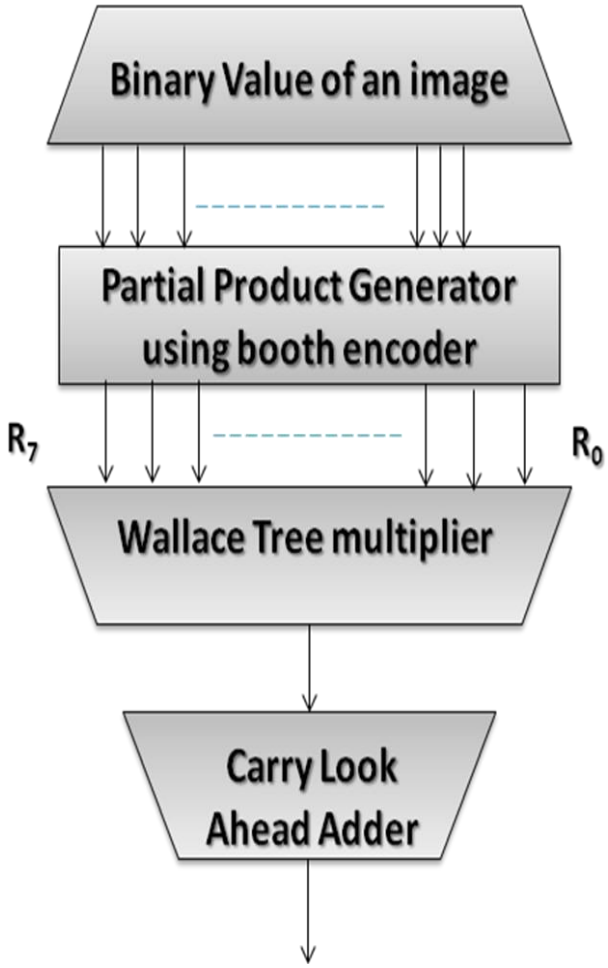
b)

Fig.5.1. Image processed by implemented with
(a) Booth multiplier (b)Wallace tree multiplier
(b) ETA (m=8).

in intermediate stages and Error Tolerant addition arithmetic at final stage of tree reduction in a Wallace multiplier is described which spares some accuracy. Extensive comparison shows that our proposed Wallace tree multiplier outperformed all other previous designs in terms of delay and area performance. The potential benefits of delay performance of our proposed multiplier can be realized in fair Area-Delay-product (ADP) saving and Power-Delay-Product (PDP) saving performance. The suitability of our proposed Wallace tree multiplier mainly falls in the area of digital image processing where some amount of error is tolerable.

VI. BOOTH ENCODED WALLACE TREE

The Booth Encoded Wallace Tree Multiplier in turn uses the booth encoder for the generation of partial products. Since, Wallace Tree has 3 phase of generating partial product, reducing and final addition. The partial products generation is carried out using the Booth encoder, then the reduction of partial into two stream of data's are carried out using the Wallace tree multiplier and then the final addition of two data are carried out through carry look ahead generator



1. Booth encoding is an effective method for multiplication of both positive and negative numbers.
2. Wallace tree reduces the number of partial products to be added into 2 final intermediate results.
3. Carry Look-ahead Adder used to add these results to generate the final output.

7. PROCESS AND PERFORMANCE

The Proposed System Of Booth encoded Wallace Tree Multiplier for DWT applications are carried out which in turn improves the accuracy of the compressed image and reduces the total power consumption also. When compared with the existing method the proposed system has the same size whereas the accuracy, PSNR values are gets increased. The fig 7.1 shows the design flow of the proposed system of booth encoded Wallace tree multiplier using the DWT (Discrete Wavelet Transform).

PowerPlay Power Analyzer Status	Successful - Sat Dec 15 21:10:31 2012
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	wallace_code
Top-level Entity Name	wallace_mult
Family	Cyclone II
Device	EP2C5T144C6
Power Models	Final
Total Thermal Power Dissipation	32.16 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	18.01 mW
I/O Thermal Power Dissipation	14.15 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

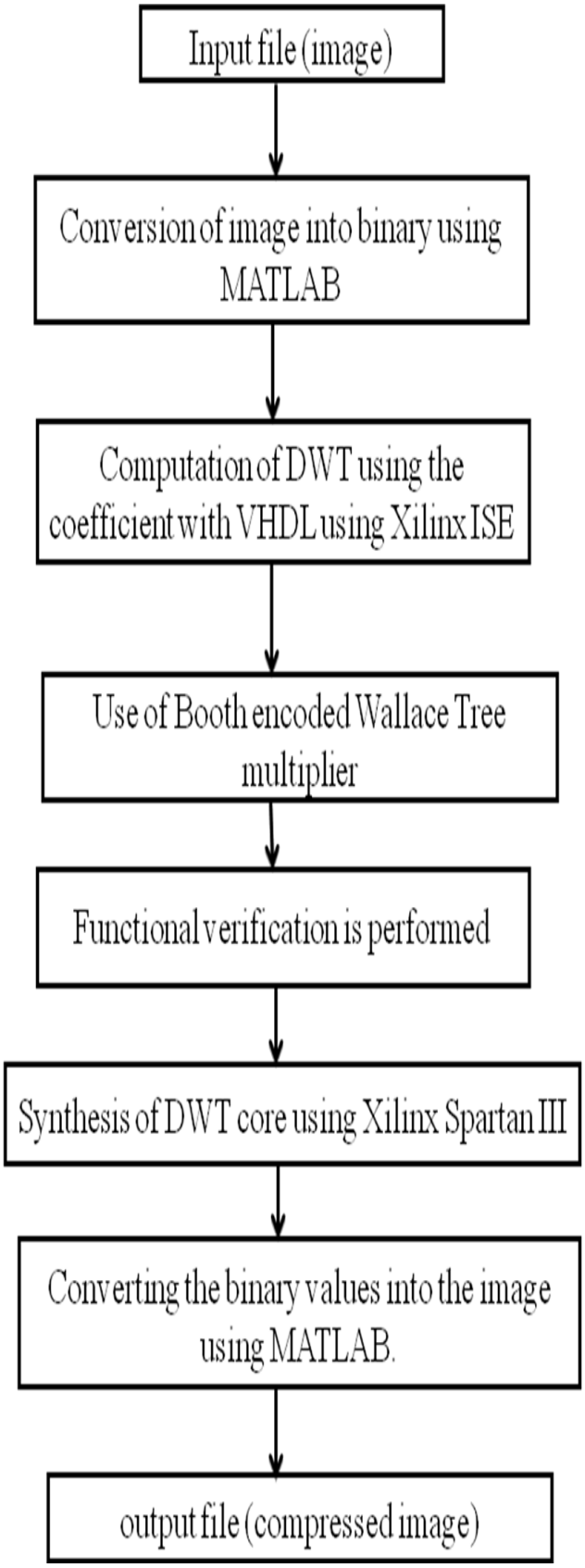


Fig 7.1 Flow chart of proposed scheme

VII. CONCLUSIONS

In this brief, They have first derived the booth encoder then apply that to the Wallace tree multiplier. The DCT is then replaced with the Wavelet transformation. Compared with the existing works the proposed method has provided smaller area and smaller truncation errors. The proposed Booth encoded Wallace tree multiplier in the DWT application has shown the improvement of the PSNR with reduced penalty compared with the existing method.

VIII. FURTURE WORK

In the future work, the wavelet transformations can be replaced with other transformations and langranges multiplier could also be used to improve the compression ratio and PSNR values

REFERENCES

[1]. J. M. Jou, S. R. Kuang, and R. D. Chen, "Design of lower-error fixedwidth multipliers for DSP applications," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process, vol. 46, no. 6, pp. 836–842, Jun. 1999.

[2.] M. J. Schulte and E. E. Swartzlander, Jr., "Truncated multiplication with correction constant," in VLSI Symp. Tech. Dig., 1993, pp. 388–396.

[3.] L. D. Van, S. S. Wang, and W. S. Feng, "Design of the lower-error fixedwidth multiplier and its application," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process, vol. 47, no. 10, pp. 1112–1118, Oct. 2000.

[4.] L. D. Van and C. C. Yang, "Generalized low-error area-efficient fixedwidth multipliers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 8, pp. 1608–1619, Aug. 2005.

[]5.] N. Petra, D. D. Caro, V. Garofalo, E. Napoli, and A. G. M. Strollo, "Truncated binary multipliers with variable correction and minimum mean square error," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 6, pp. 1312–1325, Jun. 2010.

[6.] K. J. Cho, K. C. Lee, J. G. Chung, and K. K. Parhi, "Design of low-error fixed-width modified Booth multiplier," IEEE Trans. Very Large Scale Integr. VLSI) Syst., vol. 12, no. 5, pp. 522–531, May 2004.

[7.]T. B. Juang and S. F. Hsiao, "Low-error carry-free fixed-width multipliers with low-cost compensation circuits," IEEE Trans. Circuits Syst. II, Exp.Briefs, vol. 52, no. 6, pp. 299–303, Jun. 2005.

[8.] K. K. Parhi, J. G. Chung, K. C. Lee, and K. J. Cho, "Low-error fixed-width modified Booth multiplier," U.S. Patent 7 334 200, Feb. 19, 2008.

[9.] M. A. Song, L. D. Van, and S. Y. Kuo, "Adaptive low-error fixed-width Booth multipliers," IEICE Trans. Fundam., vol. E90-A, no. 6, pp. 1180– 1187, Jun. 2007.

[10.] J. P. Wang, S. R. Kuang, and S. C. Liang, "High-accuracy fixedwidth modified Booth multipliers for lossy applications," IEEE Trans. Very Large Scale Integer. (VLSI) Syst., vol. 19, no. 1, pp. 52–60, Jan. 2011.

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