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Area and Delay Minimization of OFDM Transceiver for Various Wireless Applications

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Abstract: **This paper present area and delay minimization of Orthogonal Frequency Division Multiplexing (OFDM) transceiver for various wireless applications. The OFDM can adopt the several sub modules. In this sub modules Inverse Fast Fourier Transform (IFFT) and Fast Fourier Transform (FFT) are occupy the huge area compare to other module. The IFFT/FFT processor is used to change signal from one domain to another domain. In this IFFT/FFT design the twiddle factor co-efficient storage is the major problem and also consumes more area. This OFDM structural design uses a proposed IFFT/FFT processor. In this processor word length multipliers are replaced by Bit Parallel Multipliers (BPM). This OFDM transceiver to minimize the area and delay compared to previous work.**

Index Terms – FFT, IFFT, OFDM, RCCM, BPM

I. INTRODUCTION

The rapid growth of digital communication in recent year, the need for high speed data transmission has been increased. The mobile telecommunication industry faces the problem of providing the technology that is able to support a mixture of services ranging from voice communication to wireless multimedia. This mixture of service ranging provide by OFDM system, it introduce in the 1960's.

There are several methods to implement the OFDM system. As like Application Specific Integrated Circuit (ASIC), Microprocessor or Microcontroller and DSP processor. In this method has some problem as like inflexibility and consume more power. The aim of this work to show the compatibility of designing a OFDM transceiver in Very Large Scale Integration (VLSI) techniques.

In this OFDM design Discrete Fourier Transform is essential for transforming signal from time domain to frequency domain. However, this DFT has computational complexity and time complexity of O (N^2). [1] Cooley and Tukey proposed the Fast Fourier Transform to reduce the computation complexity and time complexity to O ($Nlog_2 N$), where N denotes the FFT size.

The several hardware implementation of FFT processor have processed [2] to [8]. This hardware implementation further classified into memory based and pipeline architecture. This pipeline FFT architecture uses the

Single-path Delay Feedback (SDF) and Multipath Delay Commutator (MDC). Compare to MDC, [7] SDF is require less memory space and only N-1 delay element to be needed. These designs are advantageous to low power, particularly for handheld equipment (DSP) devices. Because the SDF pipeline FFT is adopted in this work.

However, the FFT computation to needs to multiply the different twiddle factors in input signal. These twiddle factors to be store in a large size Read Only Memory (ROM). Therefore, to replace this ROM's for area efficient consideration [4] proposed an efficient ROM less FFT/IFFT processor. The complex multipliers ROM's are replaced by add and shift operations. In order to replace the ROM's to reduce the power consumption and area.

. In this IFFT/FFT processor are implemented into the OFDM transceiver. This propose OFDM transceiver contain a mapping unit, parallel to serial, serial to parallel converter unit. This proposed design to consume a low area and delay.

II. OFDM SYSTEM MODEL

The basic design methodology to implement the OFDM transceiver is the divide and conquer scheme in which first OFDM transceiver is divide into two main parts: OFDM transmitter and receiver.

A. OFDM Transmitter model

Fig.1 shows the OFDM transmitter the generation of OFDM signal started from amplitude modulation mapping module. This mapping module used is BPSK type of modulation.

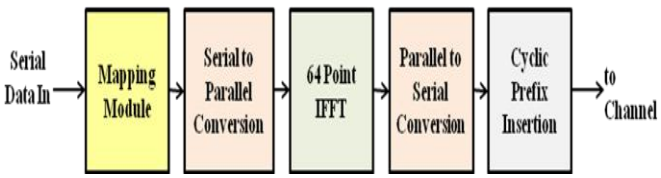

Fig. 1 OFDM transmitter

BPSK is used because module is much easier to design compared to QPSK or other modulation method. The serial input data is mapped to appropriate symbol to represent the data bits. These symbols are in serial and need to convert into parallel format since IFFT module requires parallel input to process data. The serial to parallel module does the conversion. These parallel symbols are transformed from frequency domain into time domain using IFFT module. These signals are converted into serial format and add a cyclic

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prefix to data frame before being transmitted. In this cyclic prefix insertion not be included into the design.

B.OFDM Receiver model

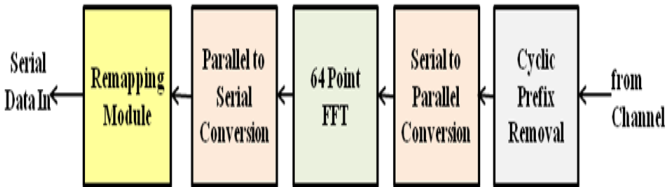

Fig.2 OFDM receiver

Fig.2 shows the OFDM receiver. There are five modules in the receiver block; cyclic prefix removal will not be included into the design. The received data is in serial format, thus since FFT input is in parallel to serial converter. The conversion is required since the serial data need to be transmitted. Finally the serial output is demodulated using remapping module to get the transmitted data.

III. PROPOSED IFFT/FFT PROCESSOR

The OFDM transceiver, IFFT/FFT module is a major part. It occupies the major area and power consumption. In this FFT design using a radix-2 Decimation in Frequency (DIF) signal flow graph as shown in Fig. 3

The below signal flow graph is split into 3 processing elements and also have a complex multipliers required. So it is hardware implementation, because some multiplication can be simplified to reduce the chip area (11)

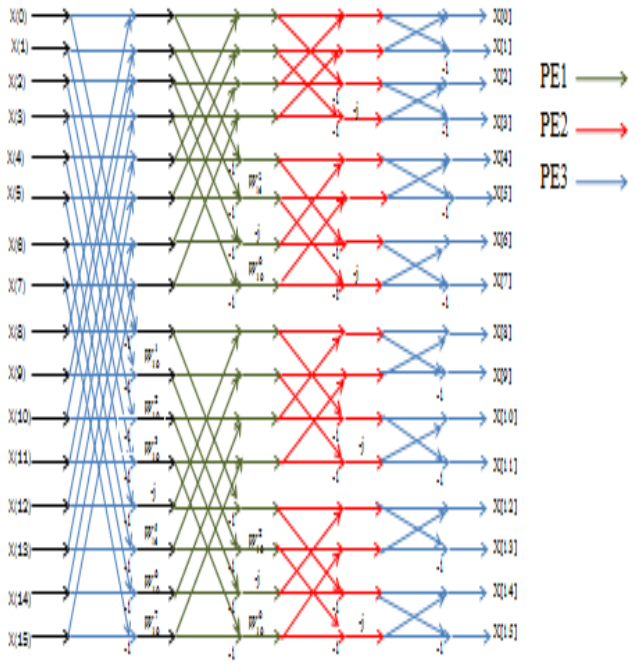

Fig.3 Radix-2 DIF FFT signal flow graph of length 16

Hardware implementation of FFT/IFFT processor usually employs a Read Only Memory (ROM) to look up the wanted twiddle factor; this ROM is consuming more power and area. In order to eliminate the ROM's to introduce a new complex multiplier circuit it contains a Bit Parallel Multiplier [11] to improve the forgoing issues.

In this new proposed radix-2 64 point pipeline FFT/IFFT Processor with low power consumption and reduce delay. This propose architecture as shown in Fig. 4

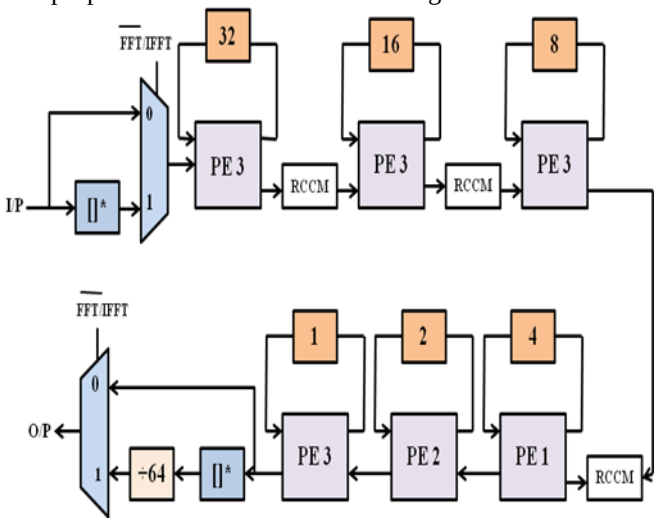

Fig.4 Propose radix-2 64 point pipeline FFT/IFFT processor.

This architecture contains the 3 processing elements PE1, PE2 and PE3 (11), a Reconfigurable Complex Constant Multipliers (RCCMs) and Delay Line (DL) buffer. This architecture the conjugate processor is easy to implement, which only take two's complement of the imaginary part of a complex value. The divide by 64 modules can be substituted with barrel shifter. The Fig.4 RCCM to eliminate the twiddle factor ROM. This RCCM has complex multiplier unit. The proposed complex multiplier to reduce the power, delay and chip area of the Existing unit.

A. Reconfigurable Complex Constant Multipliers (RCCM)

The RCCM are used to multiply the twiddle factor value W_N^i. The twiddle factor value becomes constant as shown in table 1.

Table.1 Twiddle factor value

Coefficient	Value	Coefficient	Value
i1	0.7071	q1	0.7071
i2	0.7730	q2	0.6343
i3	0.8314	q3	0.5555
i4	0.8819	q4	0.4713
i5	0.9238	q5	0.3826
i6	0.9569	q6	0.2902
i7	0.9807	q7	0.1950
i8	0.9951	q8	0.0980

Besides, the twiddle factors have a symmetric property, the complex multiplication used in FFT computation can be followed by five operation types.

$$Type\ 1: W_N^k(a+jb) = W_N^{k-(N/4)}(b-ja) \quad \frac{N}{4} < k \le \frac{N}{2} \quad (6)$$

$$Type\ 2: W_N^k(a+jb) = -W_N^{k-(N/2)}(a+bj) \quad \frac{N}{2} < k < \frac{3N}{4} \quad (7)$$

$$Type\ 3: W_N^k(a+jb) = -W_N^{k-(3N/2)}(b-ja) \quad \frac{3N}{4} < k < N \quad (8)$$

$$Type\ 4: W_N^k(a+jb) = \left[W_N^{(N/4)-k}(b+ja)\right]^* \quad 1 \le k < \frac{N}{4} \quad (9)$$

$$Type\ 5: W_N^k(a+jb) = -j\left[W_N^{(N/2)-k}(b+ja)\right]^* \quad \frac{N}{4} < k < \frac{N}{2} \quad (10)$$

Based on the five operation types, the 49 complex multiplications after the third butterfly stage for 64 point FFT will be reduced to the computation of 16 primary elements. This primary element as shown in Table.1

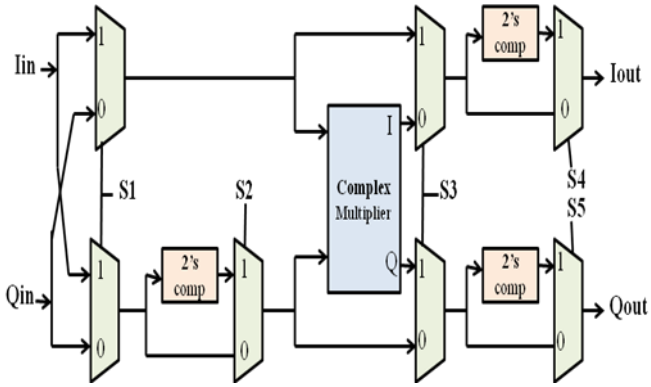

Fig.5 Proposed RCCM

This structure of the complex multiplier also adapts to cascaded scheme achieve the low cost hardware. Here In this structure two input signals (Iin and Qin) and two output signals (Iout and Qout), the pair of both inputs and outputs are real and imaginary part.

The RCCM contain the complex multiplier, this complex constant multiplier circuit diagram as shown in Fig. 8. The complex constant multiplier, constant value becomes a Bit Parallel multiplier. This proposed complex constant multiplier reduces the delay, power and area.

B. Bit Parallel Multipliers (BPM)

The multiplication by the all constant value twiddle factor value can employ a bit parallel operation in terms of power of 2 is given by.

$$output = input \times \frac{\sqrt{2}}{2}$$
$$= input \times (2^{-1} + 2^{-3} + 2^{-4} + 2^{-6} + 2^{-8} + 2^{-14}) \quad (11)$$

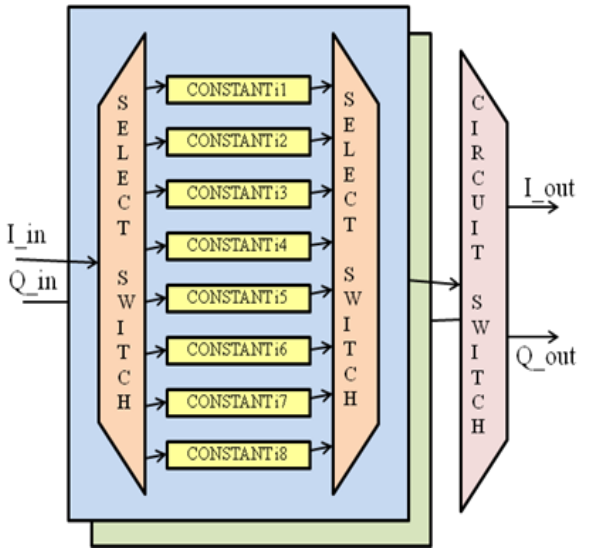

Fig. 6 Circuit diagram for the proposed complex multiplier

If a straightforward implementation for the eqn (11) is adopted, it will introduce a poor accuracy due to the truncation error, and will spend more hardware cost. Therefore to improve the accuracy and hardware cost eqn (11) can be rewritten as

$$output = input \times \frac{\sqrt{2}}{2}$$
$$= input \times [1 + (1 + 2^{-2})(2^{-6} - 2^{-2})] \quad (12)$$

According the above eqn (12), the circuit diagram of the bit parallel multiplier is shown in Fig. 9

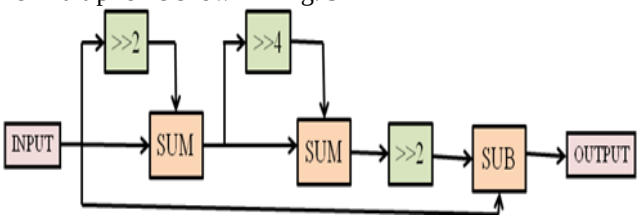

Fig. 7 Circuit diagram for the proposed BPM

This circuit contains the two additions, one subtraction and three parallel shift operations. This BPM is multiplication of 0.7071($1/\sqrt{2}$) constant value, other constant value is used this type of BPM.

IV. SIMULATION AND RESULTS

The functional simulation of the proposed architecture has been justified by using Verilog HDL. The proposed architecture is verified by the XILINX ISE software. To further validate the proposed architecture in MODELSIM software.

The performance evaluation of OFDM transceiver is summarized in Table. 2. From this table, gate counts, delay and power consumption of the proposed architecture are lower than the previous works.

Table. 2 Comparison of OFDM transceiver in Various 64-point IFFT/FFT processor

DESIGN	GATE COUNTS	DELAY	POWER
[11]	99,550	63.543ns	203.27mW
PROPOSED	74,516	51.338ns	202.62mW

V. CONCLUSION

Area and delay minimization of OFDM transceiver for various wireless applications has been described in this work. The symmetric property of twiddle factor is exploited in FFT, and reconfigurable complex constant multiplier is designed such that the size of twiddle factor ROM is nullified. This proposes IFFT/FFT processor is implementing to the OFDM transceiver. This result shows the lower hardware cost, less delay, minimum area and low power consumption as well as

highly efficient compare to the existing ones. It can serve as a powerful OFDM transceiver in various wireless applications.

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