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Design and Implementation of Multi Level logic for Digital system

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ABSTRACT

A Multi Logic Memory cell can hold many logic between high and low that's why fuzzy logic is known as multiple logic level, when I was planning for my M. tech. thesis, my plan was to do something in Fuzzy Electronics then I go through many Research paper related to fuzzy logic and I found that some of the fuzzy systems is been developed already and also I understood how does fuzzy flip-flops works.
I propose the designs of a new fuzzy memory cell of four logic levels which can hold Logic 0, Logic 1, Logic 2 & Logic 3 and also propose to design an Interface module between fuzzy memory with Digital (binary) systems, in my thesis I also plan to implement that how one can reduce the no. of wires required to parallel interface with normal memory and how one can increase the speed of simple serial data transfer.

INTRODUCTION

Fuzzy Electronics logic is a form of many-valued logic; it deals with reasoning that is approximate rather than fixed and exact. In contrast with traditional logic theory, where binary sets have two-valued logic: true or false, fuzzy logic variables may have a truth value that ranges in degree between 0 and 1. Fuzzy logic has been extended to handle the concept of partial truth, where the truth value may range between completely true and completely false.

Binary logic system: Digital electronics circuits that have exactly two possible state 0 and 1. There are some simple logic gates which can compute almost everything. Also a special combination of logic gates gives us the Flip flops for storage of the data.'0' and '1' are logical concept of two possible conditions (high & low); for physical presentation of these, there are some standard logic families like TTL, CMOS etc.

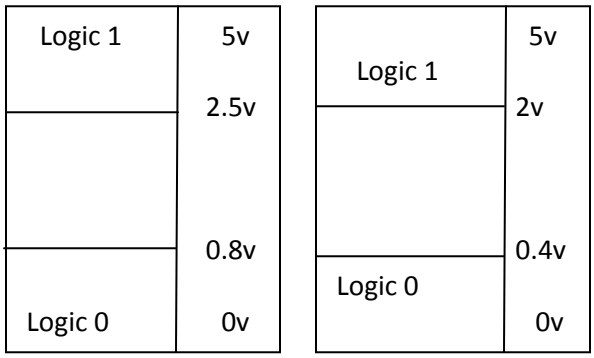


Fig 1: TTL Input / Output high ('1') and Low ('0') Logic

Figure 1 shows the how the logic '1' & '0' exist in the real world, it is in the form of some voltage levels.

Multi Level Logic: Fuzzy logic can hold multiple logic between High and Low, here I proposed a kind of Fuzzy logic which has four logic levels Logic '0', Logic '1', Logic '2' & Logic '3'as shown in Figure 2.

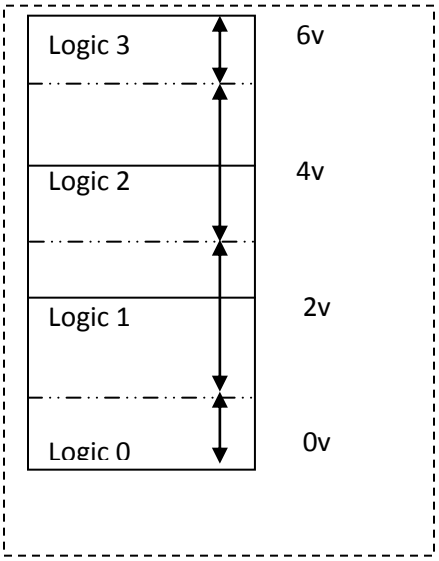


Fig 2: Multi Level Logic

Table 1: The voltage range of our proposed multi level logic

Voltage Range in/out	**Multi level Logic**
0 to 1 v	Logic '0'
1v to 3v	Logic '1'
3v to 5v	Logic '2'
5v to 6v	Logic '3'

Binary Logic V/S Multi Level Logic: Tables 2, 3, 4, 5 shown below to see the difference between basic Digital Logic Gate's & Multi level Fuzzy Logic Gate.

Table 2: Binary AND Gate

Input's		Output
0	0	0
0	1	0
1	0	0
1	1	1

Table 3: Binary OR GATE

Input's		Output
0	0	0
0	1	1
1	0	1
1	1	1

Table 4: Multi Level Fuzzy AND Gate

Input's		output
0	0	0
0	1	0
0	2	0
0	3	0
1	0	0
1	1	1
1	2	1
1	3	1
2	0	0
2	1	1
2	2	2
2	3	2
3	0	0
3	1	1
3	2	2
3	3	3

Table 5:Multi level Logic OR Gate

Input's		output
0	0	0
0	1	1
0	2	2
0	3	3
1	0	1
1	1	1
1	2	2
1	3	3
2	0	2
2	1	2
2	2	2
2	3	3
3	0	3
3	1	3
3	2	3
3	3	3

As we have new logic gate so one can also have multi logic level Flip Flop. A binary flip flop can hold only two logic level whereas Multi Level Fuzzy can hold four logic levels.

As we know a register is a collection of Flip flops and a collection of registers is memory (Static RAM). For storing any decimal value range 0 to 255 we required 8 Flip flops register as shown in the figure 2. It is used by memory for store 8 binary bits (0 or 1).

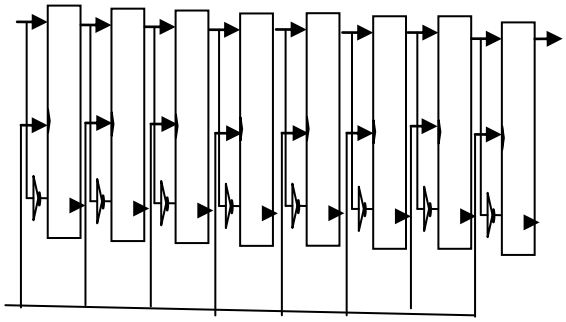


Fig 2: Binary FF based Register for storage of decimal range 0 to 255

But if we use Multi Level Fuzzy Register for storing the decimal value range 0 to 255 we required 4 Multi Level Fuzzy flip flop only as shown in figure 3. Fuzzy memory will use this for storing 4 Multi Level Fuzzy bit (0 or 1 or 2 or 3).

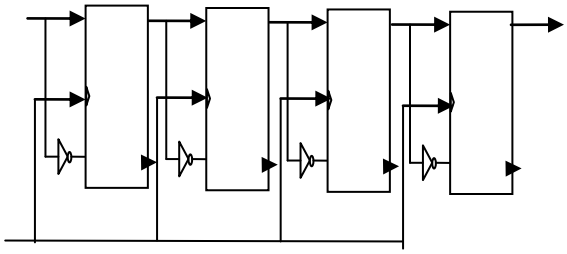
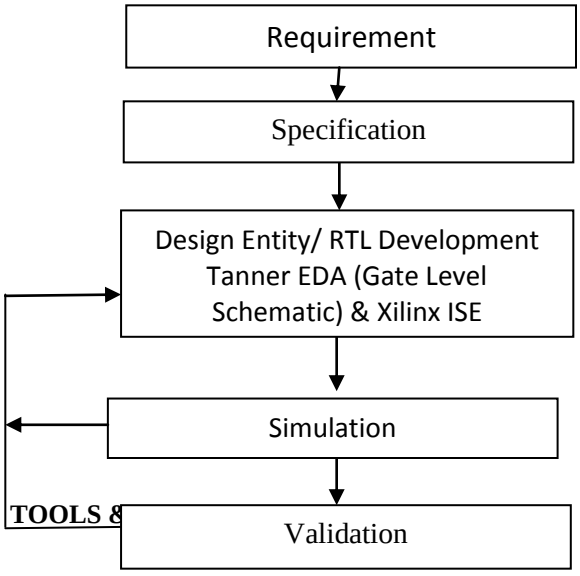


Fig 3: Multi Level Fuzzy Register for storage of decimal range 0 to 255

METHEDOLOGIE

Figure 4 shown below for the design methodology



TOOLS &

Xilinx ISE 9.2i Software: This software supports the Xilinx Integrated Software Environment (ISE).It can also generate bit file so it can program RTL design on FPGA.

Tanner EDA: Tanner EDA provides a complete line of software solutions that catalyze innovation for the design, layout and verification of analog and mixed-signal (A/MS) integrated circuits (ICs).

Spartan-2 FPGA: For implementing the design

Spartan-2 XC2S30
Family- Spartan-2
Device- XC2S30
Pakage-PQ208

RESULTS

Figure 5 shown below is the schematic design of multi level logic AND gate designed by S edit Tanner T-spice pro v6.02

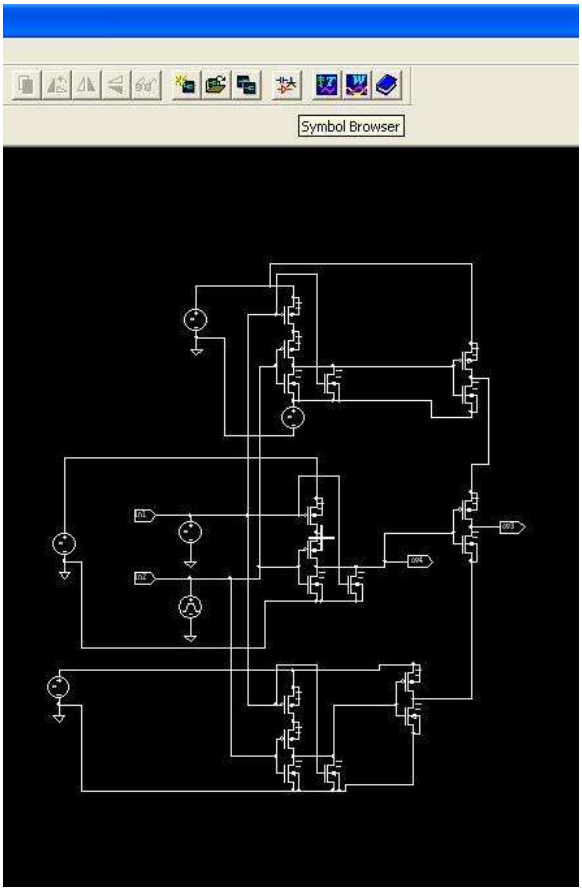


Figure 5: Multi level AND logic gate

Figure 6 is the simulation result observed using Tanner tool for the schematic shown in the figure 4.

Figure 7 is the schematic design of multi level logic OR gate designed by S edit Tanner T-spice pro v6.02

Figure 8 is the simulation result observed using Tanner tool for the schematic shown in the figure 5.

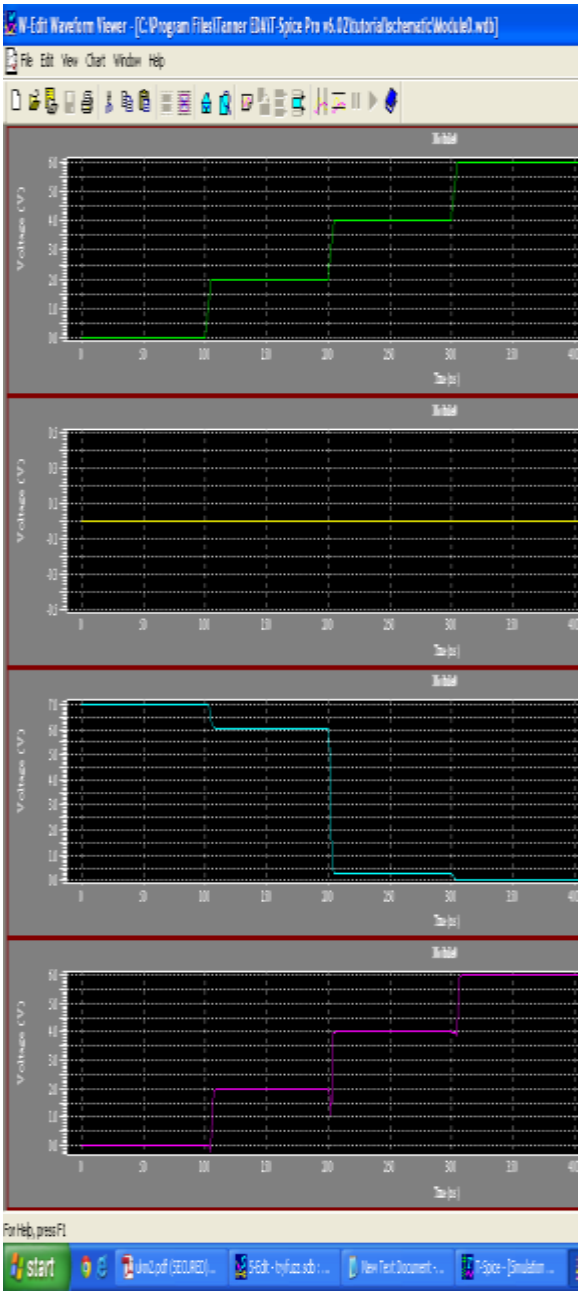


Figure 6 Simulation of Multi level AND Logic

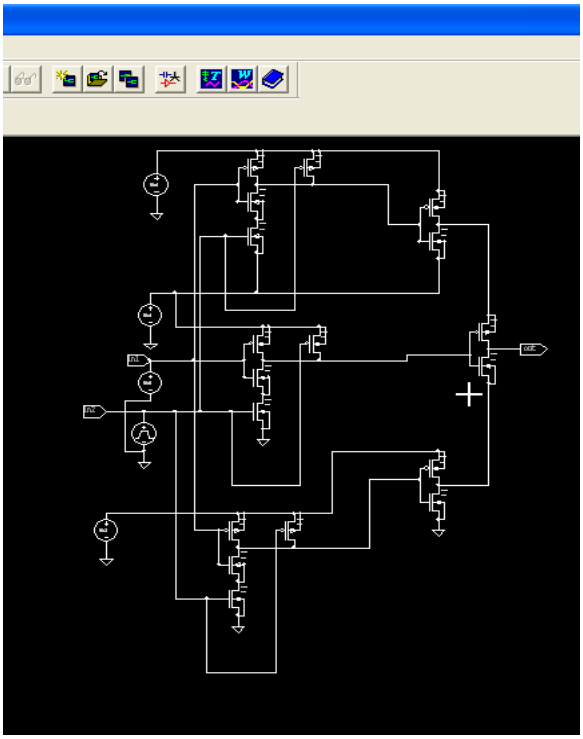


Figure 7 Multi Level OR Logic gate

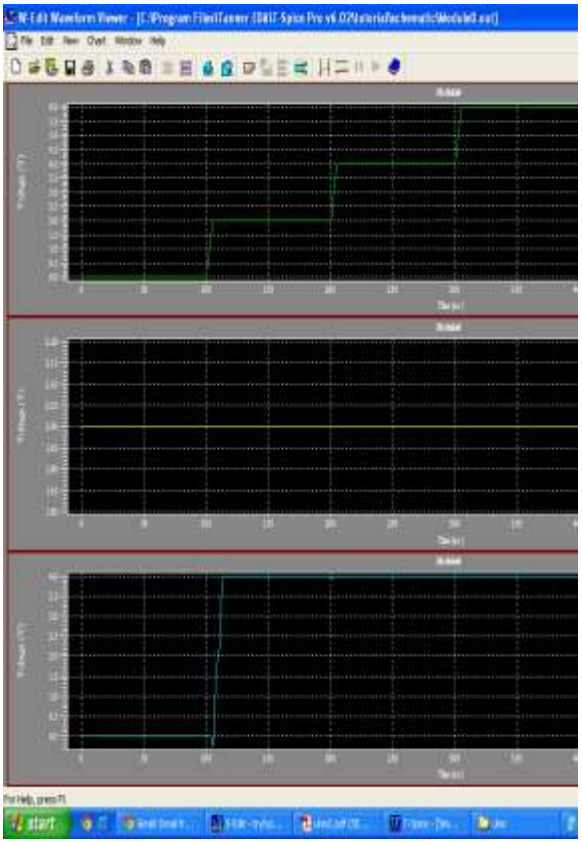


Figure 8 Simulation of multi level OR Gate

It is been verified correctly and we observed as expected but there is only problem of noise margin this logic provides noise margin of 0.7 v.

CONCLUSION

In here, we concentrated on digital approach, which results in multi-valued logic gates. We slightly modified existent designs of the many valued AND gate and OR gate in an attempt to test them using discrete components However, using of the-shelf discrete components, the test results do not produce ideal outputs. Thus, future research may focus on the improvement on the realization of many-valued logic gates as well as the improvement on the realization of truly multi-valued logic gates. The next stage for future research will be to use these multi-valued logic gates and multi -valued logic flip-flop to design large scale sequential multi-valued logic circuits and to implement multi -valued logic systems.

5. Reference:

[1] Baturone, I; Barriga, A; Sanchez-Solano, S; Lopez, D.R;"Microelectronic Design of Fuzzy Logic-Based Systems", CRC Press, ISBN 0-8493-0091-6, 2000.
[2] Leslaw, G.; Kluska, J.; "Family of fuzzy J-K flip-flops based on bounded product, bounded sum and complementation" IEEE Transactions on Systems, Man, and Cybernetics, Part B: Cybernetics, vol. 28, n 6, Dec, 1998, p 861-868.
[3] Marinos, P; "Fuzzy logic and its application to switching systems" IEEE Transactions on Computing, vol. C-18, no.4, p 343-348, Apr 1969.
[4] McLeod, D.; Pedrycz, W.; Diamond, J.; "Fuzzy JK flipflops as computational structures: design and implementation" IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 41, n 3, Mar, 1994, p 215-226.
[5] Mendel, J.M.; "Fuzzy Logic Systems for Engineering: A Tutorial" Proceedings of IEEE, vol. 83, No.3, March 1995.
[6] Miki, T; Yamakawa, T; "Fuzzy Inference on an Analog Fuzzy Chip," IEEE Micro, pp. 8-18, 1995.
[7] New Components for Building Fuzzy Logic Circuits,Ben Choi & Kunal Tipnis,Computer Science & Electrical Engineering, Louisiana Tech University, LA 71272, USA
[8] Simulink; "Simulink: Simulation and Model Based Design" version 6, The Mathworks, 2005.
[9] Zadeh, L.A.; "Fuzzy Logic = Computing with words" IEEE Transactions on Fuzzy Systems, vol.4, p 103-11, 1996.