ISSN: 2278 – 7798
International Journal of Science, Engineering and Technology Research (IJSETR)
Volume 2, Issue 5, May 2013

ECONOMICAL SCAN-BIST VLSI CIRCUITS BASED ON REDUCING TESTING TIME BY MEANS OF ADP

P. Pattunarajam[*], G. NaveenBalaji[#]

[*]*ECE Department, Madha Engineering College*
[#]*Student, Madha Engineering College*
Chennai

Abstract— **Test power reduction done by Arbitrary Density Patterns (ADP) in which the effective usage of the WRP and TDP under adaptive control of clock is used. Weighted random patterns (WRP) and transition density patterns (TDP) can be effectively deployed to reduce test length with higher fault coverage in scan-BIST circuits. New test pattern generator is designed to generate weighted random patterns and controlled transition density patterns to facilitate efficient scan-BIST implementations. We achieve reduction in test time without sacrificing fault coverage while maintaining test power constrain by dynamically adapting the scan clock, accomplished by a built-in hardware monitor of transition density in the scan register.**

***Keywords*— ADP, TDP, WRP, BIST, inactivity monitor**

I. Introduction

With the increase in size, the number of test vectors required to test them has also increased. The time taken to test a chip is the product of the number of test vectors applied and the time required to apply each vector. As the number of test vectors increases, the time required to apply them also increases. Since expensive ATE is used to test these chips, the cost per chip increases with increase in test time. There is therefore growing concern about the time required to apply these test vectors.Due to advancement of technology circuit size has increased which naturally claims longer test time. On the other hand, the test process causes higher power dissipation in the circuits compared to the power dissipated in the normal mode of the circuit. The excess power dissipation gives rise to many problems like hot spots, chip failure, performance degradation and hence testing may even dramatically shorten the battery life when on-line testing is involved.

Complete scan design is a common design for testability (DFT) method in which flip-flops in the circuit are connected together such that input vectors are shifted in and circuit responses shifted out serially through the so-called scan chains. The flip-flops serve as points of controllability and observability, thus increasing the fault coverage.

ADP consists of WRP and TDP. Weighted random patterns (WRP) have been used before to reduce test length for combinational circuits. Proper selection of the input probability can increase the efficiency of test vectors in detecting faults, resulting in reduced test time. Therefore, to achieve higher fault coverage with shorter test lengths weighted pseudo random patterns are used.

Transition density patterns (TDP) are primarily used for reducing power consumption during test. Transition density for a signal or a circuit was originally defined for estimating the dynamic power as the number of signal transitions per unit time.

II. Objective

Analyse the effect of ADP on fault coverage. (Arbitrary density pattern = Weighted random pattern +Arbitrary density pattern). Deploy an effective test generation process using the information from the analysis.Adapt the scan frequency to the transition density for power constrained testing.

Construction of new test pattern generator with the capability of producing ADP have to be done . Adjust the scan frequency according to the transition density for a scan-BIST circuit to speed up the test in multiple scan chains.Deployment of a variable transition density test pattern generator in a BIST circuit that is capable of producing pre-selected transition density vectors.Reduction of test application time further by adapting the scan clock to the pre-selected transition density.

III. Background

A. Scan Design

Sequential circuits are harder to test than combinational circuits. This is because the presence of memory elements, as shown in Figure 1, which creates internal states during circuit operation. An exhaustive test would involve application of all possible input vectors at all possible states of the memory elements.

For a circuit with n inputs there are 2n possible input combinations. As n increases the number of possible input vectors increases exponentially. This phenomenon is even more severe for sequential circuits. The DFT technique that seeks to improve testability of sequential circuits is scan design or its partial scan variations. Here the sequential circuit is modified such that it can operate in test mode. When the circuit is in test mode, the flip-flops in the circuit are chained together to form one or more shift registers. The flip-flops serve as a point of controllability and observability and help achieve better test coverage.

All Rights Reserved © 2013 IJSETR

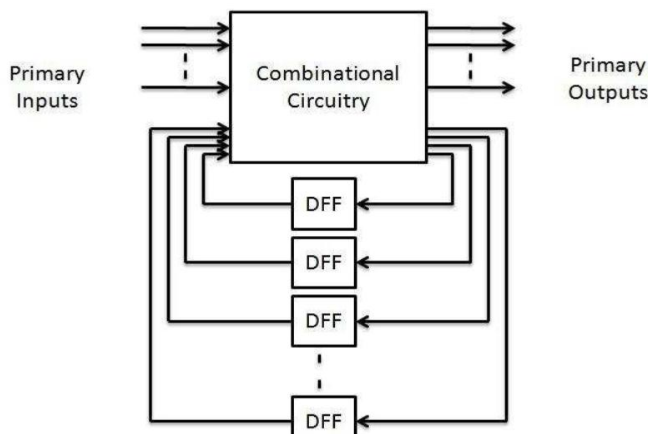

Fig 1 Architecture of a sequential circuit.

B. *Built-In Self-Test (BIST)*

BIST is a DFT technique in which additional hardware is added to the circuit to be tested so that it can test itself. The basic BIST circuitry is shown in Figure 2. Among them, the use of a Linear Feedback Shift Register (LFSR) that generates pseudorandom pattern sets is most common.

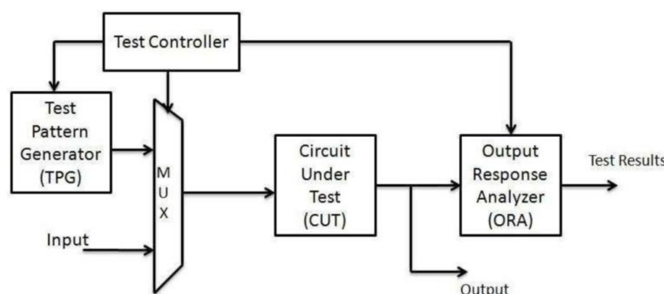

Fig. 2 Basic BIST circuitry.

A large number of outputs are received from the circuit under test. It is necessary to store the correct values of all those bits without adding a lot of extra hardware. This in turn calls for some more design techniques. A LFSR, most commonly known as Signature Analysis Register (SAR) or Multiple Input Signature Register (MISR) is used for this purpose. .

1) *Test-Per-Clock BIST Systems:* In this type of system, a test is applied every clock cycle. This type of system has short pattern lengths. A major concern for BIST is the simulation time required to compute good circuit behavior. It is therefore advantageous to have short pattern lengths".

2) *Test-Per-Scan BIST Systems:* In test-per-scan BIST, each test comprises scan-in of one input vector, one clock to conduct the test and scan-out of output responses.

As the size of the circuit increases, test complexity also increases. Their internal nodes become harder to test. Circuits are therefore modified so that they can be tested effectively.

IV. LITERATURE SURVEY

Several techniques have been used to reduce the power and testing time during testing of VLSI circuits. Reducing these parameters will contribute to the low cost of the circuits. Numerous techniques have been used in the past to reduce the test power and the test application time [9]. The assessment in the field of reducing the test power was performed.

First, an experimental method for generating large-scale integration (LSI) test patterns with weighted random pattern is analysed. In precise, this method presents a technique for generating random pattern sequences to test complex logic circuits [20]. Here path sensitizing technique is used between inputs and outputs. Fault-oriented and path-oriented path sensitizations were performed. In its primary phase, purely random patterns were measured. At later stages, some intelligence was introduced by assigning weights to the primary inputs in proportion to their relative importance. The main disadvantage of this concept was high fault coverage was attained only for small circuits.

LFSR (Linear Feedback Shift Register) is used to generate pseudo-random patterns [19]. Exhaustive testing uses all possible combinations of inputs and estimate the cost of all patterns were calculated .This takes either a day, week or even a lifetime to test. Next technique was to convert the test patterns into weight sets [18]. The deterministic test sets was less appropriate for weight generation. Two main reasons for difficult generation of test patterns were the test sets may contain redundant information and they may contain differing information. Differing information mainly contributes to a larger hamming distance. Several conflicts in weight assignment for the input patterns will arise [18]. Best Primary Input Change (BPIC) technique increases the correlation between successive states but it is not suitable for System on chip (SOC) [14].

V. TRANSITION DENSITY AND ITS EFFECTS

A. *Weighted Random Pattern*

Weighted random patterns (WRP) in which the probability of 1, p1, instead of being 0.5, can be set to any value in the range [0, 1] have certain advantages. Recent papers discuss low power test using weighted random and other reduced activity patterns. The power dissipation of scan patterns is related to the transitions they produce in the scan register. It is reported that with reduced activity patterns the fault coverage rises slowly and for the same required coverage a larger number of patterns are needed. Thus, a reduced power test may take longer time. The primary purpose of WRP is to increase the rate of fault detection and reduce the test time. They are also known to reduce power consumption.

B. *Transition density Patterns*

Ratio of no. of transitions to the no. of unit intervals in a serial data stream is in figure 3. Many Serial communication test signals ratio approaches to 0.5.If bits are generated randomly, the probabilities of generating a 1 or a 0 are equal.

All Rights Reserved © 2013 IJSETR

The transition density of the bit stream is also 0.5. To generate a transition density higher or lower than 0.5, bits must be generated with negative or positive correlation, respectively. Therefore, the bit stream will contain shorter runs of consecutive 1s or 0s for a transition density higher than 0.5 and longer runs of consecutive 1s or 0s for a transition density lower than 0.5.

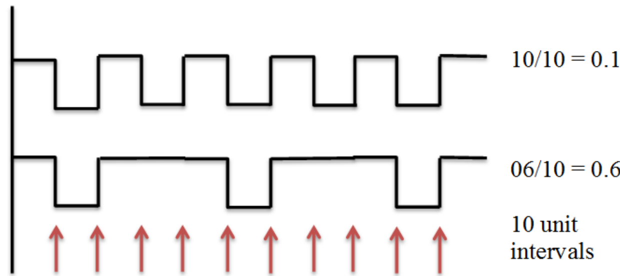

Fig.3 Transition density in a signal line

A Matlab program was written to generate test vector sets, each set containing 10000 vectors but with different transition densities. Here also the transition density was varied from 0.1 to 0.95, with 0.05 intervals. The vector set generated for 0.1 transition density has longer runs of 1s and 0s in consecutive bit positions. Likewise the vector set having transition density of 0.95 has very short runs of 1s and 0s in consecutive bit positions.

If bits are generated randomly, the probabilities of generating a 1 or a 0 are equal, i.e., p0 = p1 = 0.5. Hence the transition density of the bit stream is also 0.5.

To generate a transition density higher or lower than 0.5, bits must be generated with negative or positive correlation, respectively. Therefore, the bit stream will contain shorter runs of consecutive 1s or 0s for a transition density higher than 0.5 and longer runs of consecutive 1s or 0s for a transition density lower than 0.5.

VI. EXISTING SYSTEM

A. Test Pattern Generator

Weighted random patterns have been used before to reduce test length for combinational circuits. Proper selection of the input probability can increase the efficiency of test vectors in detecting faults, resulting in reduced test time. Therefore, to achieve higher fault coverage with shorter test lengths weighted pseudo random patterns are used.

Weighted random patterns (WRP) in which the probability of 1, p1, instead of being 0.5, can be set to any value in the range [0, 1] have certain advantages. The figure 4 contains a 28-bit external linear feedback shift register (LFSR) using the polynomial $p(x) = x^{28}+x^{3}+1$.

The Scan Bit Generator block consists of AND gates, inverters, an 8-to-1 MUX to select from eight different probabilities of a bit being 1, and a toggle flip-flop.

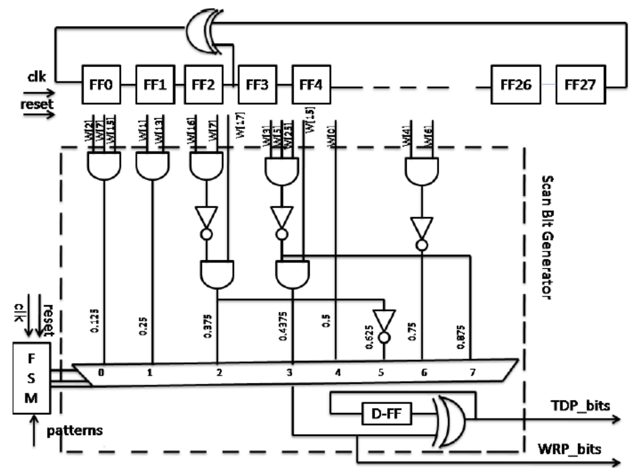

Fig.4 Test pattern generator (TPG) of a 28bit LFSR

A simple Finite State Machine provides the select inputs to the MUX. The Scan Bit Generator produces eight different weighted random bit sequences.The weights are constructed by AND-ing two or more outputs from non-adjacent cells of the LFSR.

B. Dynamic Control of Scan Clock in a BIST Circuit

The circuit model chosen for the analysis is the test-per-scan multiple scan chain based BIST model. To implement this model, flip-flops are added to primary inputs and primary outputs of the sequential circuit under test (CUT).

All flip-flops are converted into scan flip-flops and partitioned into multiple scan chains. A test pattern generator (TPG), a multiple input signature register (MISR) and a BIST controller are also added. Afrequency divider module is added, which provides either the scan clock or the system clock, based on the mode of operation of the circuit. If the circuit is in the system mode, the BIST circuitry that consists of TPG, MISR and BIST controller are kept idle and the circuit runs with the system clock provided by the control clock select block.

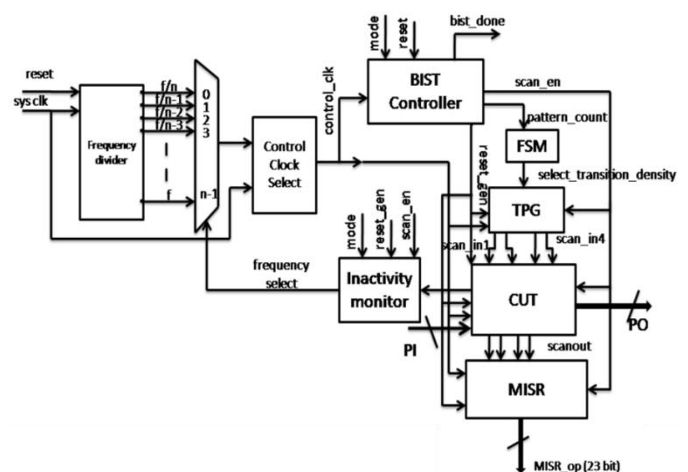

Fig.5 Dynamic scan clock scheme with TPG

Likewise if the circuit is in test mode then the BIST circuitry is active and the control clock selects the scan clock.

All Rights Reserved © 2013 IJSETR

Here the frequency of the scan clock is determined by the peak power consumption of the circuit.

A larger frequency divider divides the system clock into n different frequencies, where the fastest clock is the system clock and the slowest frequency is the test clock, based on the peak power consumption as described earlier. An n:1 multiplexer MUX is also added to select from the range of frequencies generated by the frequency divider block.

VII. INACTIVITY MONITOR

The inactivity monitors are simple XNOR gates that produce a 1 whenever inactivity enters the attached scan chain and produces a 0 when an activity enters the scan chain. We feed the output of all monitors to a counter. Depending on the number of lines that are logic 1 at the output of the XNOR gates counter adds from 0 to n (number of scan chains) per clock. Hence all the inactivity that has entered the entire scan chains per clock has been accounted for. If no inactivity enters any of the scan chains, then the counter stays in its previous state by adding 0. If 1 inactivity enters one of the scan chains, the counter counts up by 1, and so on.

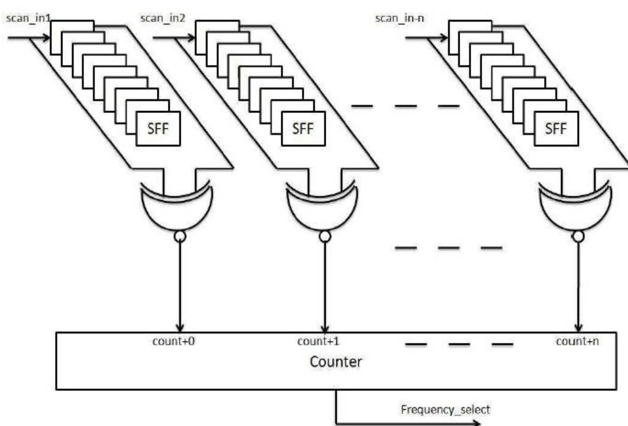

Fig. 6 An inactivity monitor block implementation with monitors attached to the first scan flip-flop of each chain.

Figure 6 shows that the working of the inactivity monitor. Therefore, if inactivity enters every one of the n scan chains, the counter adds n to the previous count. While counting up, if the counter reaches a certain threshold it signals the frequency selector MUX to deploy a higher frequency and hence dynamically adapts the scan frequency according to the inactivity in the chain. The actual hardware consists of an adder, a combinational block with a register and a MUX. At every clock, if a non-activity enters a scan chain, the inactivity monitor attached to the first flip-flop of the scan chain becomes high.The inactivity monitor from every scan chain feeds to a combinational block.

The output of the combinational block is connected to a separate select line of a MUX. The inputs of the MUX are 0, 1, 2... n, where n is the number of scan chains in the design.

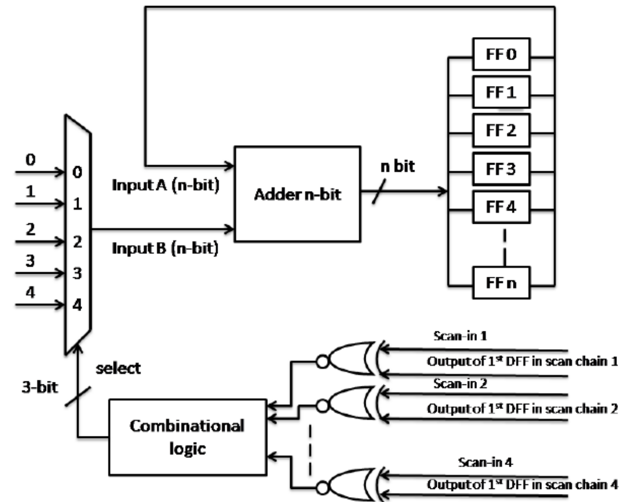

Fig.7 The inactivity monitor - Hardware implementation

The inputs to the adder are the previous state of the register and the output from the MUX. If 1 output of the inactivity monitor is high, the output of the combinational block will be 01 (assuming the number of scan chains in the design to be 4). The first input to the adder is the present state of the register and the second input to adder is the output to the mux. For our example, 1 will be added to the current contents of the register. Hence, at every clock the contents of the register will be updated according to the number of inactivity that entered the scan chains.

Similarly, If 1 inactivity enters in each of the scan chains, i.e., if the total number of inactivity is 4, then the combinational circuit output will be 11. This in turn will choose the second input of the adder to be 4. Hence, 4 will be added to the current state of the register. However, if no inactivity enters in any of the scan chains, the combinational circuit will produce 00 outputs. Hence, 0 will be added to the current state of the register.

VIII. PROPOSED SYSTEM

This chapter proposes a new method of implementation of the transition density based vector generation by a BIST-TPG. The first section describes the hardware used to implement the pattern generator, the second section estimates the randomness of the generated vectors and the last section describes the implementation of the TPG in the adaptive scan clock scheme described earlier.

A. *BIST-TPG Circuit for Arbitrary Density Patterns*

The test pattern generator (TPG) chosen for the analysis is a 28 bit external LFSR using the polynomial $p(x) = x^{28} + x^3 + 1$.

The combinational part consists of only AND gates and inverters, an eight input MUX to select from eight different probability of a bit being 1, a simple Finite State Machine (FSM) to control the MUX, and a toggle flip-flop. Figure 7

All Rights Reserved © 2013 IJSETR

ISSN: 2278 – 7798
International Journal of Science, Engineering and Technology Research (IJSETR)
Volume 2, Issue 5, May 2013

shows the circuitry for the test pattern generator. The combinational network generates eight different weighted random bit sequences.

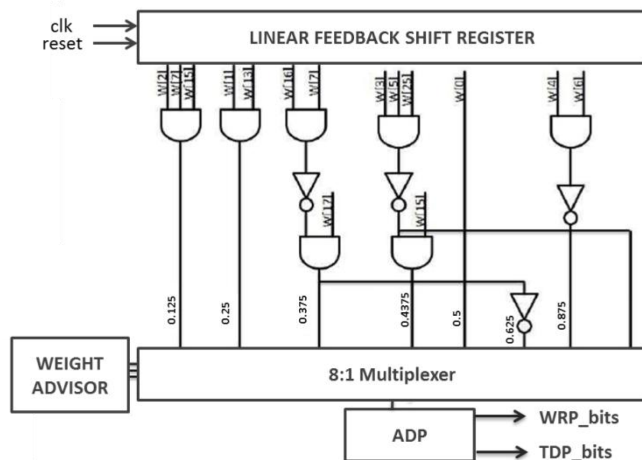

Fig. 8 Block Diagram of TPG.

The weights are constructed by ANDing two or more outputs from non-adjacent cells of the LFSR. Here it is to be noted that two cells in an n-bit LFSR are adjacent if the output of one cell feeds the input of the second directly, without an intervening XOR gate.

As shown in Figure 7.1, eight weights for the probability of a bit being 1 are 0.125, 0.25, 0.375, 0.4375, 0.5, 0.625, 0.75 and 0.875, respectively. The probability of a bit being 1 or 0 at the output of any cell of the TPG is 0.5. This weight is directly fed to one of the inputs of the MUX. Two outputs from two non-adjacent cells were ANDed to produce a weight of 0.25, three outputs from three non-adjacent cells were ANDed to produce a weight of 0.125, and inverting the

For generating weight of 0.375, weight 0.75 is again ANDed with another cell output that is not adjacent to any of those two cells that are used in creating the 0.75 weight. Similarly for generating weight of 0.4375, weight 0.875 is ANDed with another non-adjacent cell output. Finally, to construct a weight of 0.625, weight 0.375 is inverted.se two weights we get weights of 0.75 and 0.875, respectively

A toggle generating flip-flop constructed with a D-flip-flop and an XOR gate is added to produce the required transition density in the vectors that are to be fed to scan chain. Through the select lines of the MUX a weight is selected and the bit sequence fed to one of the inputs of the XOR gate; the other input line of the XOR gate is the output of the D flip-flop. Once a weight is selected, the corresponding bit sequence will then control the transition at the output of the XOR gate.

A 1 in the bit sequence will produce a transition at the output of the XOR gate and a 0 will produce no transition. Thus the resulting transition density in the bit stream at the output of the XOR gate will have the same weight (i.e., the probability of a transition to occur) as the weight selected from the MUX.

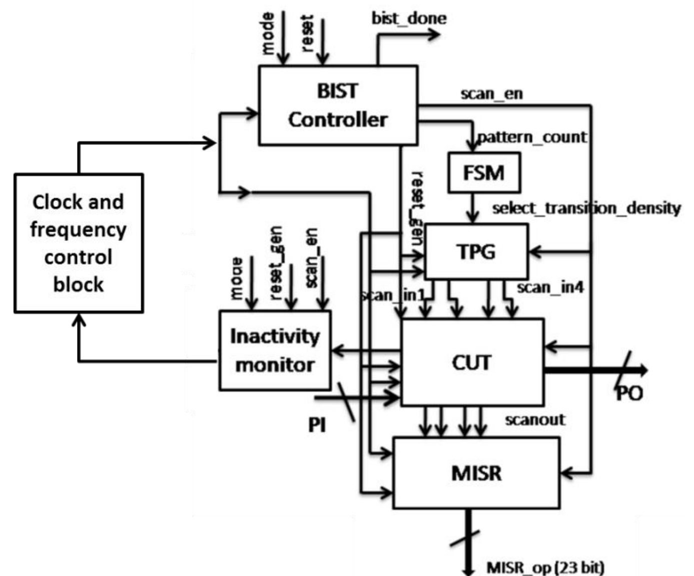

Fig.9 Implementation of one test per scan vector

IX. DESIGN OF SLOTH MONITOR

The sloth monitor is the major unit which is used to measure the circuit activity during scanning. The input bits are taken parallel form to the sloth monitor. The sloth monitor is built by a novel algorithm based approach by avoiding the logic gates as in the existing system.

A. *Novel algorithm for sloth monitor*

Step 1: Start the sloth monitor
Step 2: Initialize the input variables and count
Step 3: Fix the threshold value for the count in the counter
Step 4: Analyze the parallel input bits from the CUT
Step 5: Separate the bits in according to their position
Step 6: Select a starting frequency
Step 7: Check for inactivity in each successive two bits i, j
Step 8: If two bits are equal, increment the count
Step 9: The count once reaches the threshold, the counter resets to 0 and the frequency is increased by value say 10
Step 10: Continue the same process for entire sequence
Step 11: If 2 bits are unequal count and frequency remains the same
Step 12: Check if all bits in the sequence are scanned
Step 13: Stop the program

The sloth monitor is capable of counting the inactivity and after attaining a particular threshold of count, the frequency is increased to a particular extent. The time period is reduced so that it could test the CUT with the faster frequency. Once the frequency is increased the count value in the counter resets to zero. The frequency is selected from the frequency divider and it is given to the clock select block. This block in turn provides the clock to the other blocks.

B. *Working of Sloth monitor*

The counter states at which the clock is sped up and establishes correlation between the circuit activity and scan chain activity. If each transition in the scan chain causes a

All Rights Reserved © 2013 IJSETR

large number of transitions in the circuit, power consumption reaches large values for low scan chain transition numbers. Thus, a large number of scan chain nontransitions should be counted before the scan clock frequency is stepped up. Similarly, if a transition in the scan chain has a small effect on the circuit activity, then only a few nontransitions in the scan chain are sufficient to increase the scan clock frequency.

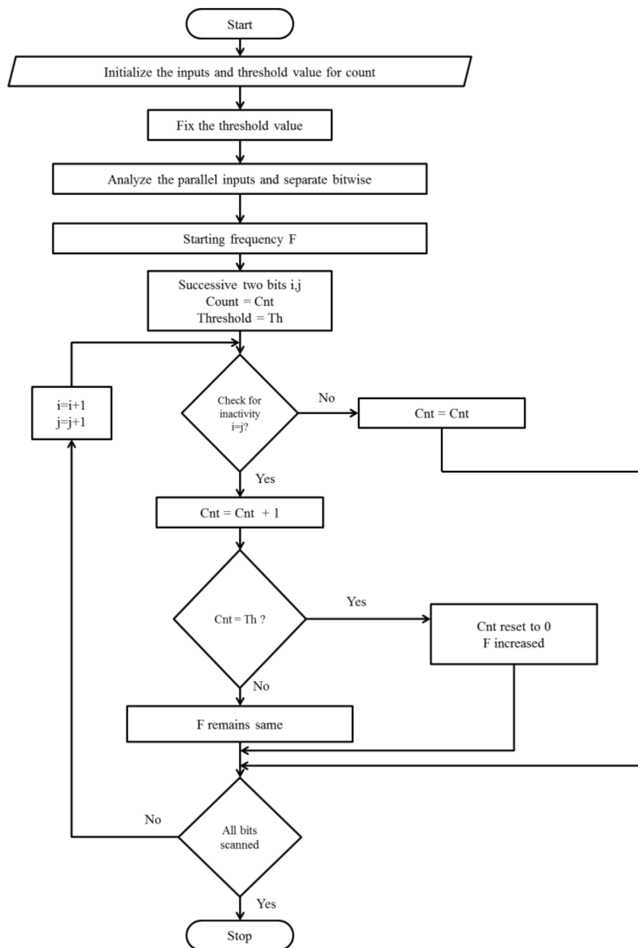

Fig. 10 Flowchart chart for novel algorithm of sloth monitor

Fig. 11 Sloth Monitor output

Clearly, a bit stream with fewer transitions will be scanned in faster than one with many transitions.

X. Modified TPG using Hamming Distance Calculator

A new test pattern generator was designed using ADP (Arbitrary Density Patterns). This ADP uses two types of patterns WRP and TDP.

Weighted random pattern is created by providing the certain weights of probability to the primary inputs of the circuit under test. The weights introduced were useful in giving particular priority to the primary inputs. This type of test patterns if used in testing they reduce the test time by using the probability imparted to the primary inputs.

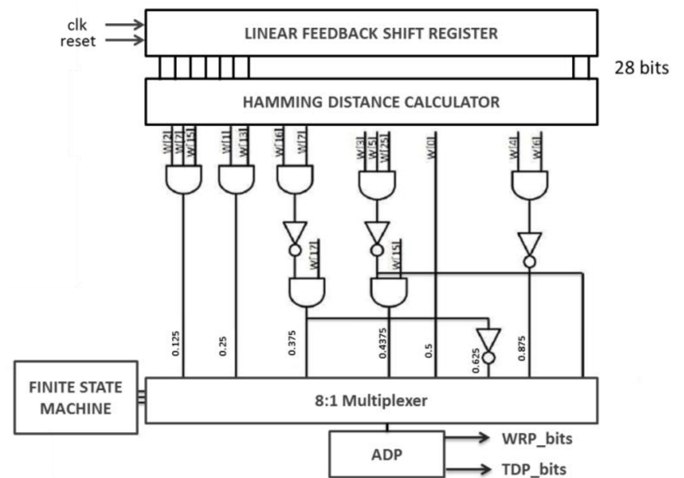

Fig.12 Modified test pattern generator using HDC

The scan bit generator is the main block which creates weights from the LFSR of the desired polynomial value. Older methods use random sequences to create the arbitrary density patterns. Test pattern generator circuit is modified as to increase the correlation between the samples for creating the weight samples. In order to increase the correlation between samples hamming distance calculator is used. Hamming distance calculator is used to select the LFSR bits with minimum hamming distance. By using low hamming distance the correlation increases thereby reduces the switching activity inside the circuit. This will result in reduced testing vectors and the testing time. Hence low power is consumed for the test power.

XI. Results

A. *Circuit parameters*

- Family of FPGA board : Cyclone II
- Device inside FPGA : EP2C5T144c6
- Total logic elements : 393
- Total registers : 174
- Chip size : 31
- Total fan-out : 1511

B. *Power parameters*

- Total thermal power dissipation : 32.62 mW
- Static thermal power dissipation : 18.01 mW
- I/O thermal power dissipation : 14.60 mW

All Rights Reserved © 2013 IJSETR

C. Timing parameters

- Worst case timing : 5.701 ns
- Clock setup : 250.13 MHz
- Period : 3.988 ns
- Total CPU time (all processors) : 00:00:02 s

XII. CONCLUSIONS

For scan testing it is important to note that both power and test time contribute to the test cost as well as quality of the test. This work proposes to strike a balance between these two factors and mainly to reduce test application time as much as possible without sacrificing the fault coverage keeping the test power under control. The lowertransition density based vectors though need more number of vectors but the differencebetween numbers of the vectors needed to detect those faults is small. Thus a lower transitiondensity can be chosen deterministically to reach that partial coverage while speeding up thescan clock without crossing the power budget.

The main ideas forwarded in this project are, transition density can be effectively selected for any circuit similar to weighted random patterns to generate test with shorter TEST LENGTH. Once the transition density is known the test application time can be further reduced by dynamically controlling the test clock keeping the test power controlled.

FUTURE WORK

In the future, more refined methods for obtaining the controlled transition density mixing in the vector set generated from LFSR by using hamming distance calculator or linear programming approach is to be examined simultaneously to reduce the test time and test power more efficiently. Fault coverage for S298 benchmark circuit and the dynamic power for different input test pattern are to be measured.

REFERENCES

[1] Farhana Rashid Vishwani Agrawal (2012) Weighted Random and Transition Density Patterns For Scan-BIST IEEE NATW

[2] Farhana Rashid Vishwani Agrawal (2012) Power Problems in VLSI Circuit Testing VDAT 2012, LNCS 7373, pp. 393–405, Springer-Verlag Berlin Heidelberg 2012

[3] Priyadharshini Shanmugasundaram, Vishwani D. Agrawal (2011) 'Externally Tested Scan Circuit With Built-In Activity Monitor and Adaptive Test Clock', National Science Foundation, Grant CNS-0708962.

[4] Priyadharshini Shanmugasundaram and Vishwani D. Agrawal Auburn University (2011) 'Dynamic Scan Clock Control for Test Time Reduction Maintaining Peak Power Limit' 978-1-61284-656-9/11/2011 IEEE

[5] Sunil Udhvanshi, (2011) 'Design of Low Power and High Fault Coverage Test Pattern Generation for BIST- Built in Self-Test' Thesis, Thapar University

[6] J. Rajski et al., (2011) "Test Generator with Preselected Toggling for Low Power Built-In Self-Test,"in Proc. IEEE 29th VLSI Test Symp.

[7] S. Abu-Issa and S. F. Quigley,(May 2009) "Bit-Swapping LFSR and Scan-Chain Ordering: A Novel Technique for Peak and Average-Power Reduction in Scan-Based BIST," IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, vol. 28, no. 5.

[8] M. Tehranipoor, M. Nourani, and N. Ahmed,(2005) "Low Transition LFSR for BIST-Based Application," in Proc. IEEE 14th Asian Test Symposium.

[9] Girard Patrick (2002), 'Survey of Low-Power Testing of VLSI Circuits' IEEE Design & Test of Computers, IEEE.

[10] S. Wang, (Dec 2002) "Generation of Low Power Dissipation and High Fault Coverage Patterns for Scan- Based BIST," in Proc. International Test Conf., , pp. 834–843

[11] P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, and H. J. Wunderlich, (May 2001) "A Modified Clock Scheme for a Low Power BIST Test Pattern Generator," in Proc. IEEE 19th VLSI Test Symp., , pp. 306–311.

[12] .D. Gizopoulos, N. Krantitis, A. Paschalis, M. Psarakis, and Y. Zorian, (May 2000) "Low Power/Energy BIST Scheme for Datapaths," in Proc. IEEE 18th VLSI Test Symp., , pp. 23–28.

[13] F. Corno, M. Rebaudengo, M. S. Reorda, G. Squillero, and M. Violante, (May 2000) "Low Power BIST via Non-Linear Hybrid Cellular Automata," in Proc. IEEE 18th VLSI Test Symp., , pp. 29–34.

[14] Nicola Nicolici (2000), University of Southampton, 'Power Minimisation Techniques for Testing Low Power VLSI Circuits' Thesis, University of Southampton.

[15] S. Wang and S. K. Gupta, (Sept. 1999) "LT-RTPG: A New Test-Per-Scan BIST TPG for Low Heat Dissipation," in Proc. International Test Conf., , pp. 85–94.

[16] X. Zhang, K. Roy, and S. Bhawmik, (Jan. 1999) "POWERTEST: A Tool for Energy Conscious Weighted Random Pattern Testing," in Proc. 12th International Conf. VLSI Design, , pp. 416–422.

[17] S. Wang and S. K. Gupta, (Nov. 1997) "DS-LFSR: A New BIST TPG for Low Heat Dissipation," in Proc.International Test Conf., , pp. 848–857.

[18] Birgit Reeb (1996) 'Deterministic Pattern Generation for Weighted Random Pattern Testing'0-89791-821/96-IEEE

[19] Eichelberger E. B. and E. Lindbloom (1984) 'Random-Pattern Coverage Enhancement and Diagnosis for LSSD Logic Self-Test', IBM J. Res. Develop. Vol. 27 No. 3.

[20] Daniel. H. Schnurmann, Eric Lindbloom and Robert G. Carpenter (1975) 'The Weighted Random Test-Pattern Generator' IEEE Transactions on Computers, Vol. c-24, No. 7.

TABLE I RESULTS OF SLOTH MONITOR AFTER TESTING THE CUT (S298 BENCHMARK CIRCUIT - 14 FLIP FLOPS) FOR THRESHOLD VALUE OF COUNT 3

PI test pattern	Time period of starting frequency	Time period after scanning the sequence	Time (ns)	System time (s)	Transition count	Nontransitions count
00001111000000	80ns	50ns	860	0.02	2	11
11001100110011	80ns	60ns	940	0.02	6	7
00110011111100	80ns	60ns	920	0.02	4	9
11111111111111	80ns	40ns	820	0.02	0	13
10101010101010	80ns	80ns	1040	0.02	13	0

All Rights Reserved © 2013 IJSETR