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Modified Approach for Harmonic Reduction in Multilevel Inverter

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***Abstract*— This paper analyses a modified approach to reduce harmonics in multilevel inverters. It uses modified Sinusoidal Pulse Width Modulation (SPWM) switching technique and compares the Total Harmonic Distortion (THD) of various modified SPWM sequences to finally obtain the switching sequence that produces minimum harmonics. The simulation is done in SIMULINK/MATLAB software. The THD in the voltages for different sequences is presented**

***Index Terms*— Harmonics, modified Sinusoidal Pulse Width Modulation (SPWM), Total Harmonic Distortion, (THD), multilevel inverter**

I. INTRODUCTION

In any solar or wind setup, an inverter is a key piece of equipment. As the need for decentralization of power production is increasing, inverters enable individual establishments to have a self-sustainable source of power. While modified sine wave inverters cannot be used with highly sensitive electronic equipment, they save energy while running small loads and are also very economical compared to pure sine wave inverters. They also utilize DC more efficiently.

The most attractive features of multilevel inverters as outlined in [1] are as follows.

1. Output voltages have extremely low distortion and low dv/dt.
2. They draw current with very low distortion.
3. They operate with a lower switching frequency.

A popular topology for multilevel inverters is the cascaded multilevel inverter which is based on the series connection of single phase H-bridge inverters with separate dc sources. In this, the output voltage waveform is nearly sinusoidal even without filtering. If the number of single phase inverters is n, then the number of output levels will be (2n+1). Therefore an increase in n will increase the number of levels in the output. But for each added inverter four switching devices will be needed.

In the new topology used in this paper from [2] and [3], the number of switching devices required for the same number of output levels as the cascaded multilevel inverter topology is less.

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An approach to reduce harmonics in the output voltage from this topology using modified SPWM is discussed in this paper.

II. CIRCUIT DESCRIPTION AND WORKING

The multilevel circuit consists of 3 Level Modules (LM), an H-bridge inverter, input DC voltage and RL load as shown. For a 15 level output, the number of switches used in the circuit is 10 as opposed to 28 switches that would be required in the cascaded topology. The Level Module consists of two semiconductor switching devices and a DC source. If the number of level modules is increased, the output voltage levels can be increased.

Number of output levels is given as

$n=2^{(m+1)}-1$

where m is the number of Level Modules used.

The number of switches used in the circuit is

$r=2(m+4)$

The input DC voltage varies as

$Vk=2^{(k-1)}V_d$,

where k=1,2,3,……m

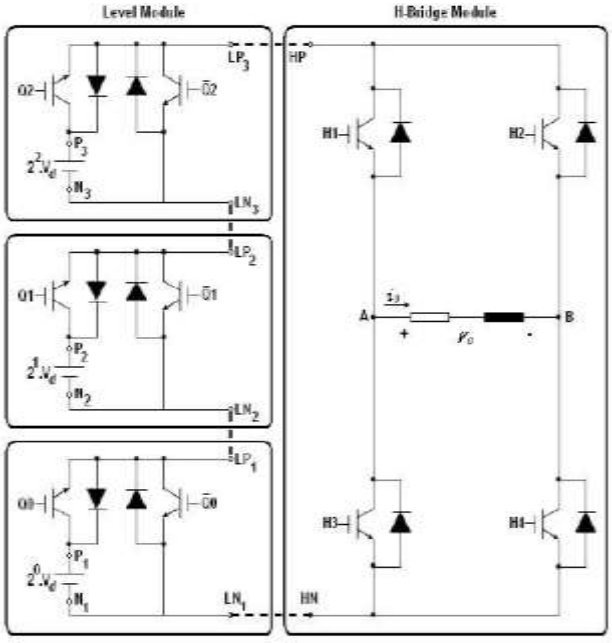

Fig.1. Multilevel inverter circuit

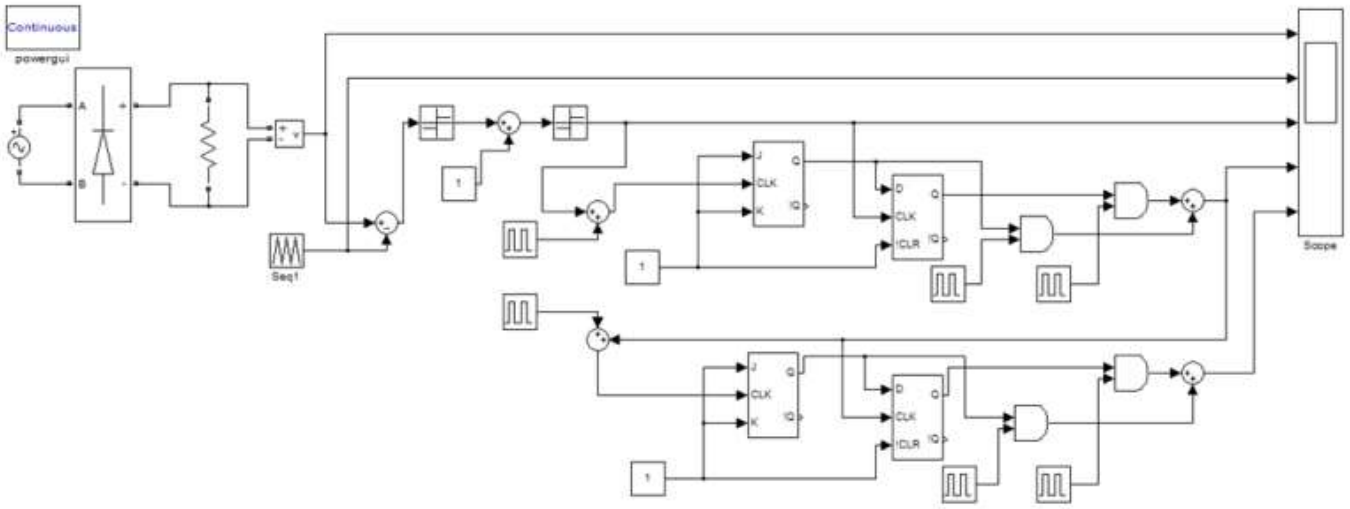

Fig.2. Simulink model for generation of switching signals

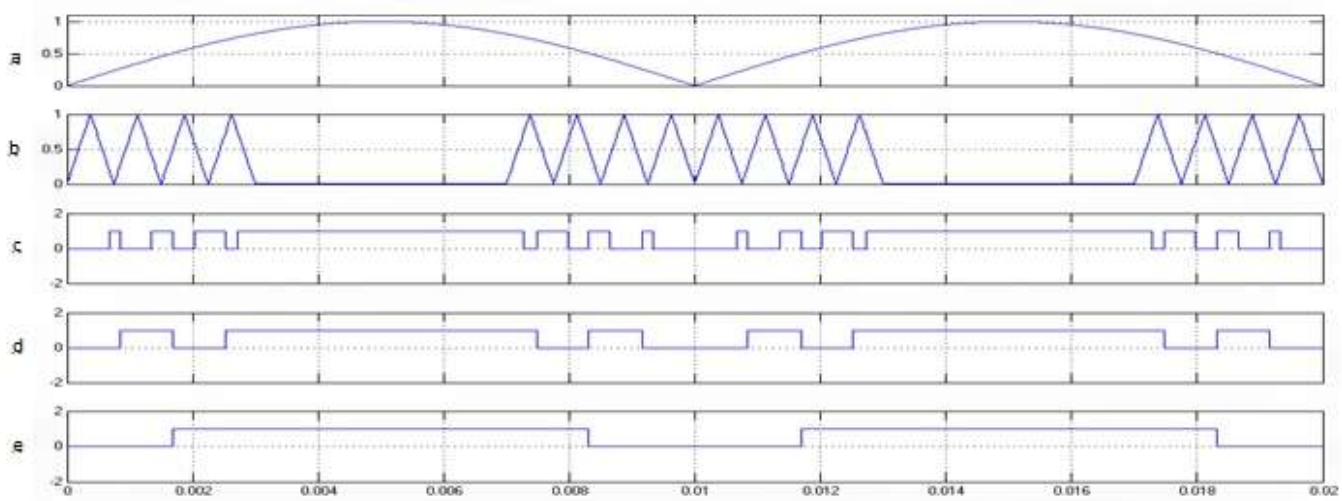

Fig.3. Generation of switching signals. a) Rectified sine reference b) Modified triangular carrier c) Switching sequence for Q0. d) Switching sequence for Q1. e) Switching sequence for Q2.

In the above circuit, the DC voltages used are V_d, $2V_d$ and $4V_d$. So the capacity of all switches in the H-bridge should be at least $7V_d$. The generation of switching signals for Q0, Q1, Q2 is as follows. A rectified sine wave, which is the reference, and a modified triangular carrier wave are compared (Fig. 3. a&b) to produce an SPWM sequence having seven pulses in each half cycle. This is the gating sequence for the first LM switch Q0 (Fig. 3. c). The gate pulses are given to a negative edge triggered JK flip flop and a positive edge triggered D flip flop and outputs from these two flip flops are combined to give the gate pulses for the second LM switch Q1 (Fig. 3. d) . Similarly the gate pulses for switch Q2 are obtained from the sequence of Q1 (Fig. 3. e). With a normal SPWM sequence, shown as Sequence 1 in Fig. 4 the THD in the output voltage is 26.2%. To improve this, a modified SPWM [4] is used. This is generated by increasing the width of the central pulse of the switching sequence for Q0. The different sequences are shown in Fig. 4. The output voltage waveform gradually becomes more sinusoidal as width of the central pulse increases. The switching sequence that produces the least harmonics is shown as Sequence 7 in Fig. 4. The THD of the output voltage, shown in Fig. 5a, is 11.26%. The load current for this sequence is shown in Fig. 5b. The current waveform is almost sinusoidal. A further increase in the width of the central pulse causes the THD to rise again.

The simulation is done in SIMULINK/MATLAB software for a constant load of R=5Ω and L=5mH. The THD of the different output voltages is obtained using the Fast Fourier Transform (FFT) analysis tool available in SIMULINK/MATLAB.

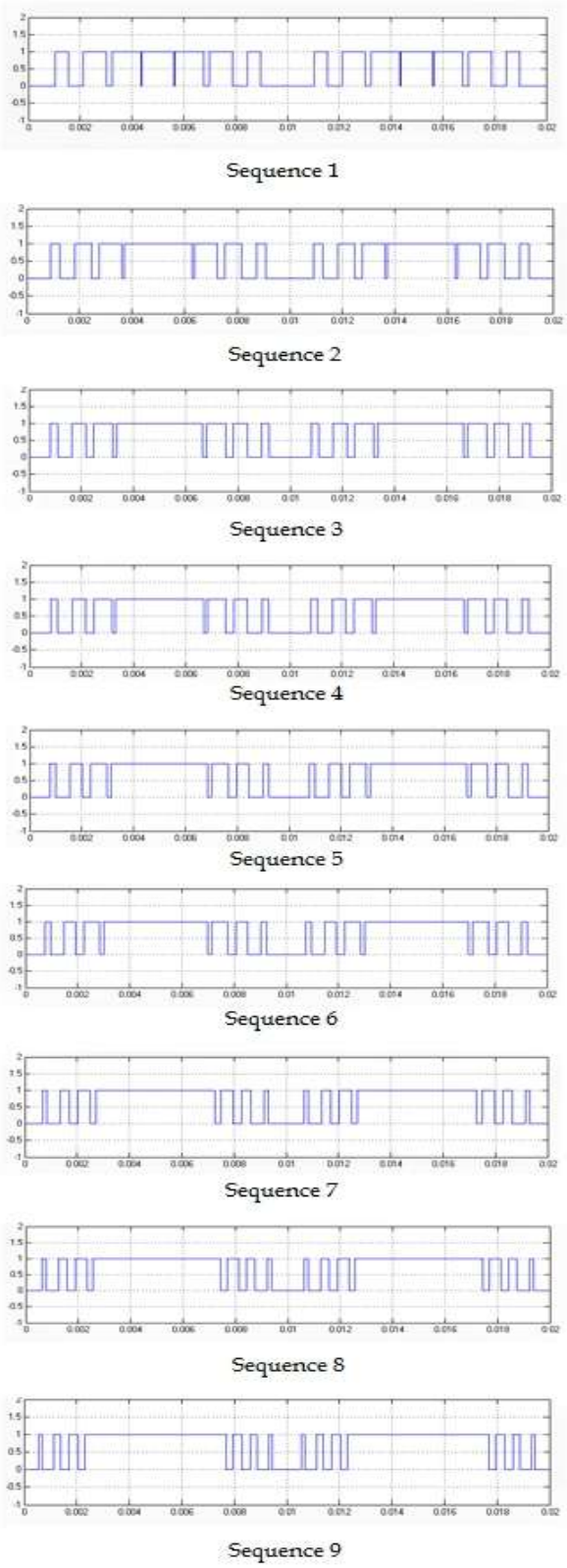

Fig.4. SPWM sequences

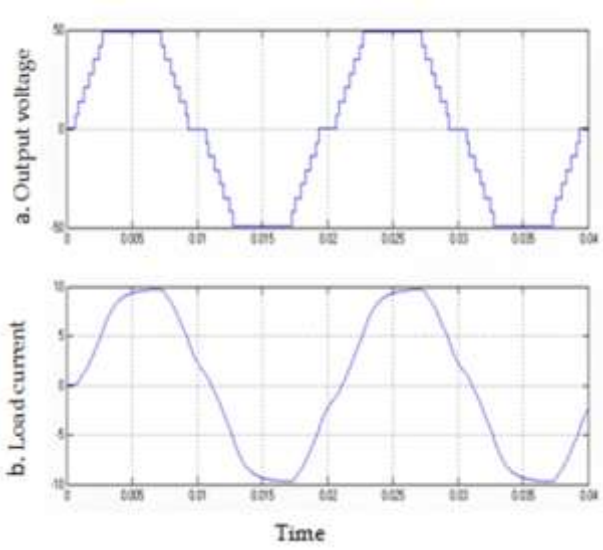

Fig.5. a. Output voltage (V), b. Load current (A)

Fig. 6 shows the % distortion in the output voltage due to each harmonic order relative to fundamental (50 Hz). It can be seen that majority of the distortion is due to the 5th and 11th harmonic. The 3rd harmonic and all its multiples are almost negligible. The % THD for each sequence is shown in Table 1.

A graph of %THD versus Sequence no. is also shown in Fig. 7.

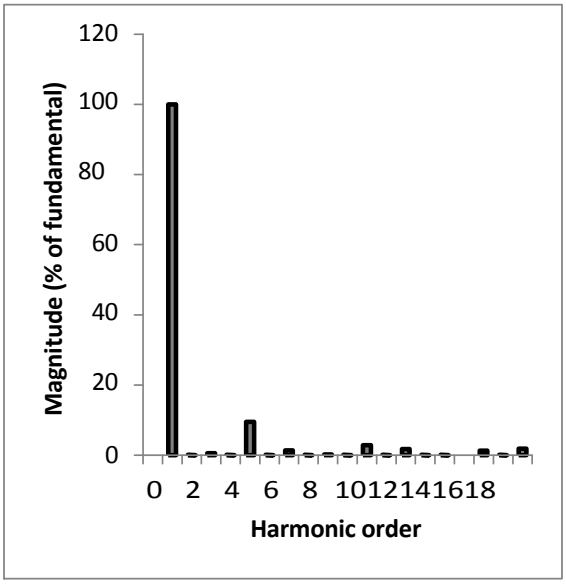

Fig.6. FFT analysis for output voltage waveform using switching sequence 7

Table 1

Sequence no.	%THD
1	26.2
2	19.58
3	15.42
4	14.97
5	13.42
6	12.43
7	11.26
8	11.58
9	13.09

In this topology it can also be seen that the %THD does not vary much for different input DC voltages. Table 2 shows the different harmonic content in output voltages when input DC V_d is different. The information is also presented in Fig. 8.

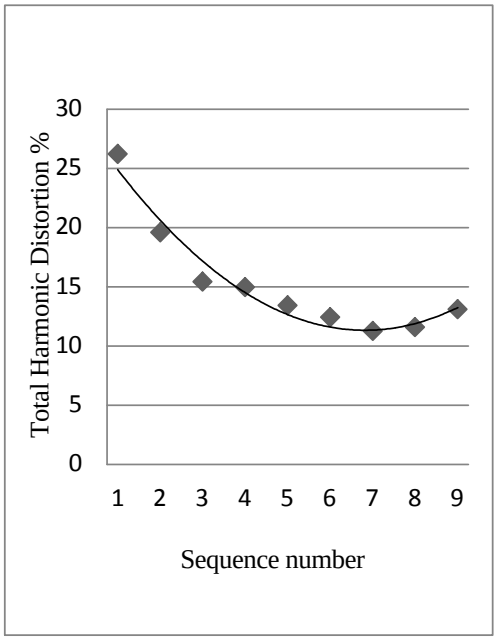

Fig.7. %THD versus sequence number

Table 2

V_d	%THD
1	11.29
2	11.29
3	11.23
4	11.29
5	11.23
6	11.27
7	11.26
8	11.30
20	11.28
33	11.28

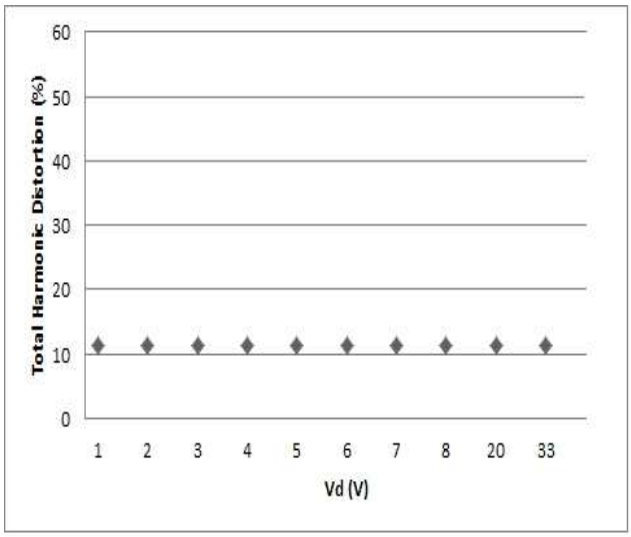

Fig.8. %THD for different values of Vd

III. CONCLUSION

An approach to reduce harmonics in multilevel inverters using modified SPWM switching pulses has been presented in this paper. The output voltages obtained using various modified SPWM sequences were analyzed using the FFT tool available in SIMULINK/MATLAB and it is shown that a significant reduction in %THD is attained for a particular modified SPWM sequence.

The topology used in this paper has a number of advantages when compared to other commonly used topologies. The number of switches is fewer leading to reduced cost. Also the number of levels in the output voltage can be increased conveniently.

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