ISSN: 2278 – 7798
International Journal of Science, Engineering and Technology Research (IJSETR)
Volume 1, Issue 5, November 2012

LOW POWER FPGA IMPLEMENTATION OF REAL-TIME QRS DETECTION ALGORITHM

VIJAYA.V, VAISHALI BARADWAJ, JYOTHIRANI GUGGILLA

Electronics and Communications Engineering Department, Vaagdevi Engineering College, Warangal, Andhra Pradesh.

***Abstract*--In this paper we proposenovel architecture for the implementation of ECG- QRS detection algorithm in FPGA. We exploit the pan and Tompkins QRS detection algorithm and provide low power architecture which uses the clock gating for reducing dynamic power and pipelining methodologies for necessary speed of execution and other low power design techniques to implement the algorithm efficiently in reconfigurable device i.e. FPGA. The implemented design has good detection accuracy and takes lesser computation time. Simulation of the algorithm is performed using MODELSIM 6.5b simulator taking the real-time ECG database as input. The overall architecture is implemented in XILINX VIRTEX 5 FPGA. The speed, power and area for the implemented algorithm are discussed.**

***Index Terms*—ECG, FPGA, ModelSim, QRS, SOC, R-R & XILINX**

I. INTRODUCTION

Many sophisticated algorithms have been proposed to improve the accuracy of prediction for electrocardiogram (ECG) waveform classification. There were methods of the principal component analysis (PCA), the adaptive resonance theory (ART), the wavelet neural network (WNN), or the fuzzy neural networks (FNN) [1]. The successful and important to reach their goal is to have an accurate extraction of ECGfeatures. Therefore, among these methods, many have created hybrid classification systems to increase the accuracy of ECG features prediction. However, these method andalgorithms were performing better using post and offline processes to extract or to predict the feature and parameters of ECG.

For a homecare ECG monitoring device, it is important to extract the features of the ECG signal in real-time. The ECG feature such as R-R interval, QRS amplitude and duration, the magnitude and duration of **p** wave, potential of **S-T** segment , and the magnitude and duration of **T** wave are important for homecare applications. For example, the information or feature of **R-R** interval can be derivate to analyze the heart rate variability (HRV). The duration of QT interval can be used to determine the status of myocardial re-polarization.

The objective of this abstract is to report a successfully development of a real-time ECG QRS detection algorithm that could be implemented using Field programmable Gate Array (FPGA) device with low power. The implemented System on Chip (SOC) using FPGA that could be used to acquire digital ECG data from an Analog-to-Digital Converter (ADC), to display ECG and extracted information on a VGA type LCD device, to store the acquired ECG and the extracted information into a flash memory chip and to communicate to a PC computer using an USB device. The hardware implementing algorithm was developed in Verilog Hardware Description Language (HDL).Simulation is performed in *ModelSim* 6.5b simulator and implementation is done in *Xilinx 9.2* with Virtex device.

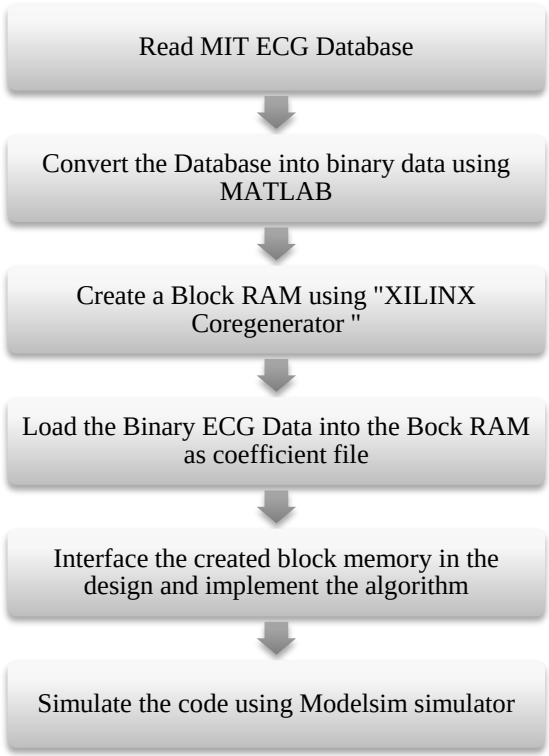


Figure 1: Real-time Simulation setup

II. Method and Material

The algorithm will be analyzing the component of the ECG signals and information in real time for identifying the abnormal rhythm and heart beat. The programmed System on Chip (SoC) will be controlling the detection and digitizing ECG, analyzing and extracting feature of ECG, monitoring the information update to the LCD, interfacing with USB and Flash Memory. In this way, both the ECG signal in real time and the analyzed information can be displayed on the LCD panel. The information can be transmitted and presented using self-developed software that is designed with Borland C++ Builder through USB device. The ECG data from MIT-BIH database could be input from hosted PC to the prototype system by USB bridge device. The real-time ECG acquired and digitized data could be inputto the prototype system directly. These data paths were shown in Figure 1. The acquired data, inputted data and result of the data processing could be shown at LCDdisplay in real-time, storedin Flash memory or transmitted to host PC by user selection.

III. Power Reduction Technique

There have been a number of power reduction methods that have been used for some time. Some of them are Clock gating, Gate level power optimization, Multi-VDD, Multi-VT etc. The method employed by this paper for power reduction of ECG-QRS detection blocks is clock-gating. A significant amount of dynamic power is consumed in the distribution network of the clock. This happens because the clock buffers have the highest toggle rate in any circuit. In addition, the flops receiving the clock dissipate some dynamic power even if the input and output remain the same. A simple solution to this power consumption is to turn off the clocks when they are not required. This approach is known as clock-gating. Figure shows how this works. In the original RTL, the register is updated or not depends on a variable ‘En’. The same result can be achieved by gating clock based on the same variable. If the registers involved are single bit, then a small savings occurs. It they are, say, 32 bits, then one clock gating cell can gate the clock to all 32 registers, there by achieving considerable power savings.

There are various sub-blocks or stages involved in the algorithm which are otherwise intermediate stages that remain idle for some delta time. Considerable power reduction can be attained by applying clock gating to these stages. Iterative structure, on the other hand has some registers that are not participating in the functioning during certain time period. Gating the clock to these registers can reduce power for the structure.

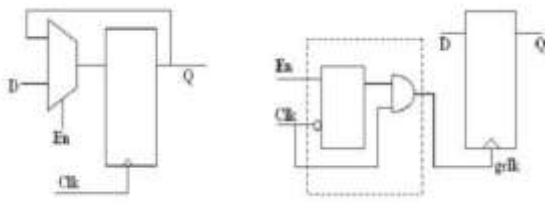


Figure 2: Register without and with clock gating

IV. Pan & Tompkins QRS detection algorithm

One of the most popular QRS detection algorithms, included in virtually all biomedical signal processing textbooks, is that introduced by Pan and Tompkins in [1]. An overview of the algorithm follows. Figureshows a graphical representation of the basic steps of the algorithm.

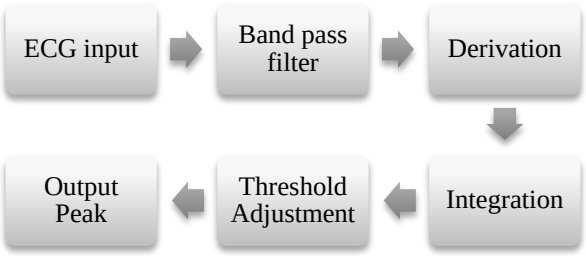


Figure 3: Algorithm Flow Diagram

In the first step the algorithm passes the signal through a low pass and a high pass filter in order to reduce the influence of the muscle noise, the power line interference, the baseline wander and the T-wave interference.

V. FPGA Architecture

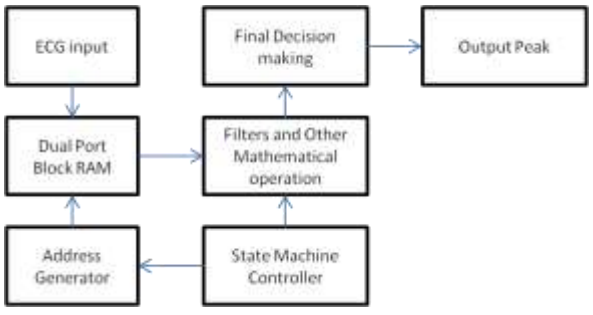


Figure 4: Architecture of the Logic

VI. Simulation Results

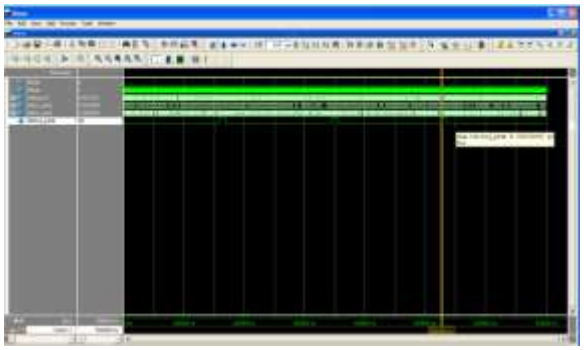


Figure 5: ModelSim output waveform as digital values

Figure 6: ModelSim output waveform as analog wave

VII. Implementation Results

A. Timing Summary:

Minimum period: 1.537ns

Maximum Frequency: 650.576MHz

Maximum output required time after clock: 3.924ns

Maximum combinational path delay: No path found

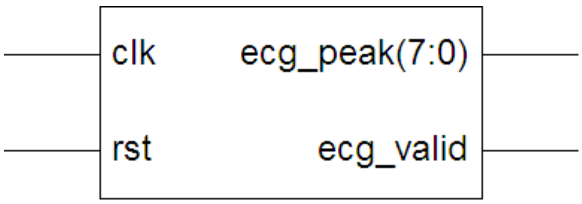
B. Power Report

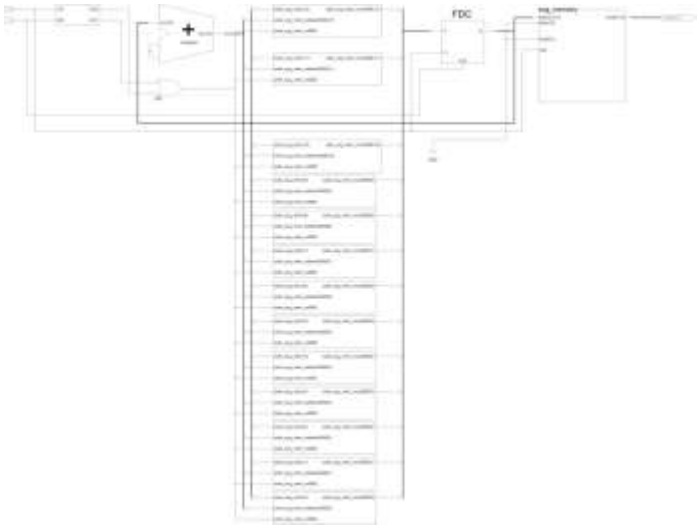
Xilinx XPower - [ecg_qrs_top.html]

File Edit View Tools Window Help

	Voltage (V)	Current (mA	Power (mW
Vccint	1		
Dynamic		0.00	0.00
Quiescent		168.72	168.72
Vccaux	2.5		
Dynamic		0.00	0.00
Quiescent		38.00	95.00
Vcco25	2.5		
Dynamic		0.00	0.00
Quiescent		1.25	3.13
Total Powe			266.84
Startup Curre		0.00	
Battery Capacity (mA Hours)			0.00
Battery Life (Hours)			0.00

Figure 7: FPGA Synthesis Snapshot





VIII. Conclusion

I have reported a successful development of a real-time ECG QRS detection algorithm that could be implemented using Field programmable Gate Array (FPGA) device with low power. I implemented System on Chip (SOC) using FPGA that could be used to acquire digital ECG data from an Analog-to-Digital Converter (ADC), to display ECG and extracted information on a VGA type LCD device, to store the acquired ECG and the extracted information into a flash memory chip and to communicate to a PC computer using an USB device.

IX. REFERENCES

A. Books:

[1] J. Pan and W. J. Tompkins, "A real-time QRS detection algorithm,"IEEE Trans. Biomed. Eng., vol. 32, no 3, pp. 230-236, Mar. 1985.

[2] J. Rabaey and M. Pedram, Low Power Design Methodologies. Kluwer, 1996.

[3] A. Chandrakasan and R. Brodersen, LowPower CMOS Design. IEEE Press, 1998.

B. Chapters in Books:

[4] P. S. Hamilton and W. J. Tompkins, "Quantitative investigation of QRS detection rules using the MIT/BIH arrhythmia database,"IEEE Trans. Biomed. Eng., vol. 33, no 12, pp. 1157-1165, Dec. 1986.

[5] L.-Y. Shyu, Y.-H. Wu and W. Hu, "Using wavelet transform and fuzzy neural network for VPC detection from the Holter ECG, "IEEE Trans. Biomed. Eng., vol. 51, no 7, pp. 1269-1273, July 2004.

[6] S. Kadambe, R. Murray and G. F. Boudreaux-Bartels, "Wavelet transform-based QRS complex detector, "IEEE Trans. Biomed. Eng., vol. 46, no 7, pp. 838-848, Jul. 1999.

[7] M. Pedram, "Power Estimation and Optimization at the Logic Level", International Journal of High-Speed Electronics and Systems, vol. 5, no. 2, pp. 179–202, 1994.

[8] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-Power CMOS Digital Design", IEEE Journal of Solid-State Circuits, vol. 27, no. 4, pp. 473–484, April 1992

[9] B. Chen and I. Nedelchev, "Power Compiler: A Gate Level Power Optimization and Synthesis System", ICCD'97: IEEE International Conference on Computer Design, pp. 74–79, Austin, Texas, October 1997.

[10] Y. Yoshida, B.-Y. Song, H. Okuhata, T. Onoye, and I. Shirakawa, "An Object Code Compression Approach to Embedded Processors", ISLPED-98: ACM/ IEEE International Symposium on Low Power Electronics and Design, pp. 265– 268, Monterey, California, August 1997.

[11] M. Pedram, "Power Minimization in IC Design: Principles and Applications", ACM Transactions on Design Automation of Electronic Systems, vol. 1, no. 1, pp. 3–56, January 1996.

[12] L. Benini, P. Siegel, and G. De Micheli, "Automatic Synthesis of Gated Clocks for Power Reduction in Sequential Circuits", EE Design and Test of Computers, vol. 11, no. 4, pp. 32–40, December 1994.

V.Vijayais working as Associate Professor in Vaagdevi Engineering Collage (affiliated to JNTUH), Warangal, Andhra Pradesh, India. She is a member in IEEE. Her current interests include MatLab.*E-mail: vijayaece009@gmail.com*

Vaishali Bharadwaj is working as Associate professor in Vaagdevi Engineering College (affiliated to JNTUH), Warangal, Andhra Pradesh, India. She is a member in IEEE, ISTE & IETE. Her current major interests include Digital Image Processing &MatLab.*E-mail: vaishalimtech@gmail.com*

JyothiraniGuggilla,studying M.Tech in Very Large Scale Integrated (VLSI) System Design in Vaagdevi Engineering College (affiliated to JNTUH), Warangal, Andhra Pradesh, India and received B. Tech degree in Electronics and Communications Engineering from JNTUH. Her current majorinterests include VLSI and Embedded Systems& Programming in Verilog as well as MatLab.