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Parallel VLSI Architectures for Communication Systems

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***Abstract*— In wireless communication the use of multiple antennas at both the transmitter and the receiver is a key technology to enable high data rate transmission without additional bandwidth or transmit power. Multiple Input Multiple Output (MIMO) schemes are widely used in many wireless standards ,allowing higher throughput using spatial multiplexing techniques. MIMO soft detection poses significant challenges to the MIMO receiver design as the detection complexity inceases exponentially with the number of antennas. As the next generation wireless system is pushing for multi-Gbps data rate, there is a great need for high-throughput low complexity soft-output MIMO detector. The brute –force implementation of the optimal MIMO detection algorithm would consume enormous power and is not feasible for the current technology.We propose a reduced-complexity soft-output MIMO detector architecture based on a trellis-search method. We convert the MIMO detection problem into a shorter path problem. We introduce a path reduction and a path extension algorithm to reduce the search complexity while still maintaining sufficient soft information values for the detection. We avoid the missing counter-hypothesis problem by keeping multiple path during the trellis search process. The proposed trellis search algorithm is a data-parallel algorithm and is very suitable for high speed VLSI implementation. Compared with the conventional tree-search based detectors, the proposed trellis-based detector has a significant improvement in terms of detection throughput and area efficiency. The proposed MIMO detector has great potential to be applied for the next generation Gbps wireless system by achieving very high throughput and good error performance. We will present ASIC and FPGA implementation results of various MIMO detectors LDPC decoders and Turbo decoders. We will discuss in details the computational complexity and the throughput performance of these detectors and decoders.**

Key Words-MIMO, VLSI architecture ,FPGA,

I. INTRODUCTION

Mobile wireless connectivity is a key feature of a growing rang of devices from laptops and cell phones to digital homes and portable devices. Many applications, such as digital video, are driving the creation of new high data rate multiple antenna wireless algorithms with challenges in the creation of area - time - power efficient architectures The mobile telecommunication system has evolved from several Kbps low data- rate 1G (for. "first generation") analog systems to the current 10-100 Mbps enhanced 3G (3.5G, 3.75G, 3.9G) generation. This is soon expected to be followed by 4G with a target data rate of 1 Gbps. Table 1.1 shows a representative set of mobile wireless standards to highlight their differences in data rates As an example of the next generation wireless system, 3GPP Long Term Evolution (LTE) [1] which is a set of enhancements to the 3G Universal Mobile Telecommuni- cations System (UMTS) [2], has received tremendous

attention recently and is con- sidered to be a very promising 4G wireless technology. For example, Verizon Wireless has decided to deploy LTE in their next generation 4G evolution. One of the main advantages of 3GPP LTE is high throughput For example, it provides a peck data rate

Table 1.1 : Major mobile telecommunication standa

Generation	Technology	Data rates	Year
1G	AMPS, TACS	14.4 Kbps	~1981
2 G	GSM, CDMA, TDMA	144 Kbps	~1995
2.5G, 2.75G	GPRS, EDGE, CDMA2000	~200 Kbps	~2000
3 G	W-CDMA, CDMA2000 1xEV-DO	384 Kbps	~2002
3.5G, 3.75G, 3.9G	HSDPA, LTE, WiMAX	10-100 Mbps	~2007
4 G	IMT-Advanced, LTE-Advanced	1 Gbps	2012 +

of 172.8 Mbps for a 2 × 2 antenna system, and a 326.4 Mbps for a 4 × 4 antenna system for every 20 MHz of spectrum. Furthermore, LTE-Advanced [3], the further evolution of LTE, promises to provide up to 1 Gbps peck data rate. In order to provide higher data rates, wireless systems are adopting multiple an- tenna configurations with spatial multiplexing to support parallel streams of wireless data. As an example, the Vertical Bell Laboratories Layered Space-Time (V-BLAST) system has been shown to achieve very high spectral efficiency [4]. There is an in- creasing demand for Gbps wireless systems. example, 3GPP LTE-Advanced, IEEE 802.16m WiMAX, IEEE 802.11ac WLAN, and WIGWAM [5] target for Gbps throughput with MIMO technology. In order to enable reliable delivery of digital data over unreliable wireless channels, the sender encodes the data using an error-correcting code prior to transmission. The additional information (or redundancy) added by the code is used by the receiver to recover the original data. Error-correcting codes are widely used in MIMO wireless communications. The most commonly used error correcting codes in modern systems are convolutional codes, Turbo codes, and low-density parity-check (LDPC) codes. As a core technology in wireless communications, FEC (forward error correction) coding has migrated from the basic 2G convolutional/block codes to more powerful 3G Turbo codes, and LDPC codes forecast for 4G systems.

II. BACK GROUND AND RELATED WORK

In this paper, we consider a spatial-multiplexing MIMO system with N_t transmit antennas and N_r receive antennas ($N_r \geq N_t$), The bit- interleaved coded modulation(BICM) is used at the transmitter, where the data bits are multiplexed onto N_t parallel streams. The MIMO transmission can be modeled as a linear system:

$$y = Hs + n,$$

where H is a $N_r \times N_t$ complex matrix and is

assumed to be known perfectly at the receiver, $s = [s_0 \ s_1 \ \dots \ s_{N_t-1}]^T$ is an $N_t \times 1$ transmit symbol vector, y is an $N_r \times 1$ received vector, and n is a vector of independent zero-mean complex Gaussian noise entries with variance σ^2 per real component. A real bit-level vector $x_k = [x_{k,0} \ x_{k,1} \ \dots \ x_{k,B-1}]^T$ is mapped to a complex symbol s_k as $s_k = \text{map}(x_k)$, where the b-th bit of x_k is denoted as $x_{k,b}$ and B is the number of bits per constellation point. Through this thesis, symbol s_k and its associated bit vector x_k will be used interchangeably. The maximum likelihood detector tries to make a hard-decision on the transmitted signal by finding an $\hat{s}$ which minimizes $\|y - H \cdot s\|^2$. ML detection is often used for a MIMO system without an outer error-correcting code, or an un-coded MIMO system. Practical wireless communication channels are inherently "noisy" due to the impair-ments caused by channel distortions and multipath effects. Error correcting codes are widely used to increase the bandwidth and energy efficiency of wireless communication systems. Table 2.1 summarizes the commonly used forward error correction (FEC) codes in mobile wireless standards. As a core technology in wireless communications, FEC coding has migrated from basic convolutional codes to more powerful Turbo codes and LDPC codes. Turbo codes, introduced by Berrou *et al.* in 1993 [6], have been employed in 3G and enhanced 3G wireless systems, such as UMTS/WCDMA and 3GPP Long-Term Evolution (LTE) systems. As a candidate for a 4G coding scheme, LDPC codes, which were introduced by Gallager in 1963 [7], have recently received significant attention in coding theory and have been adopted by some ad- vanced wireless systems such as the IEEE 802.16e/802.16m WiMAX system and IEEE 802.11n WLAN system.

Table 2.1 : Commonly used FEC odes in mobile wireless standards.

Generation	FEC codes
2G	Convolutional codes
3G	Turbo codes
4G	LDPC codes, Turbo codes

III. *HIGH THROUGHPUT MIMO DETECTOR*

ARCHITECTURE

In this chapter, we propose a novel path-preserving trellis- search (PPTS) algorithm and its high- speed VLSI architecture for soft-output MIMO detection. We represent the search space of the MIMO signal with an unconstrained trellis graph. Based on the trellis graph, we convert the soft-output MIMO detection problem into a multiple shortest paths problem subject to the constraint that every trellis node must be covered in this set of paths. The PPTS detector is guaranteed to have soft information for every possible symbol transmitted on every antenna so that the log-likelihood ratio (LLR) for each transmitted data bit can be accurately formed. Simulation results show that the PPTS algorithmcan achieve near optimal error performance with a low search complexity.The PPTS algorithm is a hardware-friendly data-parallel algorithm because the search operations are evenly distributed among multiple trellis nodes for parallel processing. Because the conventional tree-search algorithm is slow and difficult to be parallelized, we propose a search-efficient trellis algorithm to solve the soft MIMO detection prob- lem. The trellis-search

algorithm is a data-parallel algorithm that is more suitable for high speed hardware implementations. As an enhancement to the conventional Max-Log-MAP algorithm, we describe a n- Term-Log-MAP approximation algorithm to achieve near-optimum MIMO detection performance. The same trellis-search algorithm can be used to implement the n-Term-Log-MAP approximation algorithm. As we know, the optimum soft MIMO detection is based on the Log-MAP algo- rithm, which is too complex to be implemented in a practical MIMO receiver because the Log-MAP algorithm requires calculating log-sum of Q exponential terms, where Q is the $2 \wedge M$ constellation size and M is the number of transmit antennas.In practice, the Log-MAP algorithm is often approximated by the Max- Log-MAP algorithm to re- duce complexity. However, there is still a performance gap between the sub-optimum Max-Log-MAP detector and the optimal Log-MAP detector. Almost all the exist- ing MIMO detector implementations are based on the sub-optimal Max-Log-MAP approximation which limits the error performance of the detector.

III.I- *VLSI ARCHITECTURE FOR THE TRELLIS-SEARCH DETECTOR*

In this section, we describe VLSI architectures for the proposed PPTS detector We introduce a fully- parallel "systolic" architecture to achieve the maximum throughput performance, and a "folded" architecture to reduce area for lower throughput appli- cation. For the sake of clarity, we describe a PPTS detector architecture with $M = 2$ for the 4×4 16-QAM system. It should be noted that the architecture described can be easily scaled for other values of M and other MIMO configurations.

IV. *HIGH THROUGHPUT TURBO DETECTORFOR LTE/LTE-ADVANCED SYSTEM*

Turbo codes invented in 1993 [47] have attracted much attention recently because the new wireless systems are demanding higher and higher data rate. For example, in the LTE-Advance standard, the target data rate is 1 Gbps, which poses a significant challenge for the Turbo decoder design. Our goal is to develop a highly-parallel Turbo decoder architecture to achieve 1+ Gbps high data rate. We utilize the contention-free interleaver defined in the LTE standard to enable parallel Turbo decoding without additional data buffer. Turbo decoders suffer from high decoding latency due to the iterative decoding process, the forward-backward recursion in the maximum *a posteriori* (MAP) de- coding algorithm and the interleaving/de-interleaving between iterations [6, 8, 9]. Sliding window architectures are often used to reduce the latency of the MAP decod- ing. The choice of the sliding window algorithm may have a significant impact on the decoding BER performance and parallelism. In this chapter, we will present a new parallel sliding window algorithm and a new parallel non-sliding window algorithm for the LTE Turbo decoding. A high throughput Turbo decoder can be realized by parallelizing several MAP decoders, where each MAP decoder operates on a segment of the received codeword[9]. Due to the randomness of the Turbo interleaver, two or more MAP decoders may access the same memory at the same clock cycle which will lead to a memory collision. As a result, the decoder has to be stalled which consequently delays the decoding process. The Interleaver structures in the 3G standards, such as CDMA/W-CDMA/UMTS, do not have a parallel structure Although the memory stalls caused by the interleaver can be partially reduced by using write buffers . [10], the memory stalls will occur more and more frequently as the parallelism

degree increases. To solve this problem, the high data rate 3GPP LTE standard has adopted a contention- free, parallel interleaver which is called quadratic permutation polynomial (QPP) Turbo interleaver [11]. From an algebraic-geometric perspective, the QPP interleaver allows analytical designs and simplifies hardware implementation of a parallel Turbo decoder [12]. Based on the permutation polynomials over integer rings, every factor of the interleaver length can be a parallelism degree for the decoder [13] which is contension-free. Turbo decoder architectures in the literature are mostly based on the older matrix- permutation interleavers, thus the parallelism level is significantly limited. In this chapter, we will utilize the conflict-free QPP interleaving property to design a highly- parallel Turbo decoder for high speed wireless applications. The proposed decoder can achieve over 1Gbps data rate, which is significantly higher than the existing Turbo decoders.

V. *HIGH THROUGHPUT LDPC DECODER*

LDPC codes have inherent large parallelism that can be exploited to design a high- speed decoder. In theory, a random LDPC code with infinite block size will achieve near-capacity performance. However, it is very complex to implement such a decoder because of the random parity check matrix. To reduce implementation complexity while still maintaining good error protection capability, new wireless standards are adopting structured quasi-cyclic LDPC (QC-LDPC) codes. These structured QC- LDPC codes typically have a block size of several thousands bits and can be either regular codes and irregular codes. If the parity check matrix of a LDPC code has the same row and column degree, this LDPC code is called a regular LDPC code. Otherwise, it is an irregular LDPC code. Partial-parallel architectures are often used for the decoding ofthese structured QC-LDPC codes. The main challenge of the partial-parallel architecture is to de- velop a flexible decoder architecture to support multiple codes. The existing LDPC decoders are developed mostly for a particular standard which lacks the flexibility to be reconfigured to support multiple standards. In this chapter, we describe high- throughput low-density parity-check (LDPC) decoder architectures that support vari- able block sizes and multiple code rates. Various techniques are used to reduce the implementation complexity of the LDPC decoders. We first present a Min-sum algorithem based LDPC decoder Next, we present a more powerful Log-MAP algorithm. based LDPC decoder. To achieve multi-Gbps decoding throughput, we propose a multi-layer parallel decoder architecture. Furthermore, we propose a flexible decoder architecture that can support both LDPC codes and turbo code with a low hardware overhead.

VI. *ASIC AND FPGA IMPLEMENTATION RESULT*

In this chapter, we present the ASIC (application-specific integrated circuit) and FPGA (field- programmable gate array) implementation results of various MIMO de- tectors and channel decoders. The algorithms and architectures were presented in Chapters III, IV, and V, with Chapter III focusing on MIMO detection, Chapter IV fo- cusing on Turbo decoders, and Chapter V focusing on LDPC efficent verification environment before the creation of a VLSI ASIC acceleration design.

VI.I *DECODER ACCELERATOR DESIGN FOR WARP TESTBED*

We have implemented a channel decoder accelerator for the Rice WARP

Wireless Research Platform [14]. The Rice Wireless Research Platform is reconfigurable and consists of DSP and FPGA devices along with RF radios and high speed AD and DA converters. Experiments on the testbed can be performed to allow for algorithm and partitioning verification, identification of unforeseen bottlenecks, and over the air bit and frame error rate determination. The programmable transceiver hardware is connected to a general purpose host computer for control and interfacing. The testbed platform currently utilizes Mathworks Simulink environments for coordination and execution scheduling. Wireless algorithm design and mapping to parallel architecture prototypes on the FPGA boards is done via the Xilinx System Generator design tools. Additional modules can be created in Verilog HDL and either synthesized for ASIC analysis or mapped to FPGA for inclusion in the Xilinx System Generator design flow. The testbed uses the custom WARP board with Xilinx Virtex- II Pro and Virtex 4 FPGA devices. WARP allows for rapid prototyping with the integrated Maxim/Sharp2.4 GHz radio unit daughtercards for end-to-end laboratory experiments Fig. 6.1 shows the block diagram of the WARP testbed.

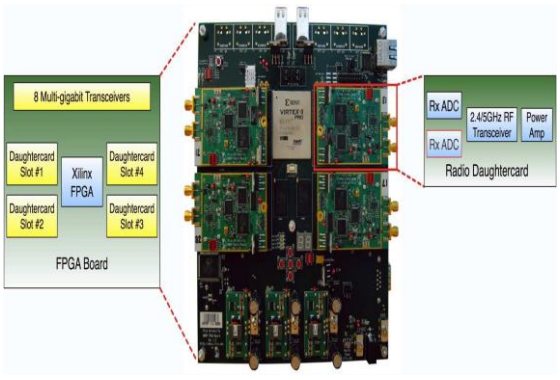

Fig.6.1 WARP testbed, including the custom Xilinx FPGA board and the radio daughtercards.

We have implemented an FEC codec (convolutional encoder + Viterbi decoder) for the WARP OFDM reference design (http://warp.rice.edu/trac/wifi/FDMReference Design). The most recent version of the OFDM reference design is v15.0. All of the PHY components are open-source and are available in the repository (with revision 1580 for FPGA v1 and svn revision 1585 for FPGA v2). The design is built using the 10.1 release of the Xilinx tools (ISE 10.1.03 + IP3, Sysgen 10.1.3.1386). In this design, a K=7 convolutional code is used. The code structure and the puncture pattern are compliant with the IEEE 802.11a standard. The FEC codec supports all three modes of the current WARP OFDM PHY: 1) SISO mode, 2) 2 × 2 MIMO mode, and 3) 2 × 2 or 2 × 1 Alamouti mode. The FEC codec supports three modulation types: 1) BPSK, 2) QPSK, and 3) 16-QAM. The coding can be turned on and off by programming the control register. The coding rate can be changed by modifying the second byte of the packet header Four different code rates are supported: 1/2, 2/3, 3/4, and 1.

VII. *CONCLUSION AND FUTURE WORK*

In this paper, we introduced a reduced-complexity MIMO detector based on a novel trellis-search algorithm. We represent the search space of the MIMO signal with a trel- lis structure and convert the MIMO detection problem into a shortest path problem. We proposed a high-throughput VLSI architecture, which can support multiple Gbps data rate. We presented the ASIC implementation results for the proposed MIMO detector architecture. Compared to the existing solutions, the proposed trellis-search based MIMO detector has a significant throughput advantage and a higher area effi- ciency. The simulation results suggest that the error performance is very close to the

optimum MAP detector. We proposed a parallel Turbo decoding algorithm and architecture to achieve Gbps data rate. We employ multiple MAP decoding units to process a codeword in parallel. By utilizing the contention-free interleaver structure, we avoid the memory conflict problem. We implemented a LTE-Advance Turbo decoder on an ASIC technology. We proposed a multi-layer parallel LDPC decoding algorithm and architecture to achieve multiple Gbps data rate. The proposed scalable LDPC decoder can be configured to support different block sizes and code rates. We presented several ASIC implementation results for LDPC decoders for various wireless standards, e.g. IEEE 802.11n and IEEE 802.16e. We further presented a joint LDPC/Turbo decoding algorithm and architecture to support more wireless standards with a small hardware overhead. We developed an iterative detection and decoding scheme based on the proposed trellis-search detector. In this scheme, the LLR soft values generated by the decoder are fed to the detector, and then the detector restarts a new round of detection to further refine the LLR soft values. The simulation results suggest that a 2.5-3 dB gain can be achieved by such a scheme. The component detector and decoder architectures and ASIC implementations can be combined to create this receiver.

Future Work

1. Real-value decomposition based trellis-search algorithm: The current trellis- search algorithm is based on the complex-value decomposition of the channel matrix. A variation of this algorithm is to use the real-value decomposition of the channel matrix and to form a real-valued trellis diagram. The number of stages and the number of nodes in each stage will change in a real-valued trellis diagram. It would be an interesting problem to extend the current complex-valued trellis-search algorithm to support real-valued model and compare the complexity and the performance of these two schemes.

2. Unified decoding architecture: It would be an interesting problem to extend the current joint LDPC/Turbo decoder architecture to support more error-correcting codes such as LDPC convolutional codes, non-binary LDPC codes, and non-binary Turbo codes.

3. Low power design: Next generation CMOS technology would offer more low- power features such as multiple supply voltages and multiple threshold libraries. Fur- thermore, the 3D CMOS technology is emerging to replace the current planar CMOS technology. The designer can take advantage of these new technologies to reduce the power consumption from all aspects. Low power design is especially useful for hand-held devices,such as cellphones.

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