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AN EFFICIENT CARRY SELECT ADDER WITH LESS DELAY AND REDUCED AREA USING FPGA QUARTUS II VERILOG DESIGN

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***Abstract*— A Carry Select Adder is one of the key hardware block in most digital and high performance systems such as FIR filters, digital signal processors and microprocessors etc. With advances in technology, design of CSA which offer either of the following high speed, low power consumption, regularity of layout less area and compact VLSI implementation. Researchers signify that Ripple Carry Adder had a smaller area while having lesser speed, in contrast to which Carry Select Adders are high speed but posses a larger area. And a Carry Look Ahead Adder is in between the spectrum having a proper tradeoff between time and area complexities. This proposed work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA .The proposed design has reduced area and power which is implemented in FPGA Model Sim Altera Edition 6.6C Quartus II simulation.**

***Index Terms*— ASIC, CSLA, Low power, Area Efficient, High Speed.**

1. INTRODUCTION

Adders are of fundamental importance in a wide variety of digital systems. Many fast adders exist, but adding fast using low area and power is still challenging. The importance of a fast, low-cost binary adder in a digital system is difficult to overestimate. Not only adders used in every arithmetic operation, but they are also needed for computing the physical address in virtually every memory fetch operation in most modern CPUs. Many styles of adders exist like Ripple adders are the smallest but also the slowest. More recently, carry-skip adders, Carry-look-ahead and carry-select adders are very fast but far larger and consume much more power than ripple or carry-skip adders.

As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a ASIC,VLSI chip. These signal processing applications not only demand great computation capacity but also consume considerable amount of energy. While performance and Area remain to be the two major design parameters, power consumption has become a critical concern in today's VLSI system design. The below figure 1 list some functions that ALU perform as the Add, Sub, Or, Rotate, Shift & In /Out Connectivity & register working.

The need for low-power VLSI system arises from two main forces. First, with the steady growth of operating frequency and processing capacity per chip, large currents have to be delivered and the heat due to large power consumption must be removed by proper cooling techniques.

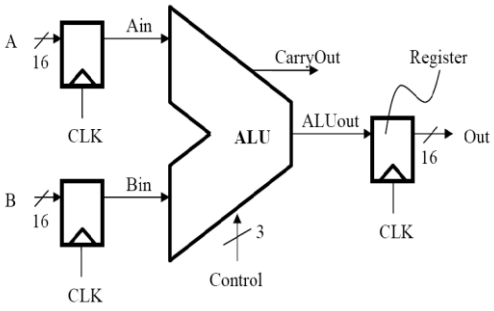

Figure 1.Basic Design Structure

Second, battery life in portable electronic devices is limited. Low power design[10] directly leads to prolonged operation time in the portable devices. Hence, optimizing the speed and area of the CSA is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas.

2. LITERATURE SURVEY

The CSLA[1] is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [3]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by the multiplexers.

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption [4][5]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area [6].In particular, carry-propagation adder (CPA) is frequently part of the critical delay path limiting the overall system performance due to the inevitable carry propagation chain. For example, the delay of a fast CPA for converting the final carry-saved number to its two's complement form in a Wallace tree multiplier is typically 25% to 35% of the total multiplier delay [7].

Power is an important factor for which Power optimization refers to number of Joules dissipated over a certain amount of time whereas energy is the measure of the total number of Joules dissipated by a circuit. In digital CMOS[2] design, the well-known power-delay product is

commonly used to assess the merits of designs. In a sense, this can be shown as power × delay = (energy/delay) × delay = energy, which implies delay is irrelevant.

3. RIPPLE CARRY ADDERS (RCA)

The well known adder architecture, ripple carry adder is composed of cascaded full adders for 4-bit adder, as shown in figure.2.It is constructed by cascading full adder blocks in series. The carry out of one stage is fed directly to the carry-in of the next stage. For an n-bit parallel adder it requires n full adders

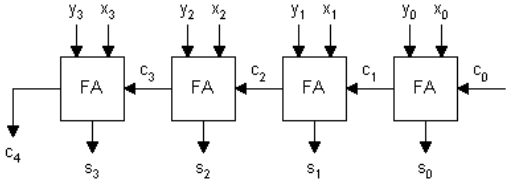

Figure 2. 4-bit Ripple Carry Adder

It is not very efficient when large number bit numbers are used. Delay increases linearly with bit length. That is delay from Carry-in to Carry-out is more important than from input to carry-out or carry-in to SUM, because the carry-propagation chain will determine the latency of the whole circuit for a Ripple-Carry adder. Considering the above worst-case signal propagation path we can thus write the following equation.

For a k-bit RCA worst case path delay is

$T_{RCA\text{-}k\ bit} = T_{FA}(X_0, Y_0\ C_0) + (k\text{-}2)* T_{FA}(Cin\ Ci) + T_{FA}(C_{in}\ S_{k-1})$.

A Brief summary of Ripple carry adder is as follows

1. **Basic ripple carry: AND-OR gates**
   Area: 32 transistors (per bit position)
   Delay: 2 stages of inverting logic (per bit position)

2. **Direct CMOS logic, share Cout**
   Area: 28 transistors
   Delay: 2 stages

3. **Use "inverting" property**
   Area: 27 (odd bits:26, even bits:28)
   Delay: ~1 stage

4. CARRY SELECT ADDERS

Carry select Adder is a better choice especially in the case of Carry delay. As in a ripple-carry adder, every full adder cell has to wait for the incoming carry before an outgoing carry can be generated. This dependency can be eliminated by pre-calculating i.e. by taking both possible values of the carry input and evaluating the result for both possibilities in advance. Once the real value of the incoming carry is known, the correct result is easily selected with a simple multiplexer stage. The implementation of this idea is called the linear carry select adder.

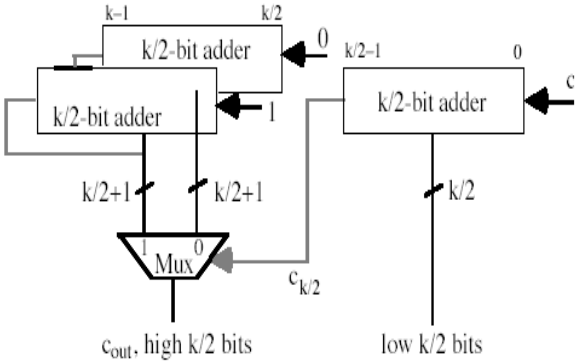

Figure 3.One level k-bit carry select adder

One-level k-bit Carry-Select Adder Cost & Latency is as follows

$C_{select\text{-}add}(k)=3C_{add}(k/2) + k/2 +1$

$T_{select\text{-}add}(k)=T_{add}(k/2) + 1$

In Carry select adder scheme, blocks of bits are added in two ways one assuming a carry-in of 0 and the other with a carry-in of 1.This results in two precomputed sum and carry-out signal pairs. Because of multiplexers larger area is required. Have a lesser delay than Ripple Carry Adders Hence we always go for Carry Select Adder while working with smaller no of bits.

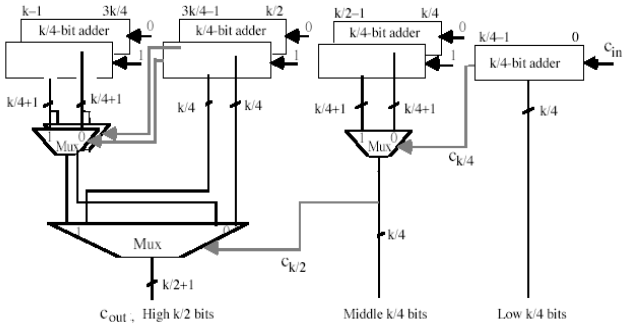

Figure 4. Two level k-bit carry select adder

In this paper we compared different adders Ripple Carry Adders, Carry Select Adders and the Carry Look Ahead Adders. The basic purpose of our experiment was to know the time and power trade-offs between different adders which will give us a clear picture of which adder suits best in which type of situation during design process as shown in table 1.

Table 1.Adder summary

Adder	Delay	Size
Ripple Carry	N	N
Carry Select	√n	2n
Carry Bypass	√n	n+√n
Carry Look ahead	Log n	n^3

The below graph describes Delay and Area for the different adders which are 32-bit and 64-bit operated as shown in the figure 5.

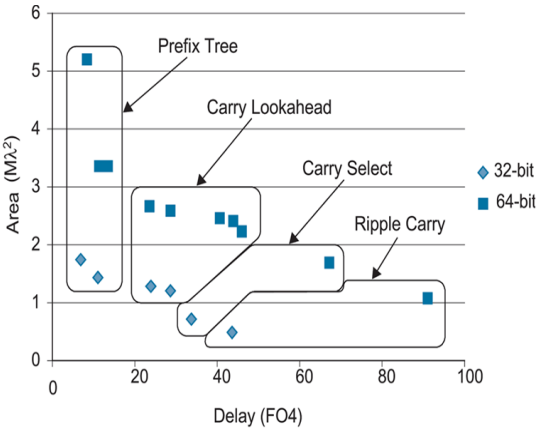

Figure 5. Area versus Delay of Synthesized adders[9]

5. PROPOSED 16-BIT CSLA

The architecture of proposed 16 bit CSLA is shown in Figure 6. It has different five groups of different bit size RCA and D-Latch. Instead of using two separate adders in the regular CSLA, in this method only one adder is used to reduce the area, power consumption and delay. Each of the two additions is performed in one clock cycle. This is 16-bit adder in which least significant bit (LSB) adder is ripple carry adder, which is 2 bit wide. The upper half of the adder i.e, most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself.

Carry out from the previous stage i.e., least significant bit adder is used as control signal for multiplexer to select final output carry and sum of the 16-bit adder. If the actual carry input is one, then computed sum and carry latch is accessed and for carry input zero MSB adder is accessed. Cout is the output carry.

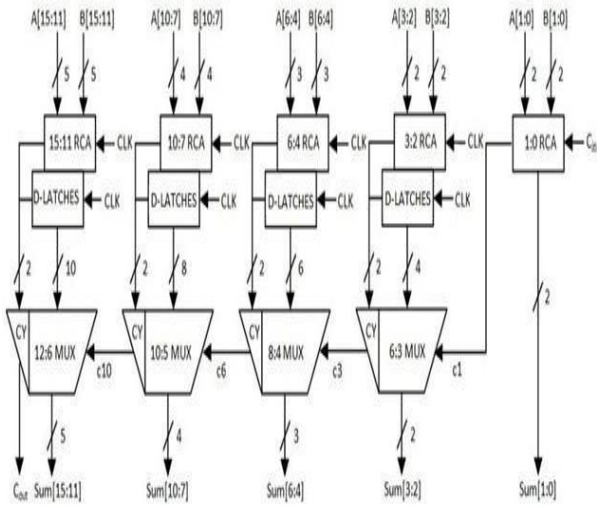

Figure 6. Proposed 16 bit CSLA

The group 2 performed the two bit addition which are a2 with b2 and a3 with b3. This is done by two full adder (FA) named FA2 and FA3 respectively. The third input to the full adder FA2 is the clock instead of the carry and the third input to the full adder FA3 is the carry output from FA2. The group 2 structure has three D-Latches in which two are used for store the sum2 and sum3 from FA2 and FA3 respectively and the last one is used to store carry. Multiplexer is used for selecting the actual sum and carry according to the carry is coming from the previous stage. The 6:3 multiplexer is the combination of 2:1 multiplexer.

When the clock is low a2 and b2 are added with carry is equal to zero. Because of low clock, the D-Latch is not enabled. When the clock is high, the addition is performed with carry is equal to one. All the D-Latches are enabled and store the sum and carry for carry is equal to one. According to the value of c1 whether it is 0 or 1, the multiplexer selected the actual sum and carry in this way power area can be reduced.

6. QUARTUS II SIMULATION RESULTS AND ANALYSIS

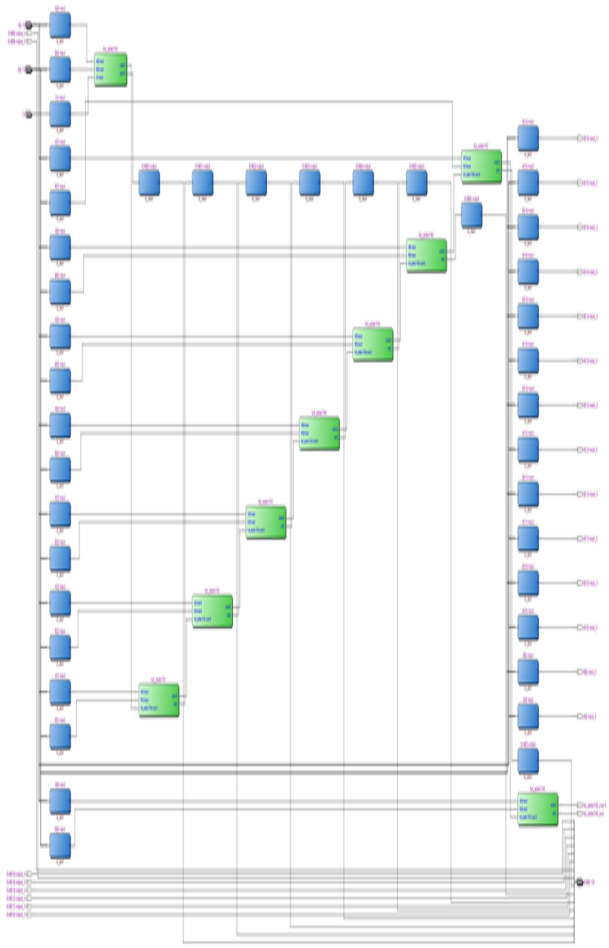

Figure 7. Block Diagram of CSA in FPGA Model Sim Altera Edition 6.6C simulator

The above figure is the schematic and technological representation of multiple full adders FA(0) to FA(15) which are connected in cascade. In this diagram the inputs A(0) to A(15) and B(0) to B(15) has connected as IO_IBUF and sum(0) to Sum(15) are acted as IO_OBUF registers.

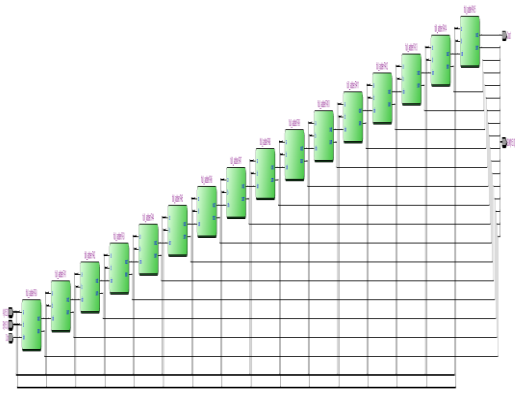

Figure 8.RTL Schematic diagram of FPGA Quartus II simulator

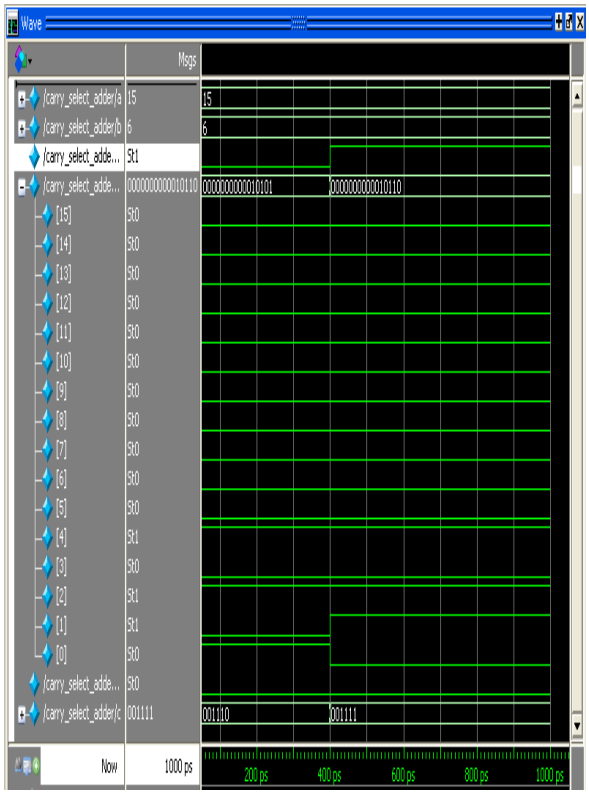

Figure 9.Timing waveforms for CSA using Quartus II simulator

Analysis & Synthesis Resource Usage Summary

	Resource	Usage
1	I/O pins	50
2	Maximum fan-out node	full_adder:FA0|cout~0
3	Maximum fan-out	2
4	Total fan-out	163
5	Average fan-out	1.23

Figure 10.Analysis & Synthesis Resource Usage Summary

Flow Summary

Flow Status	Successful - Fri Jul 19 15:53:36 2013
Quartus II Version	10.1 Build 153 11/29/2010 SJ Web Edition
Revision Name	Ripple_Carry
Top-level Entity Name	Ripple_Carry
Family	Cyclone IV GX
Total logic elements	33 / 21,280 (< 1 %)
Total combinational functions	33 / 21,280 (< 1 %)
Dedicated logic registers	0 / 21,280 (0 %)
Total registers	0
Total pins	50 / 167 (30 %)
Total virtual pins	0
Total memory bits	0 / 774,144 (0 %)
Embedded Multiplier 9-bit elements	0 / 80 (0 %)
Total GXB Receiver Channel PCS	0 / 4 (0 %)
Total GXB Receiver Channel PMA	0 / 4 (0 %)
Total GXB Transmitter Channel PCS	0 / 4 (0 %)
Total GXB Transmitter Channel PMA	0 / 4 (0 %)
Total PLLs	0 / 4 (0 %)
Device	EP4CGX22CF19C6
Timing Models	Early Fitter Estimation

Figure 11. Flow Summary for Ripple carry Adder

PowerPlay Power Analyzer Summary

PowerPlay Power Analyzer Status	Successful - Sat Jul 20 14:48:31 2013
Quartus II Version	10.1 Build 153 11/29/2010 SJ Web Edition
Revision Name	Ripple_Carry
Top-level Entity Name	Ripple_Carry
Family	Cyclone IV GX
Device	EP4CGX22CF19C6
Power Models	Preliminary
Total Thermal Power Dissipation	104.15 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	88.94 mW
I/O Thermal Power Dissipation	15.21 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Figure 12.Power Analyzer summary in Quartus II simulator

7. CONCLUSIONS

We studied about different adders among compared them by different criteria like Area, Time and then Area-Delay Product etc. so that we can judge to know which adder was best suited for situation. After comparing all we came to a conclusion that Carry Select Adders are best suited for situations where Speed is the only criteria. Similarly Ripple Carry Adders are best suited for Low Power Applications. But Among all the Carry Look Ahead Adder had the least Area-Delay product that tells us that, it is suitable for situations where both low power and fastness are a criteria such that we need a proper balance between both as is the case with our paper. The type of adder to be selected depends on the following factors

1. Area of the layout which influences the cost.
2. Timing and power which influences the performance of the adder.

The 8-bit CSLA is done by the same structure of 16-bit CSLA except group 4 and group 5. The 8th bit inputs are directly given to the full adder to complete the 8-bit sum and carry. The 32-bit CSLA is done by cascading two 16-bit CSLA and 64-bit CSLA is done by cascading two 32-bit CSLA. The major disadvantage of modified CSLA using BEC is the increasing delay. This disadvantage is overcome in proposed architecture which reduces the delay, area and power than the regular and modified CSLA.

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10. BIOGRAPHIES

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He has many accepted International Journals & Conferences in that one of the Research Paper entitled **"Design of Optimal Digital FIR Filter using Particle Swarm Optimization Algorithm"** with **DOI 10.1007/978-3-319-00951-3_31** was published in **The Fifth International Conference** on **Wireless & Mobile Networks(WIMO-2013),Turkey** which is in conjunction with Computational Science, Engineering and Information Technology **(CCSEIT-2013)** in a book title **Advances in Computational Science, Engineering and Information Technology** by **Springer International Publishing Switzerland June 2013**.

Recently He acted as **Co-Author** for the Research Paper entitled "**A Verilog Design in FPGA Implementation of QPSK Digital Modulator"** which was published in **IJESRT Volume 2 Issue 7 July 2013**. He reviewed some research papers of International Journals. With his PG Scholar another Research Paper entitled **"Implementation of Time Frequency Block Thresholding Algorithm in Audio Noise Reduction"** which was published in **IJSETR Volume 2 Issue 7 July 2013.** & His current research interest includes design of Signal & Image Processing, and Embedded VLSI System design.