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Automobile Data Acquisition and Processing System Based on Dual CPU Architecture

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***Abstract*— Data Acquisition System (DAQ) plays a key confront in all recent technologies. In traditional approach, the DAQ system is generally designed with single CPU architecture. The major limitation with this Single core Architecture is, with undeterministic inputs it could be impossible to guarantee everything is serviced in time. In order to triumph over this a new generation of affordable sophisticated automobile data acquisition and processing (DAQP) systems which consists of embedded controller and Field Programmable Gate Array (FPGA) i.e., dual CPU Architecture is introduced. With FPGAs hardware reconfigurability, the hardware implementation of the different processing functions of the device allows for high-speed processing without the need of expensive general-purpose processors, as is the case of computer-based or microcontroller-based data acquisitions (DAQs)**

***Index Terms*— DAQ, Embedded system Wireless communications, FPGA, GPS tracking.**

I. INTRODUCTION

Highlight a s Data acquisition systems (DAQ) are devices that are used to obtain data from the environment surrounding it. Existing DAQs, can acquire single channel or multi-channel signals. Numerous applications stipulate the existence of a multi-channel DAQ.

An embedded system is a special-purpose computer system intended to execute one or a few dedicated functions, frequently with real-time computing restriction. Employing the embedded systems into the data acquisition environments can achieve low cost, low power consumption and portability. Field-programmable gate arrays (FPGA) are the state of the art technology for building a prototype which can be used in various applications. For smaller designs and/or lower production volumes, FPGAs may be more cost effective than an ASIC design. The prevailing FPGA advantage reconfigurability that allows design upgrades without hardware replacement. Moreover, FPGA provides a wide range of DSP operations.

The next generation Intelligent Transportation System (ITS) will rely profoundly on several vehicle communication systems as well as peer-to-peer and peer-to-base station communications. The cornerstone of next-generation ITS, is seamless integration of in-vehicle networking with existing wireless telephony infrastructure. Drivers ought to be capable to wander amid their cellular phone network and their in-vehicle network. There will be transparent and automatic data access and synchronization. Peer-to-peer communications offers a facility for information to be relayed down a highway therefore transportation system can adapt and react to events autonomously in real-time.

In this paper, an extensible vehicle performance monitoring system is presented and that exploits data transmission capabilities of the Global System for Mobile Communication (GSM). Global Positioning System (GPS) technology is also exploited to provide vehicle location.

II. SYSTEM DESIGN AND IMPLEMENTATIONS

Three parts of embedded data acquisition for mobile vehicle are: i) PIC16F877A Microcontroller with Peripheral Circuit Unit, ii) XC3S50A featuring Xilinx Spartan3A FPGA Data Acquisition Unit and iii) The Sensor Signal Processing Unit.

Sensor module involves fuel level monitoring speed monitoring, distance monitoring and GPS device and so on. FPGA Data Acquisition unit collects the data acquired by every sensor.

The sensor output normally enters pre-processing or conditioning before it can be used by another processing unit such as a microcontroller or a DSP.

Pre- Processing or Interface Unit includes actions such as buffering, signal amplification, noise reduction, error correction and compensation. Thereby the DSP or processor will concentrate on additional complicated activities that need enormous computing resources.

Field Programmable Gate Array (FPGA) processes the acquired data and the microcontroller unit controls the

vehicle and also transmits the data through GSM network based on

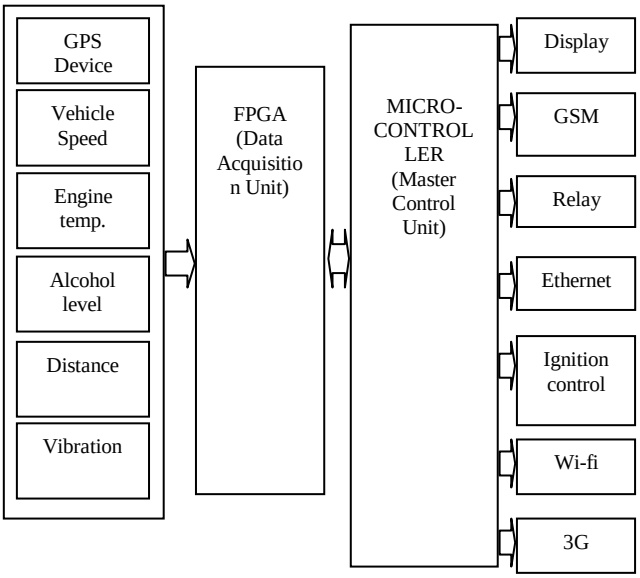

Fig.1 System block diagram for data acquisition

the processed results.The system block diagram for data acquisition is shown in Fig.1

III. SENSOR SIGNAL PROCESSING UNIT

If Data Acquisition channel is secluded by linear optocoupler and also all the input powers are isolated by DC converter modules in order to achieve the safety of the systems. Initially, all sensor signals are filtered through the low-pass filter circuit. For the current signal, the precision resistance is used to convert the current into voltage. To acquire vehicle diagnosis and to get the driving status various types of sensors are used. Each sensor signal ought to be sent in a straight line to FPGA for parallel processing. Thus, high capability and multi-port FPGA with upper price is needed. In order to decrease the system cost and meet up the real-time requirements, the grouping of parallel acquisition mode is used in the design. The following parameters of a vehicle can be observed are speed, temperature, fuel, battery indication, coolant level etc. These are measured by appropriate sensors. And then it is followed by signal processing block and then given to Analog to Digital Converter (ADC) and in turn to FPGA unit.

IV. FPGA DATA COLLECTION

In data acquisition system, for sensor parameters collection and processing FPGA is used as coprocessor. The functions of FPGA includes AD control acquisition module, channel configuration module, switch signals acquisition module, and so on.

Four actions are performed by sensor processing system, they are: i) Acquisition, ii) Processing, iii) Integration and iv)Analysis. Sensor data congregation and processing is vital to ecological structure, isolated systems, intellectual industrialized systems and medical systems, to name a few. The primary action in a sensor processing system is to obtain data from a physical system or surroundings. Classically, the data composed is a function of a physical variable over time and space. Fig.2 below depicts a distinctive sensor processing system. The electrical production from a sensor normally necessitates some form of conditioning or pre-processing prior to it can be used by other processing units called a DSP or a microcontroller.

Some of the functions of this pre- processing or interface unit consist of activities such as signal amplification, noise reduction, buffering, error correction and compensation. This will allow the DSP or processor to concentrate on more classy activities that need enormous computing resources.

Single likely approach is to construct this interface circuitry on a Field Programmable Gate Array (FPGA) platform. FPGAs are being progressively more used in sensor based applications. FPGAs found to be sensible alternatives to discrete mechanism or custom hardware (ASICs). They offer speed-ups from end to end hardware area while still only if the flexibility to adapt the hardware to changing application needs. High end FPGAs provide enormous processing resources, significant on-chip
independent RAM banks and high clock speed building them appropriate for scheming well-organized data capture and analysis systems. Unlike microcontroller-based acquisition systems, the large number of configurable input/output channels available in FPGAs allows designers to set up systems supporting multi-channel acquisition paths. FPGA acquisition function block diagram is shown in Fig.3.

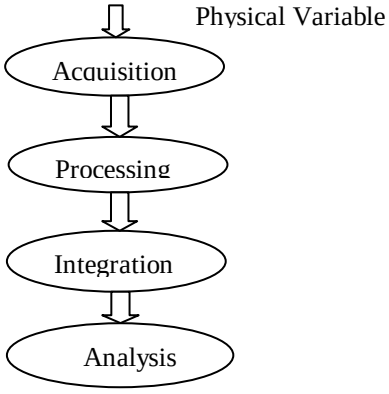

Fig.2 Sensor Processing System

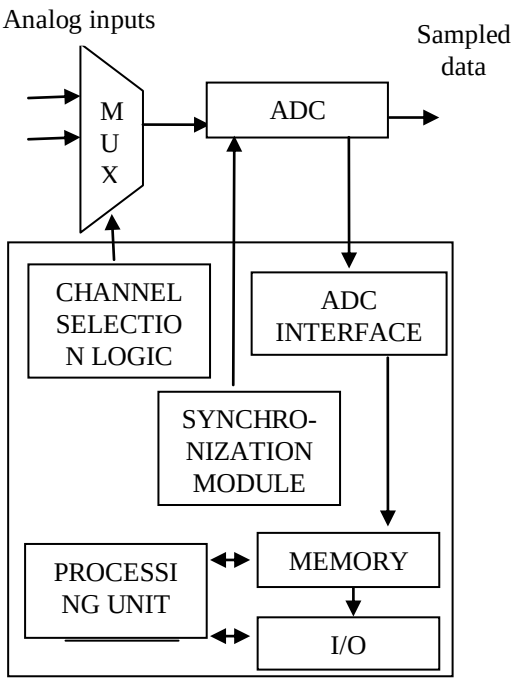

Fig.3 FPGA Acquisition Function Block Diagram

The working process of FPGA modules is shown in Fig.4. First and foremost, various trial parameters have to be affirmed. N channels are obtained by our proposed system. Each channel is allocated a predefined time slot in order to acquire n sample/ channel is the sample acquisition time and T is the elapsed time. As shown in Fig. 4, the acquired samples from the first channel are accumulated in the buffer. If the buffer is not filled (i.e. T < N. n), then increment buffer index and the channel time slot is checked. If this channel still has extra samples, ADC will acquire more data from this channel. If not, the selection lines (sel) will be altered by incrementing it by one and taking mod N where N is the number of channels and mod operation find the reminder of the division process. This alteration provides collecting data from the next channel and storing it into the same buffer in order to optimize the utilization of the ADC. Following data is collected from all channels and the buffer is full, all data is ready to be processed and thereafter it is stored into the memory.

V THE COORDINATED CONTROL OF CONTROLLER AND FPGA

The projected data acquisition system entails the communication with GSM network, real-time process parameters, control signals and output alarm signals. Several tasks are scheduled by embedded operating system.

The software of microcontroller is divided into several parts including FPGA collection results reading, parameters analysis, LCD display, GSM communications, relay control, interrupt handling of communications and other tasks. In the design, not merely the controller can be programmed with dynamism through the PC communication, but as well FPGA

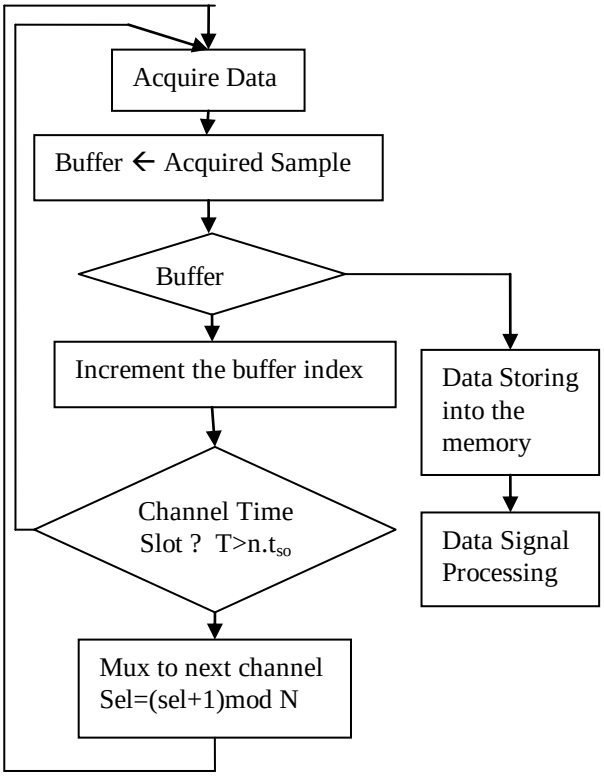

Fig.4 The working process of FPGA data acquisition unit.

be able to be programmed all the way through controller interface when the system is operating.

VI CHARACTERISTICS OF PROPOSED SYSTEM

The proposed system determined to be an accurate, reliable and cost-effective data collection machine that will be fitted on vehicles to monitor vehicle/driver performance.

The proposed system functionality involves inputs from a number of disciplines and involves the application of various technologies. Therefore project is challenging on both technical and management levels, and thereby presents a part of hazard to the implementation of the project. The high level functional architecture of the proposed system consists of various main functional elements described in following sub sections.

6.1 NAVIGATION FUNCTION/POSITIONING

Navigation Function/Positioning is responsible for the derivation of all spatial, temporal and spatio-temporal (derivative) data of the vehicle. It includes location in 3-D space, time, slope, speed and acceleration. The function supported by existing technological developments including GSM, GPS and GIS, could be improved by better modeling and augmentation with other space based and/or terrestrial systems.

The GT-320R GPS Module is used in this system. It is a compact all-in one GPS module, provides fast and easy system integration with minimal development risk.

6.2 Vehicle And Driver Performance

It is responsible for monitoring and capturing the vehicle and driver performance data, including the deflection (displacement) of the pedals. This function supports the necessary instrumentation for driver and vehicle performance, and could be interfaced to the existing (embedded) vehicle engine management and analytical systems.

This system permits observing most electrical systems on the vehicle. Monitored objects are speed, RPM, fuel level, ignition voltage, and coolant temperature. Also it gives collision caution and automatic crash warning modules.

6.3 Communications And Interface

For the transportation of data and control messages between the functional elements and with the mobile network communication and interface unit is needed. Communications function of system is envisaged to be hold by enhanced GSM technology, even though other communications systems employing other frequencies also considered. The controller is specified to provide efficient data handling and processing with the interfaces defined. GSM has become key confront in the world's fastest growing mobile communication standard. It allows faultless and secure connectivity between networks on a global scale. Digital encoding is used for voice communication, and time division multiple access (TDMA) transmission methods provide a very efficient data

Fig.5.1 Engine Speed Monitoring Module

rate/information content ratio. Our proposed system uses SIM900 GSM module.

VII. APPLICATIONS

7.1 Engine Speed Monitoring & Control System

The crankshaft is applied with a reflective coating and at the middle strip of black absorbing material is placed. Light is projected on to this rotating shaft. The light is reflected by the reflecting surface and is absorbed by the black-colored strip. The reflected light is sensed by photo sensor, followed by the signal amplifier. This signal is applied to Schmitt trigger and corresponding pulses are obtained, then this pulse is given into the counter circuit.

The Engine speed is monitored once in a second and converted to RPM, and displayed in the display unit. When the Engine speed exceeds a predefined value, the monitor intervenes, and activates a motor to apply the brake. In this way the speed is automatically inadequate to a predefined value.

7.2 ALCOHOL Level Monitoring

The alcohol level can be monitored by using MQ-3 sensor. This system consists of a ultra sonic transponder. The transponder is fixed in such a way that the driver has to undergo alcohol test before starting the vehicle. The sensor measures the alcohol level. This information is stored in FPGA processor Memory regularly. If any predefined value is set earlier and the measured alcohol level exceeds that value then the PIC microcontroller automatically stop the vehicle.

7.3 COLLISION Detection System

One of the major problems in road transport is Head on Collisions. To avoid or minimize collisions, the distance between this vehicle and neighboring vehicles is to be monitored. If the distance reduces between the vehicles once again, using Ultrasonic proximity sensor which gives intermittently to warn the driver. This Ultra sonic proximity sensor consists of ultra sonic transmitter and receiver and signals are transmitted at regular intervals. These signals, upon falling on approaching vehicle, would be reflected. The

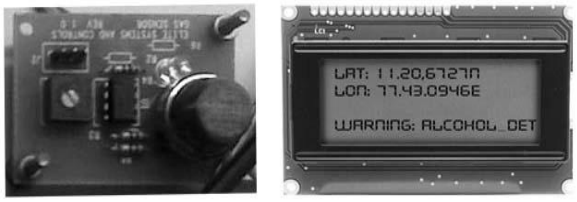

Fig.5.2 Alcohol Detection Module

Fig.5.3 Collision Detection Module

reflected signal is received by Receiver circuitry, and the time for receiving the reflecting the signal is calculated. The time reduces for an approaching vehicle. This can be checked by a program, which alerts the driver.

6.4 Temperature Monitor

The temperature monitor is used to monitoring the engine temperature by using thermal relays such as thermistors. Thermistor is used to form a resistor divider network and the junction voltage is fed to a voltage amplifier followed by ADC. Then the digitized value is used by the program to check the limits and gives the warning to driver to stop the vehicle. Most of the vehicles have a temperature gauge, but it lacks the ability to provide an audible warning when problem exists. But this system gives the real-time engine temperature

on a digital display. If the engine overheats, the ETMS will start beeping intermittently to warn the driver. When engine temperature continuously growing, it will beep continuously. This protects engine from overheating.

VII. Conclusion

In this paper, a new generation of affordable sophisticated data acquisition and processing (DAQP) system for automobiles was implemented. Our system design has an open architecture that can be easily expanded to other applications. In this system, we have used controller as a part for controlling the applications. But, here the parallel processing and reconfigurable feature of FPGA is not utilized completely. So, a DAQ system completely based on FPGA is planned to design in future. It will support DSP applications in a great manner with high speed.

Fig.5.4. Engine Temperature Monitoring Module

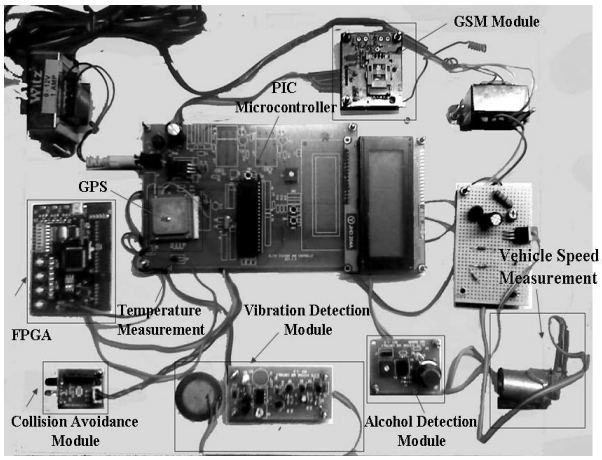

Fig.6 The Prototype of Proposed System

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