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DVM: A New Multiplier Architecture with Two Variables

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***Abstract*— Multiplication is one of the supplementary silicon-intensive functions, particularly while executed in Programmable Logic. Multipliers are key apparatus of several high concert systems such as FIR filters, Microprocessors, Digital Signal Processors, etc. A system's performance is usually dogged by the performance of the multiplier, since the multiplier is usually the slowest component in the system. Additionally, it is normally the most area consuming. Therefore, optimizing the speed and area of the multiplier is a most important design issue.**

As a solution to optimizing the speed and area of the multiplier we are proposing DVM a novel multiplier architecture based on ROM approach using Vedic Mathematics. DVM is similar to that of a Constant Coefficient Multiplier (KCM). But, KCM depends on fixed one input, while DVM can multiply two variables. The DVM is implemented on a Cyclone III FPGA, compared with Array Multiplier and Urdhava Multiplier for both 8 bit and 16 bit cases and the results are presented. The DVM is 1.5 times faster than the other multipliers for 16x16 case and consumes only 76% area for 8x8 multiplier and 42% area for 16x16 multiplier.

Keywords: DVM; KCM; Vedic Maths; Array Multiplyer; FPGA;

I. INTRODUCTION

Multiplication is one of the supplementary silicon-intensive functions, particularly while executed in Programmable Logic. Multipliers are key apparatus of several high concert systems such as FIR filters, Microprocessors, Digital Signal Processors, etc. A system's performance is usually dogged by the performance of the multiplier, since the multiplier is usually the slowest component in the system. Additionally, it is normally the most area consuming. Therefore, optimizing the speed and area of the multiplier is a most important design issue.

Vedic mathematics [I] is the prehistoric Indian method of mathematics which primarily deals with Vedic mathematical formulae with their relevance to diverse kindling of mathematics. The sound 'Vedic' is consequent from the sound 'Veda' which means the stockroom of all knowledge. After eight years of research Sri Bharati Krishna Tirthaji reconstructed the vedic mathematics from the ancient Indian Vedas. According to his research, Vedic mathematics is principally based on sixteen morality or word-formulae which are called as Sutras. This is a awfully fascinating countryside and presents some efficient algorithms which can be applied to diverse kindling of Engineering such as Computing and Digital Signal Processing.

II. ARRAY MULTIPLIER

In Array multiplier AND gates are use for invention of the bit-products and adders for gathering of produce bit products. All bit-products are produce in similar and composed throughout a collection of complete adders or any other category of adders. Seeing as the collection of multiplier is having a usual formation, cabling and the explain are complete in a lot basic manner. Hence, along with other multiplier structure, collection multiplier takes up the smallest amount amount of region. Although it is as well the slowest with the latency comparative.

Example 1: (1011 ×1101) = 10001111

```
      1 0 1 1
      1 1 0 1 ×
      1 0 1 1
    0 0 0 0     ——→ Left Shift by 1 bit
  1 0 1 1       ——→ Left Shift by 2 bit
1 0 1 1         ——→ Left Shift by 3 bit
-----------------
1 0 0 0 1 1 1 1
```

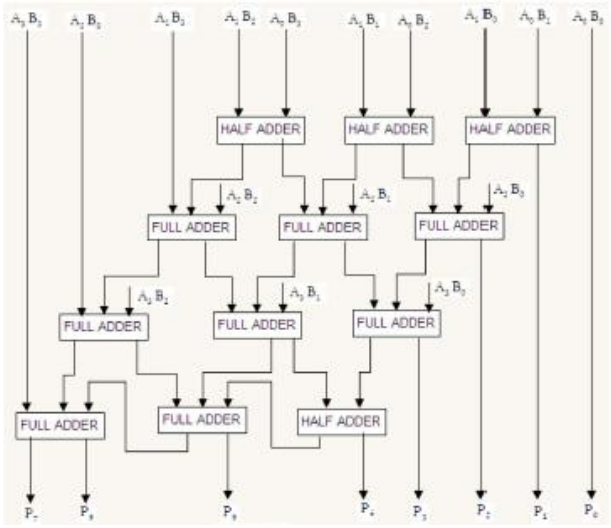
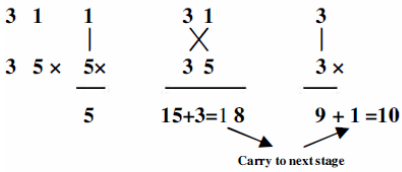


Figure 1. Array Multiplier using CSA Hardware Architecture

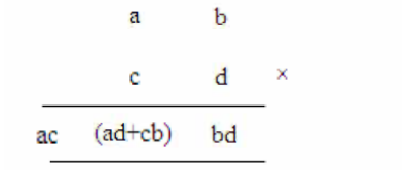
III. TIRYAKBHYAMA MULTIPLIER

Tiryakbhyam (upright and diagonally), is one of Sixteen Vedic Rules and transaction among the increase of numbers. The Rule is illustrate in Example 2 and the hardware planning is represent . In this case two decimal numbers (31 x 35) are increase. Procession plan for the development of two, three and four numeral numbers is shown using Tiryakbhyam Method. The digit on the two split ends of the line are reproduce and the outcome is additional with the earlier hold. what time three or more appearance are near, all the consequences are additional to the earlier hold. The smallest amount considerable numerals of the digit thus attain act as single of the effect digit and the relax act as the carry for the after that step. originally the carry is in use to be zero.

Example 2: 31 × 35 = 1085



Answer: 31 × 35 = 1085



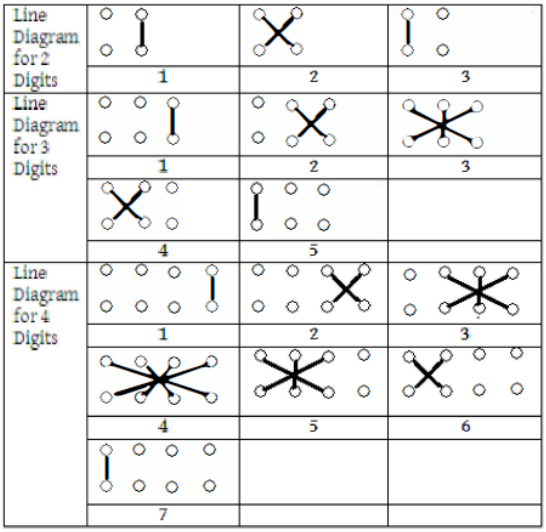


Figure 2. Line Diagram for Urdhava Multiplication

The above consideration know how to nowadays be extensive to reproduction of binary number system with the beginning familiarity that the development of two bits aa and ba is immediately an AND procedure and can be execute utilize easy AND gate. To demonstrate this development proposal in binary number system, judge the reproduction of two binary numbers a3a2al aa and b3b2bl ba. As the effect of this increase would be extra than 4 bits, the produce is uttered as r7r6rSr4r3r2rlra. Smallest amount momentous bit ra is obtain by reproduce the least significant bits of the multiplicand and the multiplier as shown.

$$r_0 = a_0b_0 \quad \dots (1)$$
$$c_1r_1 = a_1b_0 + a_0b_1 \quad \dots (2)$$
$$c_2r_2 = c_1 + a_2b_0 + a_1b_1 + a_0b_2 \quad \dots (3)$$
$$c_3r_3 = c_2 + a_3b_0 + a_2b_1 + a_1b_2 + a_0b_3 \quad \dots (4)$$
$$c_4r_4 = c_3 + a_3b_1 + a_2b_2 + a_1b_3 \quad \dots (5)$$
$$c_5r_5 = c_4 + a_3b_2 + a_2b_3 \quad \dots (6)$$
$$c_6r_6 = c_5 + a_3b_3 \quad \dots (7)$$

The digits on both sides of the procession are multiplied and supplementary with the hold from the earlier pace. This generate one of the bits of the consequence (rn) and a bring (Cn). This bring is additional in the subsequently stride and consequently the procedure going on. If extra than one procession are there in one stair, the complete product are spare to the preceding carry. In equally step, slightest central bit acts as the consequence bit and the extra entire bits act as carry. For example, if in a few middle step, we get 110, after that 0 will proceed as consequence bit and 11 as the hold. It must be plainly eminent to Cn could be a multi-bit number.

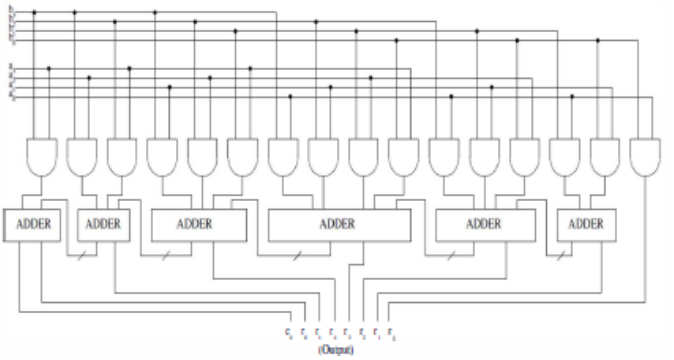


Figure 3. Urdhava Multiplier Hardware Architecture

The major benefit of the DVM(A New Multiplier Architecture with Two Variables) shoot from the fact that it can be simply execute in DVM due to its minimalism and reliability . The digital hardware awareness of a 4-bit multiplier utilize this Sutra is shown. This hardware propose is extremely parallel to that of the collection multiplier somewhere an range of adders is necessary to disembark at the concluding creation. Here in DVM, all the incomplete goods are designed in similar and the postponement connected is mostly the time full by the bring to spread during the adders.

IV. PROPOSED METHOD

The expected scheme is support on ROM come up to though equally the effort for the multiplier knows how to be variables. In this expected method a ROM is utilize for amass the quadrangle of statistics as evaluate to KCM wherever the multiples are store.

Technique: To discover (a x b), primary we contain to discover whether the distinction connecting 'a' and 'b' is odd or even. base on the dissimilarity, the creation is designed utilize

i. In container of yet dissimilarity

Outcome of development= [standard] ^{2}- [difference]^2

ii. In container of Odd dissimilarity

Outcome of reproduction = [standard x (standard + [departure (departure+ I)]

Where, standard = [(a+b)/2] and departure = [standard least (a,b)]

Example 3 (flat disparity and Example 4 (strange disparity) show the multiplication method. therefore the two variable growth is do by averaging, square and calculation. To discover the standard [(a+b)/2], which involve partition by 2 is perform by right variable the addition by one bit. If the square of the statistics are accumulate in a ROM, the outcome can be immediately considered. Though, in container of strange dissimilarity, the method is dissimilar as the standard is a balanced summit number. In order to feel balanced tip mathematics, Ekadikena Purvena - the Vedic Rules which is utilize to discover the quadrangle of numbers ending with 5 is functional. Example 5 demonstrates this. In this container, as a substitute of square the standard and departure, [standard x (standard + 1)] - [departure x (departure+ I)] is utilize. Though, as an alternative of performing arts the multiplications, the same ROM is utilize and apply equation (10) the outcome of multiplication is achieve.

$$n(n+l) = (n^2 + n) \ldots$$

now n^2 is obtain from the ROM and is additional with the attend to which is equivalent to n(n+l). The example ROM inside are known

Table 1. ROM Contents

Address	Memory Content (Square)
1	1
2	4
3	9
4	16
…	…

Therefore, separation and increase operation are efficiently transformed to calculation and adding process utilize Vedic Maths. quadrangle of both standard and departure is convert out concurrently by utilize a two port recollection to condense recollection contact moment.

Represent the RTL outlook of the projected multiplier for 4x4 as a example casing, execute on a typhoon II machine. SxS multiplier is execute utilize ROM come near, by accumulate the square of the numbers in the recollection preliminary from 0000 0000 to 1111 1111. The recollection prerequisite for an SxS development will be SKB. However in the container of 16 xl6 multiplier the recollection obligation will be massive, 216 x 32 = 2MB. Therefore, in classify to decrease the recollection necessities for advanced classify bit multiplication, lesser classify (SxS) multiplier can be instantiated. Through this method the limitations of bigger recollection necessities know how to be beat.

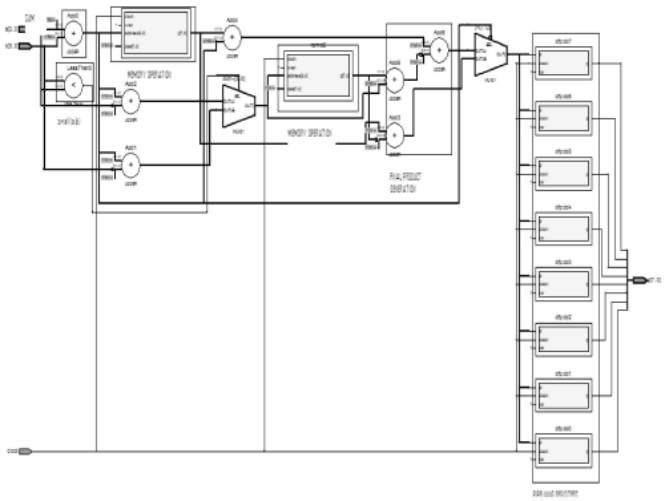


Figure 4. RTL view of Proposed Multiplier

V. EXPERIMENTAL RESULTS

It is conditional that the projected multiplier is most excellent suitable for top classify bit development (i.e., more than SxS). Because in FPGA there is enough quantity of on chip recollection, which can be utilize to amass the quadrangle of the numbers, the projected multiplier will utilize simply less reason fundamentals for its realization.

Table 2. Results for 8X8 Multiplier

Criterion	Array Multiplier	Urdhava Multiplier	Proposed Multiplier
Area			
Total Combinational Functions	163	149	114
Dedicated Logic Registers	48	48	16
Total Memory Bits(Kb)	0	0	8
Transitions	1557	1501	1782
Speed(After Pipelining)(MHz)	137.46	142. 67	129.52
Power			

Table 3. Results for 16X16 multiplier

Criterion	Array Multiplier	Urdhava Multiplier	Proposed Multiplier
Area			
Total Combinational Functions	738	694	291
Dedicated Logic Registers	96	96	48
Total Memory Bits(Kb)	0	0	16
Transitions	3173	3084	5341
Speed(After Pipelining)(MHz)	77.65	80.23	119.76
Power			
Static Power(mW)	46.20	46.19	46.17
Dynamic Power(mW)	4.41	3.61	9.57
I/O Power(mW)	17.37	17.34	17.41

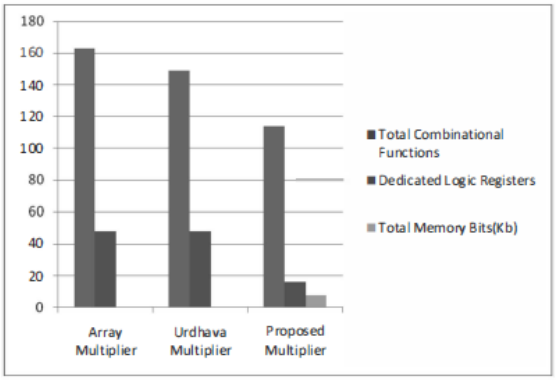


Figure 5a. Area Comparison for 8x8

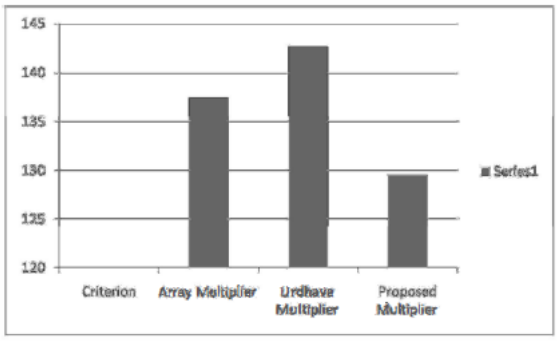


Figure 5b. Speed Comparison 8x8

VI. Conclusion

Thus the projected multipliers offer advanced presentation for elevated arranges bit enlarge. In the future multiplier for advanced order bit increases i.e. for 32x32 and extra, the multiplier is comprehend by instantiating the lesser regulate bit multipliers similar to 16x16. This is primarily suitable to memory control. Successful recall performance and consumption of memory firmness algorithms can capitulate even improved outcome.

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