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An Efficient Test Data Compression Using Viterbi Algorithm

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Abstract-This paper presents An Efficient Test Data Compression Using Viterbi Algorithm that provides high encoding efficiency and scalability with respect to the number of test channels. Proposed numerous test vector compression technique is linear decompression is used for simplicity high encoding efficiency. The proposed viterbi decompressor goal is produced large amount of output using small volume of inputs. Viterbi encoder is a good decompressor its used for increase the no of outputs. Experimental results are observed on Xilinx based simulator "Isim" wave forms and compared to previous test data compression architectures. Using Verilog and tool used is Xilinx ISE12.1 software.

Index Terms- Logic test, low-power test, on-chip decompressor, scalability, test data compression.

I. INTRODUCTION

Proposed numerous test vector compression technique is linear decompression is used for simplicity high encoding efficiency. Compression architectures are classified into three types are namely

1. Code based
2. Linear decompression
3. Broad cast scan

Linear compression is popular for simplicity and high encoding efficiency. Linear decompressor produced output of set of compressed test vectors in random. Effects on the compressed, requirements.

- Reducing high power consumption
- Not providing the systematic methodology to trade off compressions

This technique is used successful linear decompressor mainly combinational linear expansion or use linear feedback shift register (LFSR) implemented by XOR gates. Linear decompressed text vectors can be obtained by ATPG having solving linear equations. Output response comparator can be designed by using lossy algorithm which having multiple input signatures registers (MISR).

Viterbi algorithm is a dynamic programming technique and has time complexity O ($l \cdot 2^F$).

l = length of input sequence, F= number of flip flops
l is a linear function proposed algorithm generates compressed text vector quickly even for large circuits. F is determined by target compression ratio. The proposed viterbi algorithm validates whether a compacted test cube can be compressed.
Compression algorithm works in incremental mode. The number of specified bits in a test cube keeps increasing.

II. PROPOSED ARCHITECTURE

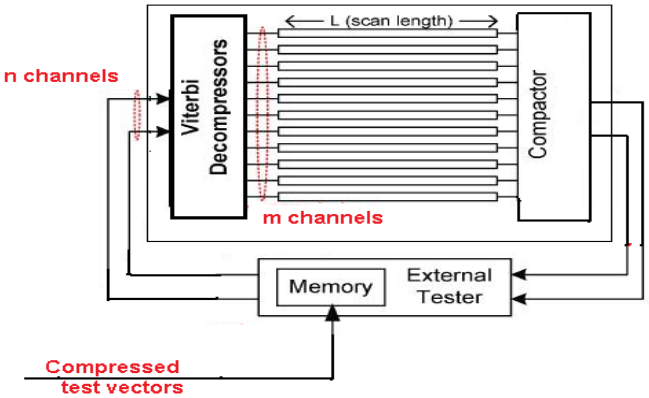


Figure-1: Proposed Architectures(reference [3])

Proposed architecture based on viterbi algorithms, which computes optimal state sequences in a hidden markove model Consists

1. Viterbi decompressed test vector
2. Memory
3. External tester
4. Decompressor
5. Scan path units
6. Compactor

At every clock cycles viterbi decompressor accepts nbits from external test vectors, apply mbits into internal scan chain (m>>n). Scan length = L. then (L x n) bits are stored in external testers instead of (L x m) bits.
After completing scan length that are given to compactor. Compactor is used to reduce the scan length. Finally, external tester value is equal to compactor output, then compression is successfully completed, output is 1 otherwise 0.

III. DECOMPRESSOR

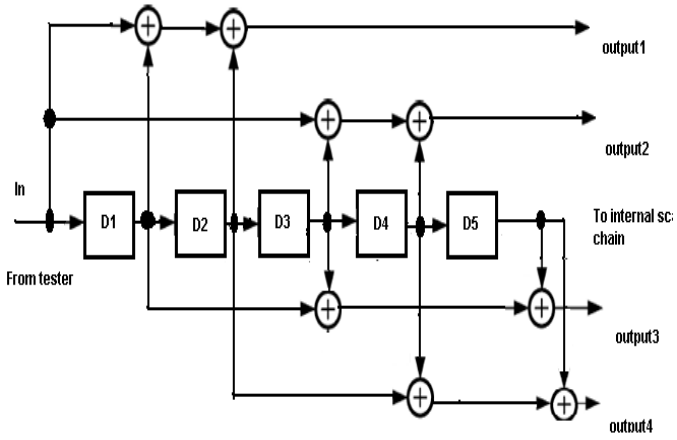


Figure-2: Decompressor

Viterbi de compressor goal is produced large amount of output using small volume of inputs. Viterbi encoder is a good decompressor. Its increase the number of outputs. Viterbi decompressor consists

1. Branch metric unit
2. Path metric unit
3. Trace back unit

Branch metric unit: It also calculates the hamming distances (i.e branch metric) between the received symbol and expected symbol.

Path metric unit: the path metric which is the minimum cost of arriving at a certain state. This stores the partial path metric of each state at the current state.

Trace back unit: All the path metrics for all the states are calculated from the first time index to the final time index.

Survivor path A survivor path assigned to this state (of the minimum path metric) indicates one state at the time index of (L+1). Viterbi architecture selects one state of the minimum path metric at the final time index.(L+2).

Viterbi decoder calculates a semi-brute form estimate of the likelihood for each path through the trellis. Four basic steps are:

1. Calculate the trellis
   a) Weight the trellis branches by calculating branch metrics.
   b) Compute minimum weight path to time n+1 in terms of the minimum weight path to time n. Uses add compare select(ACS) algorithm.
2. Find the last state of the minimum weight path.
3. Find the entire minimum weight path, is called survivor path decoder or trace back.
4. Reorder bits into correct forward ordering.

IV. SCAN PATH

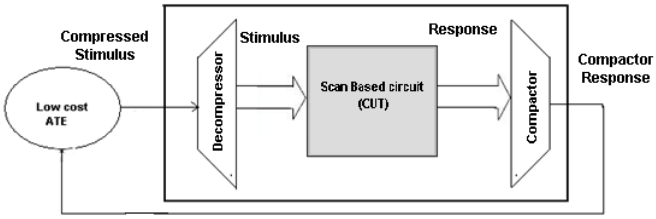


Figure-3: Scan path

A. TEST STIMULUS COMPRESSION

A test cube is defined as a deterministic test vector in which the bits that are not assigned value by the ATPG procedure are left as "don't cares" (X's). Normally, ATPG procedures perform random fill, in which all the X's in the test cubes are filled randomly with 1's and 0's to create fully specified test vectors. However, for test stimulus compression, random fill is not performed during ATPG so the resulting test set consists of incompletely specified test cubes. The X's make the test cubes much easier to compress than fully specified test vectors. Test stimulus compression should be an information lossless procedure with respect to the specified (care) bits in order to preserve the fault coverage of the original test cubes.
After deompression the resulting test patterns shifted into the scan chains should match the original test cubes in all specified (care) bits. Many schemes for compressing test cubes have been proposed.

B. TEST RESPONSE COMPRESSION

Test response compaction is performed at the outputs of the scan chains. The purpose is to reduce the amount of test response that must be transferred back to the tester. While test stimulus compression must be lossless, test response compaction can be lossy. A large number of different test response compaction schemes have been presented and described to various extents in the literature.

Automatic test equipment (ATE) has limited speed, memory and I/O channels. The test data bandwidth between the tester and the chip, is relatively low and generally is a bottleneck with regard to how fast a chip can be tested.

Test data compression offers a promising solution for the problema of increasing test data volume. A test set circuit under test (CUT) is compressed to a much smaller data, which is stored in ATE memory.

C. SCAN CHAIN

It is a technique used in design for testing. Objective is to make testing easier by making way to set and observe every flip-flop in an IC.

Scan – In = input of scan chain

Scan – out = output of scan chain

In full scan mode usually each i/p drive only one chain and scan observe one as well.

Enable pin = 1, flip flops are connected into a long shift resgister.

Clock signal which is used for controlling all the flip flops in the chain during shift phase and the capture phase.

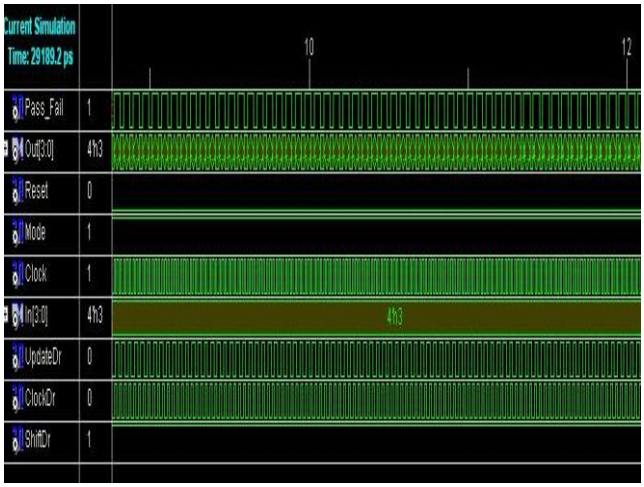
V. COMPACTOR

This compression schemes make use of MISRs (Multiple input signature registers) for the test response compressiion. There are disadvantages with MISRs. First, the usage of time saving aborto n fail testing is limited as the test result is known only at the end of the testing when the signature is produced. Second, diagnositc capabilities are reduced as it is difficult to determine where the fault is in DUT (device under test based on a faulty signature. And finally, when the unspecified bits in the test stimuli are defined, the expected test responses are defined after stimulation. Unfortunately, simulation cannot always determine all bits in the test responsed to 0 or 1. In this cases the responsed are simply unknown (X). A fault- free design may produce a 0 or 1 at such an X-position where both are correct, however it corrects the signature in the MISR. Several making approaches have been proposed; however they become test dependent and cannot guarantee masking all X's.

In order to address these problems, we propose a MISR free test compression scheme that supports abort-on-fail testing with termination at clock-cycle granularity and has good diagnostic capabilities. We propose a novel approach to test response compression and make use of a processor, placed on chip or at the ATE loadboard. The processor receives the compressed test data volumen from the ATE, decompresses and applies it to the DUT. The test evaluations is perfomed on chip by added test independent logic.

VI. FINAL OUTPUT RESULTS

Simulation Results



VII. CONCLUSION

In this paper, we proposed new and with the number of channels, linear compression scheme which is based on the viterbi algorithm defining proper branch metrics, path metric the proposed technique can include and optimise different test constraints, and selects, a set of compressed vectors that has minimum cost of function among all possible states. Limitations of proposed schemes

1. Scalable: number of test channel test is external scan input output port decompressor
2. Low pin count test becoming increasing important due to limited external data interface on a chip. If compression ratio increased it will need to increase the total number of test channels.

Proposed linear decompressor produce the output of set of test vectors in random effects on test compressed requirements resulting high power consumption. Not providing the systematic methodology to trade off compressions. Output response

compactor can be designed by using lossy algorithm which having multiple input signature registers(MISR)

VIII. REFERENCES

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