COMPARATIVE STUDY ON MCPWM STRATEGIES FOR 15 LEVEL ASYMMETRIC INVERTER

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Abstract—This paper focuses on a new topology of multilevel inverter with a reversing-voltage technique. This topology requires fewer components compared to conventional inverters and requires fewer carrier signals and gate drives. Multilevel inverter is triggered using Unipolar Sine Pulse Width Modulating (USPWM) strategies using sine reference and trapezoidal reference with triangular carriers. It include Phase Disposition (PD) strategy, Alternate Phase Opposition Disposition (APOD) strategy, Carrier Overlapping (CO) strategy and Variable Frequency (VF) strategy. The performance measures like Total Harmonic Distortion (THD), V RMS (fundamental), crest factor, form factor and distortion factor are evaluated for various modulation indices. Simulation is performed using MATLAB-SIMULINK.

Index Terms— APOD, CO, PD, VF, PWM.

I. INTRODUCTION


II. PROPOSED ASYMMETRICAL MULTILEVEL INVERTER

The proposed new asymmetric cascaded multilevel inverter is shown in Figure 1. inverter consists of 3 sub multilevel inverter and H bridge. Conversion cell consists of separate voltage sources(V1,V2,V3) connected in cascade and two active switching elements that can make the output voltage in positive polarity with several levels. H bridge consists of four active switching element that can make the output voltage in positive or in negative polarity depending on the switching condition. By
using $V_{dc}$, $2V_{dc}$ and $4V_{dc}$, it can synthesize 15 output levels: $-7V_{dc}$, $-6V_{dc}$, $-5V_{dc}$, $-4V_{dc}$, $-3V_{dc}$, $-2V_{dc}$, $0V_{dc}$, $2V_{dc}$, $3V_{dc}$, $4V_{dc}$, $5V_{dc}$, $6V_{dc}$, $7V_{dc}$. Expected output voltage level is given by

$$V_n=2^{n+1}-1,$$

Where $n=1,2,4…….$

III. MULTI CARRIER BASED PWM METHODS

In this proposed work a unipolar sine and trapezoidal reference with a triangular carrier is used to generate firing pulses for a 15 level inverter. For an $m$-level inverter using unipolar multi-carrier strategies, $(m-1)/2$ carriers with the same frequency $f_c$ and same peak-to-peak amplitude $A_c$ are used. The reference waveform has amplitude $A_m$ and frequency $f_m$ and it is placed at the zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off. There are many alternative strategies are possible, some of them are tried in this paper and they are:

a. Phase disposition PWM strategy (UPDPWM).

b. Alternate phase opposition disposition PWM strategy (UAPODPWM).

c. Carrier overlapping PWM strategy (UCOPPWM).

d. Variable frequency PWM strategy (UVFPWM).

The formulae to find the Amplitude of modulation indices are as follows:

For PDPWM, APDOPWM and VFPWM:

$$m_a=2A_m/(2A_c)$$

For COPPWM:

A. Unipolar Phase disposition PWM strategy (UPDPWM)

Fig. 2 and 3 shows the sinusoidal and trapezoidal pulse width modulation of an m-level inverter, $(m-1)$ carriers with the same frequency $f_c$ and same amplitude $A_c$ are positioned such that the bands they occupy are contiguous. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off.

B. Unipolar Alternate phase opposition disposition PWM strategy (UAPODPWM)

In UAPOD strategy the carriers of same amplitude are phase displaced from each other by 180 degrees alternately. The carrier arrangement of sinusoidal references and trapezoidal reference are illustrated in figures 4 and 5 respectively.
C. Unipolar Carrier overlapping PWM strategy (UCOPWM)

In UCOPWM strategy, carriers with the same frequency $f_c$ and same peak-to-peak amplitude $A_c$ are disposed such that the bands they occupy are overlap each other; the overlapping vertical distance between each carrier is $A_c/2$. The carrier arrangement of sinusoidal references and trapezoidal reference are illustrated in figures 6 and 7 respectively.

D. Unipolar Variable frequency PWM strategy (UVFPWM)

The number of switching’s for upper and lower devices of chosen MLI is much more than that of intermediate switches in PWM using constant frequency carriers. In order to equalize the number of switching’s for all the switches, variable frequency PWM strategy is used as illustrated in Fig.8 and 9 in which the carrier frequency of the intermediate switches is properly increased to balance the number of switching’s for all the switches.
IV. SIMULATION RESULT

The single phase binary DC source 15 level inverter is modeled in SIMULINK using power system block set. Switching signals for binary multilevel inverter using USPWM strategies are simulated. Fig.10 (a) and (b) respectively shows the 15 level output voltage generated by UPDPWM strategies with sinusoidal reference and its FFT plot. Fig .11 (a) and (b) respectively shows the 15 level output voltage generated by UPDPWM strategies with trapezoidal reference and its FFT plot. Fig .12 (a) and (b) respectively shows the 15 level output voltage generated by UAPODPWM strategies with sinusoidal reference and its FFT plot. Fig .13 (a) and (b) respectively shows the 15 level output voltage generated by UAPDPWM strategies with trapezoidal reference and its FFT plot. Fig.14 (a) and (b) respectively shows the 15 level output voltage generated by UCOPPWM strategies with sinusoidal reference and its FFT plot. Fig .15 (a) and (b) respectively shows the 15 level output voltage generated by UCOPPWM strategies with trapezoidal reference and its FFT plot. Fig .16 (a) and (b) respectively shows the 15 level output voltage generated by UVFPWM strategies with sinusoidal reference and its FFT plot. Fig .17 (a) and (b) respectively shows the 15 level output voltage generated by UCOPPWM strategies with trapezoidal reference and its FFT plot. Simulations were performed for different values of \( m_a \) ranging from 0.8 to 1 and the corresponding %THD are measured using the FFT block and their values are shown in Table I. Table II represents the \( V_{RMS} \) of the inverter output voltage. Table III represents the crest factor of the output voltage. Table IV and V represents the form factor and distortion factor of the output voltage. For \( m_a = 0.9 \), it is observed from the figures[10b 11b 12b 13b 14b 15b 16b 17b] the harmonic energy is dominant in:10b) 39th order in UPDPWM strategy with sinusoidal reference and triangular carrier.11b) 5th, 7th, 37th, 39th order in UPDPWM strategy with trapezoidal reference.12b) 39th order in UAPODPWM strategy with sinusoidal reference and triangular carrier.13b) 5th, 7th, 19th, order in UAPDPWM strategy with trapezoidal reference.14b) 38th, 39th, order in UCOPPWM strategy with sinusoidal reference and triangular carrier.15b) 5th, 37th, 39th order in UCOPPWM strategy with trapezoidal reference.16b) 19th, 31st, 33th, 37th, 39th order in UVFPWM strategy with sinusoidal reference and triangular carrier.17b) 5th, 39th, order in UVFPWM strategy with trapezoidal reference. The following parameter values are used for simulation:

\[ V_{dc} = 21.5 \text{V}, \ R \text{ (load)} = 100 \text{ohms}, \ f_c = 2000 \text{Hz} \text{ and } f_m = 50 \text{Hz}. \]
Fig 12 (a): Output voltage generated by UAPODPWM strategy with sinusoidal reference

Fig 12 (b): FFT plot for output voltage of UAPODPWM strategy with sinusoidal reference

Fig 13 (a): Output voltage generated by UAPODPWM strategy with trapezoidal reference

Fig 13 (b): FFT plot for output voltage of UAPODPWM strategy with trapezoidal reference

Fig 14 (a): Output voltage generated by UCOPWM strategy with sinusoidal reference

Fig 14 (b): FFT plot for output voltage of UCOPWM strategy with sinusoidal reference

Fig 15 (a): Output voltage generated by UCOPWM strategy with trapezoidal reference

Fig 15 (b): FFT plot for output voltage of UCOPWM strategy with trapezoidal reference
Fig 16 (a): Output voltage generated by UVFPWM strategy with sinusoidal reference

Fig 16 (b): FFT plot for output voltage of UVFPWM strategy with sinusoidal reference

Fig 17 (a): Output voltage generated by UVFPWM strategy with trapezoidal reference

Fig 17 (b): FFT plot for output voltage of UVFPWM strategy with trapezoidal reference

### TABLE I. %THD FOR DIFFERENT MODULATION INDICES

<table>
<thead>
<tr>
<th>m_a</th>
<th>UPDPWM Sine Ref.</th>
<th>UPDPWM Trapezoidal Ref.</th>
<th>UAPODPWM Sine Ref.</th>
<th>UAPODPWM Trapezoidal Ref.</th>
<th>UCOPWM Sine Ref.</th>
<th>UCOPWM Trapezoidal Ref.</th>
<th>UVFPWM Sine Ref.</th>
<th>UVFPWM Trapezoidal Ref.</th>
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### TABLE II. V_{RMS} FOR DIFFERENT MODULATION INDICES

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<th>m_a</th>
<th>UPDPWM Sine Ref.</th>
<th>UPDPWM Trapezoidal Ref.</th>
<th>UAPODPWM Sine Ref.</th>
<th>UAPODPWM Trapezoidal Ref.</th>
<th>UCOPWM Sine Ref.</th>
<th>UCOPWM Trapezoidal Ref.</th>
<th>UVFPWM Sine Ref.</th>
<th>UVFPWM Trapezoidal Ref.</th>
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<tr>
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<td>105.1</td>
<td>101.1</td>
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### TABLE III. CF FOR DIFFERENT MODULATION INDICES

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<tr>
<th>m_a</th>
<th>UPDPWM Sine Ref.</th>
<th>UPDPWM Trapezoidal Ref.</th>
<th>UAPODPWM Sine Ref.</th>
<th>UAPODPWM Trapezoidal Ref.</th>
<th>UCOPWM Sine Ref.</th>
<th>UCOPWM Trapezoidal Ref.</th>
<th>UVFPWM Sine Ref.</th>
<th>UVFPWM Trapezoidal Ref.</th>
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TABLE IV. FORM FACTOR FOR DIFFERENT MODULATION INDICES

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<th>UCOPWM</th>
<th>UVFPWM</th>
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TABLE V. DISTORTION FACTOR FOR DIFFERENT MODULATION INDICES

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<th>m_a</th>
<th>UPDPWM</th>
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<th>UCOPWM</th>
<th>UVFPWM</th>
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V. CONCLUSION

In this paper, USPWM techniques for binary DC source 15 level inverter have been presented. Binary DC source multilevel inverter gives higher output voltage with reduced switch count and low harmonics. Performance factors like %THD, \( V_{\text{RMS}} \), CF, FF and DF have been evaluated presented and analyzed. It is found that the UVFPWM strategy with sinusoidal reference provides relatively lower %THD, UCOPWM strategy with trapezoidal reference is found to perform relatively higher fundamental RMS output voltage. CF is almost same for all the strategies. FF is almost same for all the strategies. DF relatively low in UPDPWM strategy with sinusoidal reference.

REFERENCES


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