INVESTIGATION ON SINGLE PHASE ASYMMETRIC REDUCED SWITCH INVERTER WITH HYBRID PWM TECHNIQUES

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***Abstract*--This paper intends a new topology of an asymmetrical multilevel inverter with reduced switch count. Unipolar Hybrid Pulse Width Modulation (UHPWM) techniques are used to trigger the proposed Multilevel Inverter. It includes Alternative Phase Opposition Disposition (APOD) technique, Carrier Overlapping (CO) technique, Phase Disposition (PD) technique and Variable Frequency (VF) technique. The Performances measure like, Crest Factor (CF), Distortion Factor (DF), Form Factor (FF), Fundamental V_{RMS} and Total Harmonic Distortion (THD) are estimated for various modulation indices. Simulation is performed by using MATLAB-SIMUINK. It is observed that UVF technique provide lower THD, UCO technique provide higher fundamental V_{RMS} output voltage and higher Form Factor then UPD technique provide lower Distortion Factor.**

Index Terms: **APOD, CO, PD, PWM, UHPWM, VF.**

I. INTRODUCTION

Multilevel Inverters are developed to minimizing the switching stress and to obtain the required output voltage with multiple steps to achieve reduced total harmonic distortion (THD) and higher fundamental V_{RMS}. Multilevel inverter has become more familiar over the years in high voltage and high power electric applications without the use of a transformer. Anshuman et al [1] represented flying-capacitor-based chopper circuit for dc capacitor voltage balancing in diode-clamped multilevel inverter. Caballero et al [2] introduced symmetrical hybrid multilevel dc–ac converters with reduced number of insulated dc supplies. Mukherjee and Poddar [3] analyzed series-connected three-level inverter topology motor drive applications. Govindaraju and Baskaran [4] proposed efficient sequential switching hybrid-modulation techniques for cascaded multilevel inverters. Nami et al [5] made a comparison of a hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped h-bridge cells. Silva et al [6] developed a implementation and control of a hybrid multilevel converter with floating dc links for current waveform improvement. Cougo et al [7] represented pd modulation scheme for three-phase parallel multilevel inverters. Lee [8] introduced quantitative power quality and characteristic analysis of multilevel pulse width-modulation techniques for three-level neutral-point-clamped medium-voltage industrial drives. Rajeevan and Gopakumar [9] analyzed a hybrid five-level inverter with common-mode voltage elimination having single voltage source for IM drive applications. Maheswari et al [10] proposed design of neutral-point voltage controller of a three-level NPC inverter with small dc-link capacitors. Wang et al [11] represented neutral-point potential balancing of a five-level active neutral-point-clamped inverter. This paper proposed a single phase asymmetrical 7 level inverter using various UPWM switching

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techniques with Hybrid Reference. Simulations were developed using MATLAB SIMULINK.

II. PROPOSED SINGLE PHASE ASYMMETRIC MULTILEVEL INVERTER

Fig.1 represents a circuit configuration of a cascade two half H-bridge asymmetric multilevel inverter using binary DC input source. The seven level output are obtained by the series connected two half H-bridges with different voltage ratings. The output voltage of the first half H-bridge is taken by V_1 and the output of the second half H-bridge is taken by V_2. So that the total output voltage of the proposed inverter is the sum of the two voltages (V) i.e. V=. $V_1 + V_2$. The voltage of seven levels are $0V_{dc}$, V_{dc} $2V_{dc}$, $3V_{dc}$, $-V_{dc}$, $-2V_{dc}$, & $-3V_{dc}$. The switches S_1, S_2, S_3 and S_4 operate at the higher frequencies to get the positive polarity output. The switches A_1, A_2 and B_1 B_2 are operate at the normal frequency.

The output voltage level is calculated by the following formula,

$$V_n = 2^{n+1}\text{-}1,\ n = 1, 2, 4...$$

Where,

n= number of dc sources

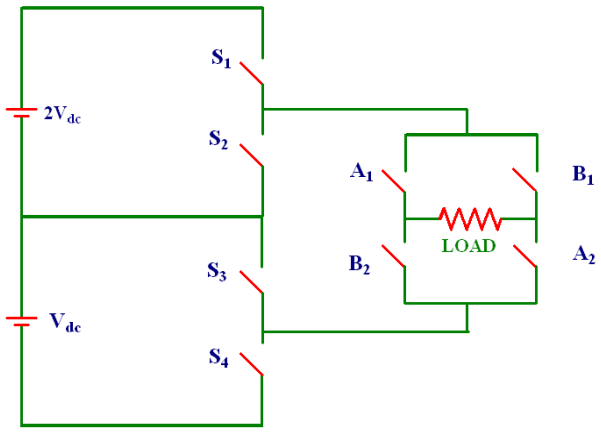

Fig 1: Circuit of 7 level asymmetrical MLI

III. UNIPOLAR PWM TECHNIQUES WITH HYBRID REFERENCE

In proposed work a unipolar hybrid reference ((sinusoidal + trapezoidal) i.e. the first half cycle should be sine reference and second half cycle should be trapezoidal reference) with triangle carrier is used to generate gate pulses for a 7 level proposed asymmetrical inverter. (m-1) /2 carriers are needed to the 'm' level output with the same frequency (f_c) and same peak to peak amplitude (A_c) are used. The hybrid reference waveform has amplitude A_m and frequency f_m and it is placed at the zero reference. The hybrid reference is sequentially compared with each of the triangle carrier. If the hybrid reference is more than a triangle carrier, then the devices corresponding to that carrier are turned on. Or else, the device switches off.

There are many alternative techniques are possible, some of them are developed in this paper and they are:

a. Unipolar Phase Disposition PWM technique (UPDPWM)
b. Unipolar Alternative Phase Opposition Disposition PWM technique (UAPODPWM)
c. Unipolar Carrier Overlapping PWM technique (UCOPWM)
d. Unipolar Variable Frequency PWM technique (UVFPWM)

The frequency ratio m_f is calculated by the following formula:

$$m_f = f_c / f_m$$

The formula for finding the amplitude modulation indices for UPD, UAPOD, UVF techniques as follows:

$$m_a = 2A_m / (m\text{-}1)A_c$$

The formula for finding the amplitude modulation indices for UCO technique as follow:

$$m_a = A_m / (2*A_c)$$

a. *Unipolar Phase Disposition PWM (UPDPWM) Technique*

The same frequency and same amplitude three carriers are in phase. The carrier arrangement for asymmetrical 7 level inverter is shown in figures 2.

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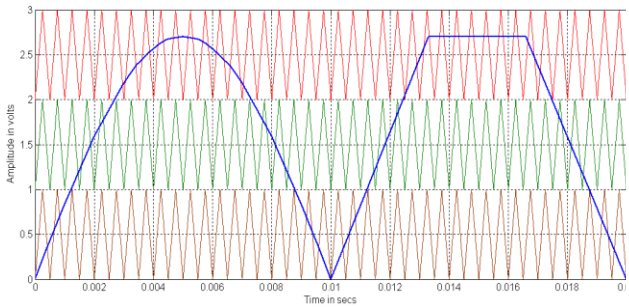

Fig 2: Carrier Arrangement for UPDPWM technique with hybrid PWM (m_a=0.9 and m_f=40)

b. *Unipolar Alternative Phase Opposition Disposition PWM (UAPODPWM) Technique*

In that same amplitude and same frequency three carriers is in out of phase with its neighbor by 180 degree. The carrier arrangement for asymmetrical 7 level inverter is shown in figures 3.

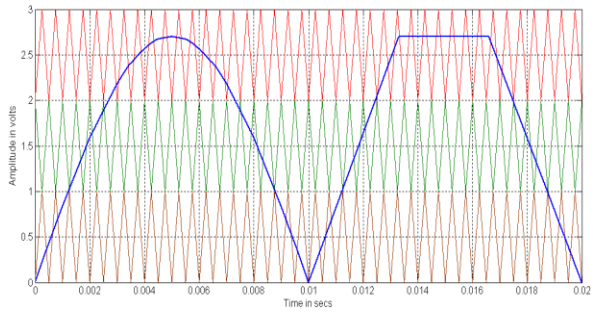

Fig 3: Carrier Arrangement for UAPODPWM technique with hybrid PWM (m_a=0.9 and m_f=40)

c. *Unipolar Carrier Overlapping PWM (UCOPWM) Technique*

In that the same frequency and same amplitude three carriers are to be overlap with each other. The overlapping should be vertical distance between each carrier is half the peak to peak amplitude (A_C/2). The carrier arrangement for asymmetrical 7 level inverter is shown in figures 4.

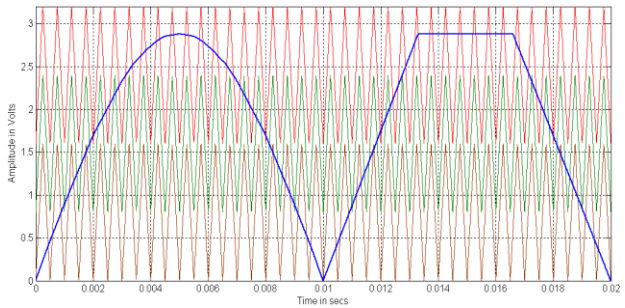

Fig 4: Carrier Arrangement for UCOPWM technique with hybrid PWM (m_a=0.9 and m_f=40)

d. *Unipolar Variable Frequency PWM (UVFPWM) Technique*

The number of switching for upper and lower devices of chosen MLI is more than that of middle switches in other PWM technique having constant frequency carriers. In order to equalize the number of switching for all the switches, variable frequency PWM strategy is used. The carrier arrangement for asymmetrical 7 level inverter is shown in figures 5.

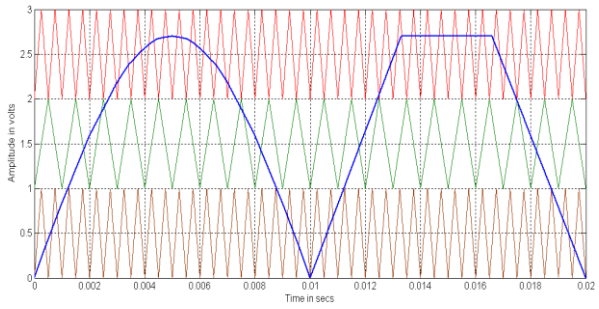

Fig 5: Carrier Arrangement for UVFPWM technique with hybrid PWM (m_a=0.9, m_{f1}=20, m_{f2}=40)

IV. SIMULATION RESULT

The simulation results are carried out for the proposed inverter by the MATLAB simulation software. Switching signals for proposed multilevel inverter using Unipolar Hybrid Pulse Width Modulation techniques are simulated. Fig. 6 and 6(a) respectively shows the seven level output voltage generated by UPD technique and its FFT plot. Next Fig. 7 and 7 (a) respectively shows the 7 level output generated by UAPOD technique and its FFT Plot. Then the Fig 8 and 8(a) represents the seven level output voltage

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generated by UCO technique and its FFT plot. Fig 9 and 9 (a) shows the seven level output created by UVF technique and its FFT plot. The following parameter values are used for simulation: V_{DC}=100, R (load) = 100, f_c=2000 Hz and f_m=50 Hz.

For m_a=0.9 it is observed from the figures [6(a), 7(a), 8(a), 9(a)] the harmonic energy is dominant in: Fig. 6(a): 27th and 39th orders in UPD technique. Fig. 7(a): 31st, 33rd, 37th and 39th orders in UAPOD technique. Fig. 8(a): 5th, 37th and 39th orders in UCO technique. Then Fig. 9(a):, 17th, 21st, 23rd, 27th, 33rd and 39th orders in UVF technique.

Simulations were carried out for different values of m_a ranging from 0.8 to 1 and the corresponding %THD is measured using the FFT block and their values are shown in the Table 1. Compare to all PWM techniques, UVFPWM technique provides low %THD. Table 2 shows the V_{RMS} of the proposed inverter output for the same modulation indices. In that UCOPWM technique provides higher fundamental RMS voltage. Table 3 and Table 4 shows respectively the corresponding Crest Factor (CF) and Form Factor (FF) of the proposed inverter output voltage. CF is almost same for all the PWM techniques. In that UCOPWM technique provides higher Form Factor (FF). Table 5 shows the Distortion Factor (DF) of the proposed inverter output voltage. In that UPDPWM technique provides less DF.

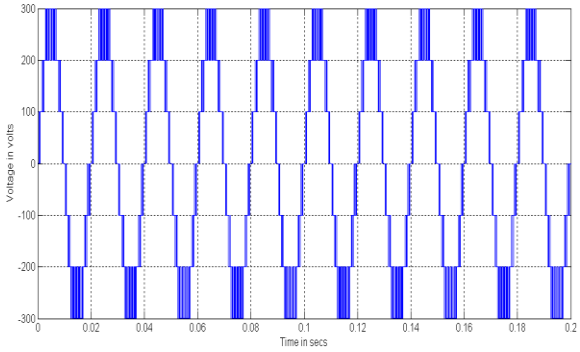

Fig 6: Output Voltage generated by UPD technique

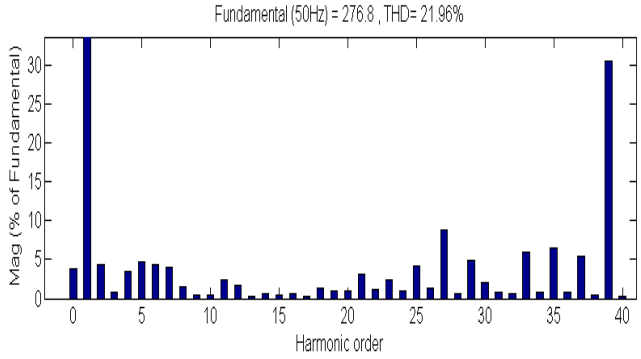

Fig 6(a): FFT Plot for output voltage of UPD technique

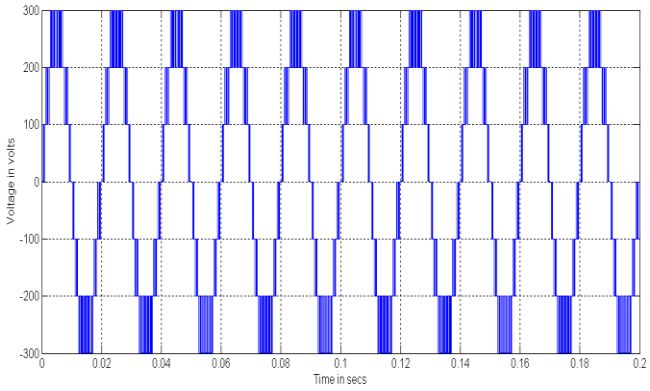

Fig 7: Output Voltage generated by UAPOD technique

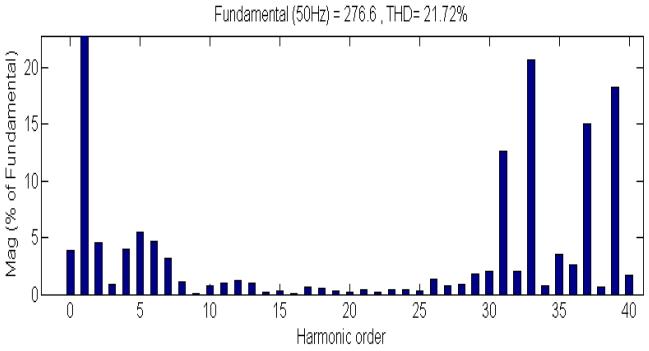

Fig 7(a): FFT Plot for output voltage of UAPOD technique

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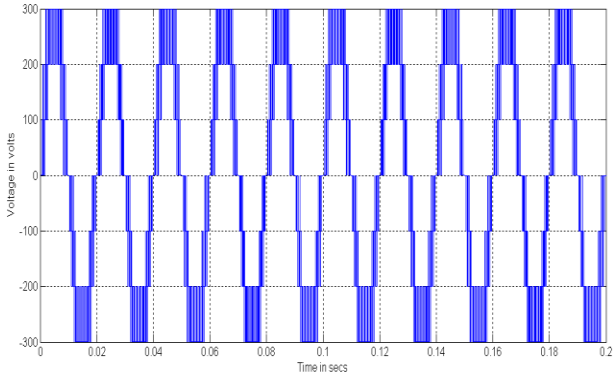

Fig 8: Output Voltage generated by UCO technique

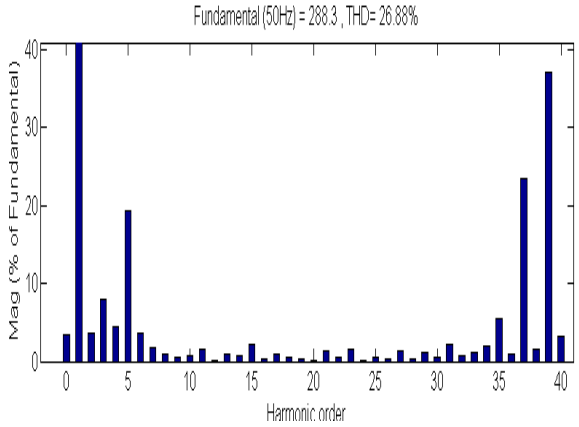

Fig 8(a): FFT Plot for output voltage of UCO technique

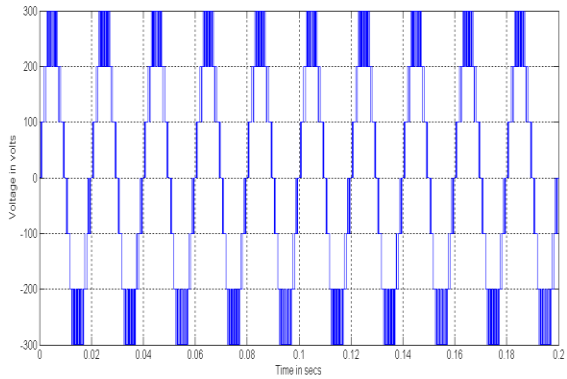

Fig 9: Output Voltage generated by UVF technique

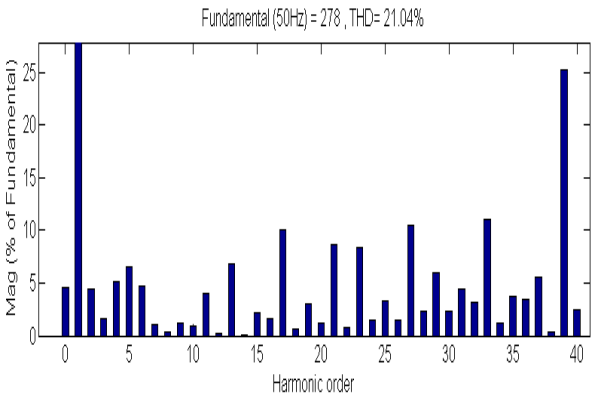

Fig 9(a): FFT Plot for output voltage of UVF technique

TABLE 1. %THD FOR DIFFERENT MODULATION INDICES

m_a	PD	APOD	CO	VF
1	16.70	17.05	22.09	15.67
0.95	19.78	19.62	24.54	18.42
0.9	21.95	21.69	26.92	21.05
0.85	23.63	23.47	29.22	23.55
0.8	24.54	24.65	31.44	25.02

TABLE 2. V_{RMS} FOR DIFFERENT MODULATION INDICES

m_a	UPD	UAPOD	UCO	UVF
1	217.5	217.2	221.7	217.2
0.95	206.5	206.6	213.1	207.2
0.9	195.7	195.7	203.8	196.5
0.85	184.9	184.8	193.8	185.1
0.8	174	174	184.2	173.9

TABLE 3. CREST FACTOR FOR DIFFERENT MODULATION INDICES

m_a	UPD	UAPOD	UCO	UVF
1	1.414253	1.414365	1.414073	1.414365
0.95	1.414528	1.414327	1.41389	1.414093
0.9	1.41441	1.413899	1.414132	1.414249
0.85	1.414819	1.413961	1.414345	1.414371
0.8	1.414368	1.413793	1.414224	1.414031

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TABLE 4. FORM FACTOR FOR DIFFERENT MODULATION INDICES

m_a	UPD	UAPOD	UCO	UVF
1	45.71248	47.873044	71.677983	50.629371
0.95	45.39459	49.927501	67.52218	48.844884
0.9	52.83477	49.444164	60.206795	44.187092
0.85	50.82462	50.272835	56.849516	43.676262
0.8	48.11946	51.011434	50.438116	48.292141

TABLE 5. DISTORTION FACTOR FOR DIFFERENT MODULATION INDICES

m_a	UPD	UAPOD	UCO	UVF
1	0.00424326	0.00443	0.003802	0.004391
0.95	0.0042199	0.00429	0.004161	0.004267
0.9	0.00412464	0.00433	0.005202	0.004325
0.85	0.00421586	0.00428	0.006561	0.004266
0.8	0.00430551	0.00426	0.007971	0.004164

V. CONCLUSION

In this paper, UHPWM techniques having binary DC source inverter have been presented. Binary DC source proposed inverter gives higher output voltage with reduced number of switches and low harmonics. Performance parameters like Crest Factor (CF), Distortion Factor (DF), Form Factor (FF), Fundamental V_{RMS} and Total Harmonic Distortion (%THD) have been estimated presented and analyzed. It is found that the UVFPWM technique, provides lower %THD. UCOPWM technique is found to perform better since it provides relatively higher fundamental RMS output voltage and higher Form Factor. UPDPWM technique provides less DF.

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