Low power sleep switch based domino logic circuit with voltage regulated static keeper

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Abstract— **Prevailing CMOS design practice has been very conservative with regard to choice of transistor threshold voltage, so as to avoid the difficult problems of threshold variations and high leakage currents. It is becoming necessary to scale threshold voltages more aggressively in order to obtain further power reduction, performance improvement, and integration density. Substantial leakage reduction can be achieved in single V_{th} designs by stacking low V_{th} transistors. When the transistors are stacked between power and ground rails, the resistance increases and power consumption is reduced. But there occurs reduction in enhancement of speed along with increase in area which degrades the performance of the circuit. Hence to simultaneously reduce power and to enhance speed a new sleep switch based VRSK keeper technique is proposed in which it optimizes both power consumption and speed. The performance of the proposed technique is compared with existing technique by performing transistor level simulations for benchmark circuits using Microwind 2 and DSCH2 CMOS layout CAD tools. The simulation result shows that PDP of the proposed technique is reduced by 96% with that of existing technique.**

Index Terms— **Power delay product, domino logic, stacking transistor, VRSK keeper.**

I. INTRODUCTION

The high performance microprocessor employs domino logic circuit because of its higher speed of operation. The domino logic involves the implementation of only the nMOS logic as compared to the static CMOS circuits which involves the implementation of both the nMOS and pMOS logic due to which there is colossal amount of reduction in the number of transistors in domino logic thus reducing the area of the circuit. The basic domino logic circuit is shown in Fig.1 in which C_L represents the parasitic capacitance and PDN represents the pull down network which realizes the logic function to be implemented. When the clock is low the circuit is in precharge phase and Qp is on and Qe is off [1]-[2]. The dynamic node precharge to V_{DD} and the output of the CMOS inverter is low. When clk =1 the circuit is in evaluation phase, Qe is on and Qp is off.

When the input combination result in logic '0' then the dynamic node stays charged and output is low. When the input combination results in logic '1' then the dynamic node discharges to ground and the output of the CMOS inverter is high. However these domino logic gates suffer from lesser noise immunity and higher power dissipation. As the technology scales down, the leakage current increases and plays a vital role in the total power dissipation. Since the dynamic power is given by P=CV^2 f, voltage must be limited to keep dynamic power within tolerable levels. However in order to meet the required conditions the threshold voltage (V_{th}) of the transistors must be reduced in order to compliment supply voltage scaling down, but this in turn result in exponential rise in the sub threshold leakage current.

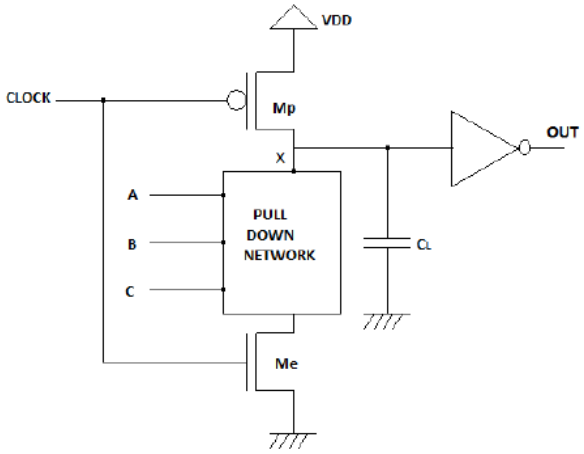

Fig.1. Basic domino logic circuit

Techniques such as the dual threshold voltage (DTV) which deploys high V_{th} and low V_{th} transistors are widely used in VLSI circuits to suppress the leakage current to reduce the total power dissipation. Dual threshold voltage-voltage scaling (DTVS) is a hybrid approach which incorporates both the DTV and the voltage scaling technique to gain an edge over the rudimentary DTV method. These techniques are discussed in section II of the literature. A novel stacked transistor–dual threshold voltage (ST-DTV) technique which incorporates the conventional DTV along with the stacked pMos and nMOS transistors are discussed in section III. Section IV proposes sleep switch based domino logic circuit with a detailed description. Section V comprises of the simulation results and Section VI offers the wholesome conclusion of the literature.

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II. SURVEY OF EXISTING SYSTEMS

A. Dual Threshold Voltage Technique

DTV is an efficient approach to quell the sub threshold leakage current in designing power efficient integrated circuits. The DTV technique deploys two types of transistors (a) high V_{th} transistors and (b) low V_{th} transistors. High- V_{th} devices can be used to reduce leakage currents while low- V_{th} devices can be used whenever high performance is required. The main principle of the technology is simply to partition a circuit into critical and noncritical regions and to use only fast low-V_{th} devices when necessary to meet performance goals. This approach will reduce sub threshold leakage currents in both active and standby mode.

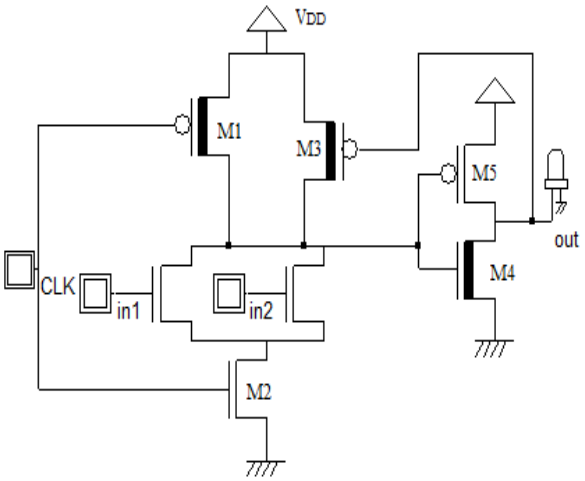

Fig.2. DTV Technique

In Fig. 2 the DTV is implemented as a 2 input OR gate. Transistors (M1, M3, M4) are high V_{th} transistors which are active during the precharge phase of the domino circuit. The transistors (IN1, IN2, M5, and M2) which are low V_{th} transistors are active during the evaluation phase [3]. When the clock is low M1 is on such that the dynamic node is precharged to V_{DD} which turns off M4 and the output of the pMOS inverter is low which as a result turns on M3. When the clock is set M1 is off and M2 is on and depending upon the logic combination, the evaluation node can stay high or can make a 1 to 0 transition. However, the circuit technique does not address energy and delay overhead for entering and leaving its standby mode.

B. *Stacked Transistor Dual Threshold Voltage Technique*

The transistor stack is a leakage reduction technique which works both in active and stand-by mode. It is based on the observation that two off-state transistors connected in series cause significantly less leakage than a single device. The leakage current of the stack is even smaller than the leakage of a single device with double channel length. The stacked transistor dual threshold voltage (ST – DTV) technique is shown in the Fig. 3. This technique deploys forced stacked approach which helps us to limit the leakage current by dissevering an existing transistor into two transistors as a result the W/L of each of the dissevered transistors is half as compared to the existing transistor[4] . In Fig. 3 M1 and M4 are the stacked such that (M1, M2) and (M3, M4) are two half size transistors. When the two dissevered transistors are switched off simultaneously, then the induced reverse bias between the two half divided transistors results in abatement of leakage current. But when the transistor stack is increased then the speed is reduced because the propagation delay is inversely proportional to the depth of the stack. Also when the depth of the stack is increased the circuit might fail due to charge sharing.

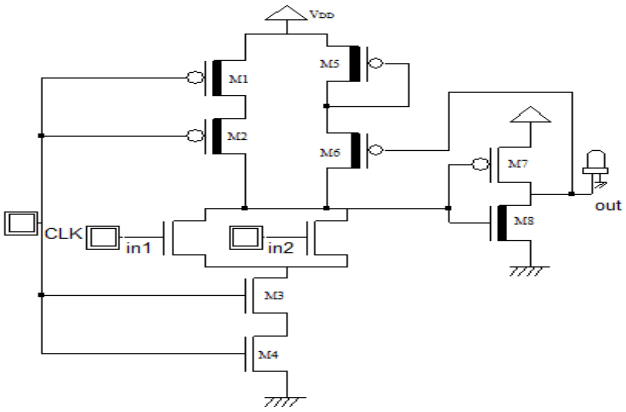

Fig.3. ST-DTV Technique

When clock is low the M1, M2 are on and M3, M4 are off as a result the evaluation node is precharged to VDD and the output of the CMOS inverter is low. During the evaluation phase the clock is high, stacked pMOS transistors are off and stacked nMOS transistors are on. Depending on the combination of the inputs in the pull down network the evaluation node can stay charged or can make a high to low transition[5]-[6]. This technique helps us to abate the sub threshold leakage current which results in reduced power consumption.

III. PROPOSED TECHNIQUE

A low energy and delay overhead circuit technique is proposed in this paper to lower the sub threshold leakage currents in an idle domino logic circuit. The circuit technique employs sleep switches to place a dual- V_{th} domino logic circuit into a low leakage state within a single clock cycle. A domino logic circuit based on the sleep switch dual- V_{th} circuit technique is shown in Fig.4. A high- V_{th} nMOS switch is added to the dynamic node of a domino circuit as shown in Fig. 4. The operation of this transistor is controlled by a separate sleep signal. During the active mode of operation, the sleep signal is set low, the sleep switch is cut-off, and the proposed dual- V_{th} circuit operates as a standard dual- V_{th} domino circuit. During the standby mode of operation, the clock signal is maintained high, turning off the high V_{th} transistors(M1,M3,M4,M6) of each domino gate. The sleep signal transitions high, turning on the sleep switch. The dynamic node of the domino gate is discharged through the sleep switch, thereby turning off the high- V_{th} nMOS transistor within the output inverter. The output transitions high, cutting off the high- V_{th} keeper. Following the low-to-high transition of the output of a sleep switch dual- V_{th} domino gate, the subsequent gates (fed by the noninverting signals) also evaluate and discharge in a domino fashion. After the node voltages settle to a steady

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state, all of the high- V_{th} transistors are strongly cut-off, significantly reducing the subthreshold leakage current. Note that this technique, requiring no additional gating on the input signals while strongly turning off all of the high- V_{th} transistors within a single clock cycle, is significantly more power, delay, and area efficient as compared to the techniques proposed.

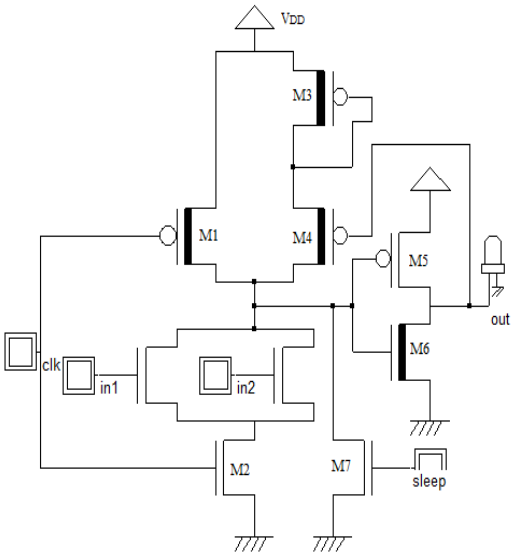

Fig .4. Sleep switch based domino circuit

This technique also incorporates a voltage regulated static keeper (VRSK) instead of a conventional pMOS keeper as shown in Fig. 6. In VRSK a self-biased M_p transistor is cascaded with the M_k transistor[7]. By using the conventional keeper circuit the contention effect occurs when the dynamic node is to be evaluated as logic '0' as the keeper and the pull down network are simultaneously on. By incorporating VRSK the transistor M_k has a lower supply voltage with a weaker strength resulting in lowering the contention effect.

IV. SIMULATION RESULTS & PERFORMANCE ANALYSIS

To assess the reduction in power offered by the above discussed circuit techniques, Domino logic gates were simulated according to the test circuit for the 45-nm technology and the following results are obtained.

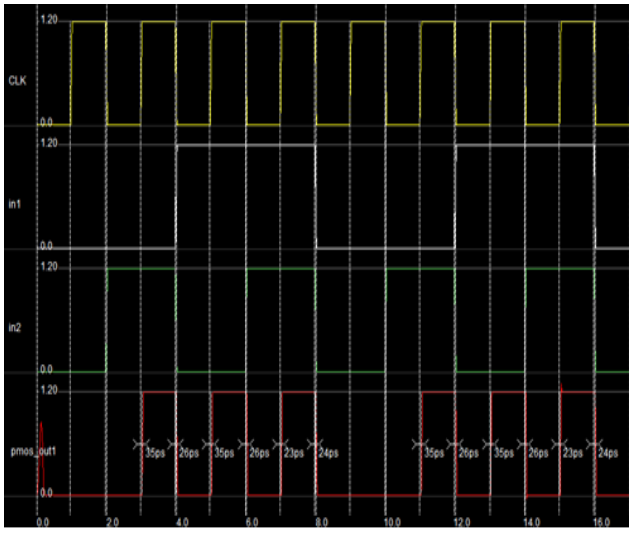

Fig.5. Output Waveform for DTV Technique

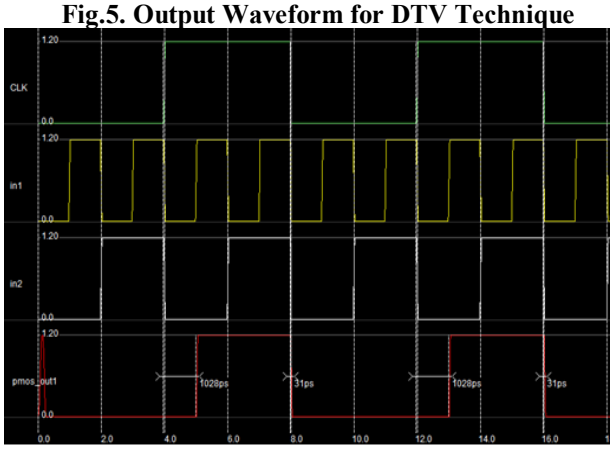

Fig.6. Output Waveform for STDTV Technique

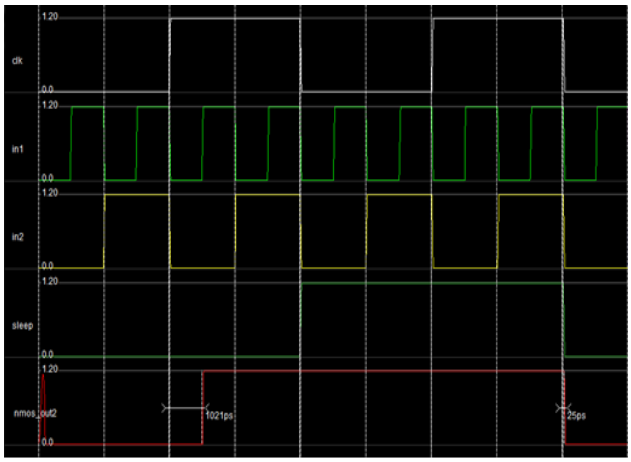

Fig.7. Output Waveform for Sleep Switch Based Domino Circuit

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Table -1: Optimum Values for 2 Inputs OR Gate.

Circuit techniques	Area (μm2)	Power (μW)	Delay (ns)	PDP (fJ)
DTV	93.7	12.785	0.630	8.054
ST-DTV	166.3	4.325	0.750	3.243
Sleep switch based circuit	134	0.142	0.700	0.099

From the table 1, it can be observed that the PDP has been reduced by 96% and area has been reduced by 19% for 2 input OR gate when compared with stacked transistor dual threshold technique. Also when comparing with dual threshold voltage technique, the proposed technique reduces power by 98%.

V. CONCLUSION

In deep submicron technology, power consumption must be reduced to increase the efficiency of the circuit. The proposed sleep switch based domino logic circuit can reduce power consumption. The various parameters like power, delay, area and PDP are calculated for 2 input OR gate using different circuit techniques in 45-nm technology. From the results it can be concluded that the proposed sleep switch based domino logic circuit shows good performance by offering reduction in power consumption when compared with various circuit techniques.

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