Design of Clocked Pair Shared Flip Flop Using low Power Techniques

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***Abstract*— In the past, the major issue of the VLSI designer were area, cost, performance, and reliability; power consideration was mostly of only inferior importance. But over the last few years power in the circuit is the major problem now days which is being faced by the very large scale integration industries. The power dissipation in any circuit is usually take place by the clocking system which includes the clock distribution system and sequential elements (flip flops and latches) in it. The amount of power dissipation by any clock distribution system and sequential circuit in any chip is about of 30% to 60% of the total chip power dissipation by the circuit. Clock is the most important signal present in the chip. Clock signals are synchronizing signals which provide timing references for computation of any work in synchronous digital systems. In this paper the power of the sequential circuit is reduced which in reference reduce the overall power of the chip. Here different low power techniques for the lowering static power dissipation are used in the sequential circuit are surveyed.**

***Index Terms*— Stack effect, Sleepy effect, Static power reduction, Low power.**

I. INTRODUCTION

In the past, the major importance's given by the VLSI designer were area, cost, performance and reliability; the field of power was mostly considered of only inferior importance. But in recent years, however, this is getting change and increasingly, power is being given similar importance same as the area and the speed. There are several factors which focus light towards the power factor of the chip or design. In high-speed implementation of any circuit and complex functionality applications with low power consumption of the circuit is of critical concern. The art of the power analysis and its optimization of the integrated circuits is very important in the chip designing procedure. The need of the low power chips and the system are driven importance by both in the business and the technical fields. There are generally four sources of power dissipation in digital CMOS circuits. They are: switching (or dynamic) power, short-circuit power, leakage power, and static power.

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These are summarized in the following

$$P_{avg} = P_{switching} + P_{short\ circuit} + P_{leakage} + P_{static} = \alpha C_L V_{dd}^2 f + I_{sc} V_{dd} + I_{leak} V_{dd} + I_{static} V_{dd}$$

The switching power $P_{switching}$ consists of the activity factor α, or the average number of transitions for a circuit node per clock cycle, the load capacitance C_L switched, and the power supply voltage V_{dd} which is mostly in the cases the voltage is always equal to the supply voltage ($V=V_{dd}$). The short-circuit power is controlled by the current that flows between V_{dd} and ground I_{sc}. This current flows in static CMOS logic when both the P_{pullup} and $N_{pulldown}$ networks are on simultaneously during an output transition. I_{leak} the main component of the leakage power is current due to leakage through reverse-biased PN junctions and sub threshold conduction of MOSFETs. Finally, static power is due to designed current sources, like biasing networks for linear amplifiers, whose current sums to I_{static}.

Here clocking system is the main point in the chip configuration [1]. The clock network constitutes one of the most important segments of a synchronous VLSI chip as it can significantly influence the speed, area, and power dissipation of the system. The carefully design of the clocking system is generally a neglected in the design process. The reason of this is that the older chip had higher tolerance to the change in the clock signal and had less execution timing requirements. However with the increase in the demand of the high speed operation the design of the clocking system has being very important concern in the chip. The system timing specifications are executed using clocking system.

There are large numbers of methods available to reduce the energy and power consumption of a chip in a circuit. There are many approaches which focus on circuit and its application specific techniques, There are techniques for power reduction that are non-application specific, which includes widely popular techniques such as voltage scaling, frequency scaling and leakage power reduction [2]. Voltage scaling combined with frequency scaling is very popular because reducing the supply voltage of a CMOS circuit lowers the active and leakage power polynomials, while only reducing the frequency linearly. The dynamic power loss has been dominant culprit in the past, static power loss has become a considerable contributor to power consumption in nanoscale technologies due to leakage currents. One of the main causes of static power loss is leakage currents. There are wide varieties of techniques designed to reduce leakage currents as the power dissipation by this has become one of

the most dominant factors in total power consumption and is a challenge for the VLSI designers.

II. Survey of Low Power Clocking System

Flip-Flops are the basic elements for storing data and they are the fundamental building blocks for all sequential circuits. In Flip-flops their content change only either at the rising or at falling edge of the enable signal. But, after the rising or falling edge of the enable signal, the flip-flop's content remains constant even if the input data changes. The part of the clock energy is consumed by the internal clock buffer to control the transmission gates unnecessarily. CDFF and CCFF both have large clocked transistors. For example, CDFF used 15 clocked loads and CCFF used 14 clocked transistors. In respect to this, conditional data mapping flip-flop used only 7 clocked transistors, which resulting in about 50% reduction in the number of clocked transistors load, so due to this CDMFF used less power than CCFF and CDFF. This result illustrate that the by reducing clocked loads numbers help in achieving low power. Since CDMFF is better in performance than CCFF and CDFF in respect of power consumption [3].

CDMFF ha less number of clocked loads but it has redundant clocking in it and it has floating node as a drawback. To result in efficient and error free implementation of low power register element, a Clocked Pair Shared flip-flop (CPSFF) is proposed. In this circuit of clocked-pair-shared flip-flop, a clocked pair (N3, N4) is shared by first and second stage of the latching part as which is shown in figure 1 below [4].

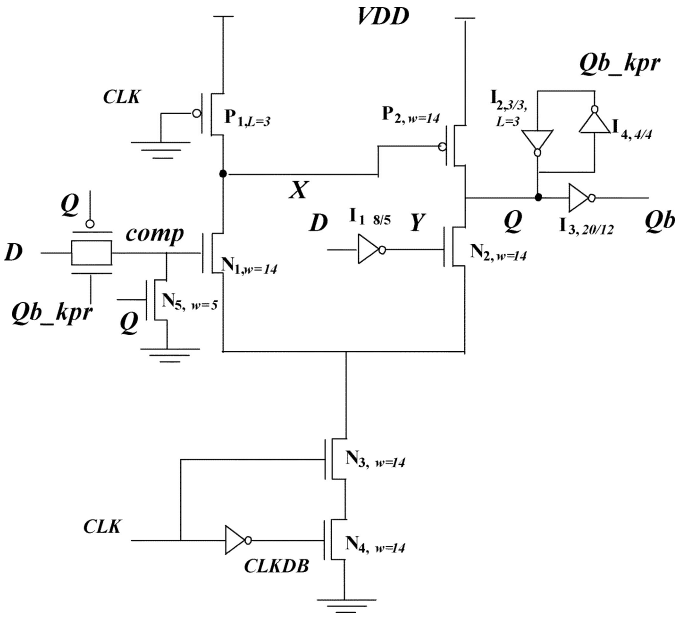

Fig. 1 Clocked-Pair Shared Flip-flop

The pseudo NMOS transistor that is PMOS, P1, is used to charge the internal node X despite being using the two clocked pre charging transistors (P1, P2) which is used in CDMFF. By comparing CDMFF with CPSFF, a total of three clocked loads are reduced in CPSFF, such that the clock load seen by the clock driver is minimized, resulting in an efficient design. CPSFF uses four clocked loads despite of seven clocked loads which is used in CDMFF, it result in about 40% reduction in number of clocked loads. Additional to this the internal node X is connected to supply voltage V_{dd} with the help of a pseudo NMOS P1, so is not floating point is now present, and result also shows an improvement in the noise robustness of node X.

When input D stays at HIGH level then Q=1, here N5 is kept ON, N1 will be kept off to avoid the redundant transient activity at node X, as well as in any short circuit current. PMOS P2 is allowed to pull Q to high level when D switches to 1 value. Then second NMOS branch (N2) is in charge for pulling down the output of Q if D = LOW value and Y=1when the clock pulse is arrives. PMOS present in N1 should turn on NMOS N2 when D=LOW. Although P1 is always ON, short circuit only occurs one time when D makes a transition from LOW to HIGH, and then discharge path is disconnected after two gates delay. After all that, if at this time also D remains at HIGH, then the discharge path is already disconnected by N1; there would be no short circuit. Here the clocked-pseudo-NMOS scheme is different from the general idea of common pseudo-NMOS logic. In the previous one we use clocked transistors in the pull down branch. P1, N1, N3, and N4 should be properly scaled to guarantee a correct noise margin. CPSFF uses three less clocked loads, which by default leads to about 40% reduction in number of clocked loads. It achieves 25% less clock driving power consumption than CDMFF, which improves power efficiency.

III. Survey of Different Low Power Techniques

In this section we have review various proposed several circuit level approaches for sub-threshold leakage power reduction.

A. Sleep Transistor Techniques :

In this approach sleep transistors are used between the power rails to break the power supply when the device is in the idle mode of operation. Due to this approach this technique is commonly known as power gated technique. Here in this technique high Vth sleep transistors is placed in pull up network and low Vth transistors is placed in the pull down network of the device to maintain high switching speed. Sleep transistors are turned off when the device is in idle state, which in respect directly reduces the leakage power in standby mode. But during active mode the device works normally. But this technique results in destruction of state plus a additional floating output voltage is generated in sleep mode.

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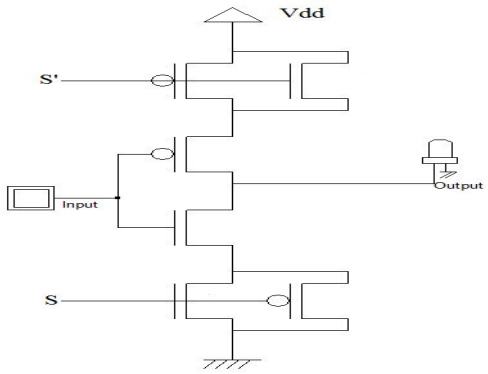

Fig 2 Sleep Transistor Approach

B. Sleepy Stack Technique:

Sleepy stack approach is the combination of Sleep approach and forced transistor technique approach. The forced transistor breaks the transistor into two halves which there by reduces the leakage power. Here sleep transistor technique retains the same logic state and saves the power when it is in sleep mode. In this approach we uses two additional sleep transistors parallel to the existing sleep transistor, here thereby the area and delay gets increased. Here during idle mode, sleep transistor are turned off and the power is substantially reduced. But during active mode, sleep transistors are on and here delay is reduced as there is active resistance path.

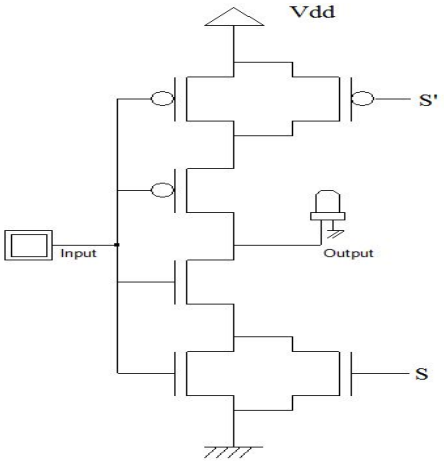

Fig. 3 Sleepy Stack Approach

C. Sleepy Keeper Technique:

In this approach, a PMOS transistor is placed in parallel to the pull up sleep transistor and a NMOS is placed parallel to pull down sleep transistor. When they are in sleep mode, here the NMOS is the only source of V_{DD} to the pull up network as the sleep transistor is turned off here. When they are in active mode, PMOS is the only source of ground to pull down network as at this time the sleep a transistor is turned on. Here due to the presence of sleep transistor, the resistance of the ON path get increases which by default decrease the propagation delay. The main advantage of this approach is that it retains the logic state of the circuit.
circuit.

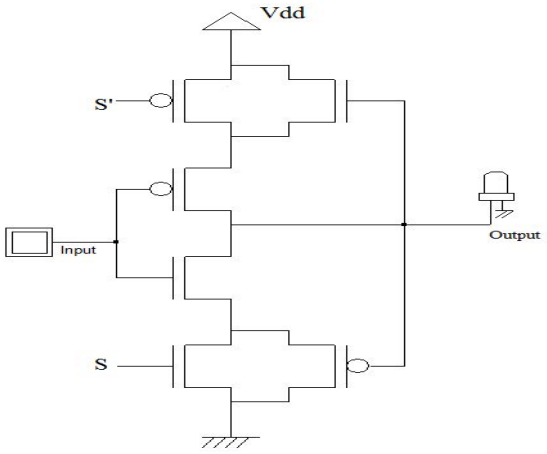

Fig. 4 Sleepy Keeper Approach

D. Dual Sleep Technique:

The dual sleep approach utilizes the advantage of using the two extra pull-up and two extra pull-down transistors in the sleep mode either in the OFF state or in the ON state. Here in the circuit since the dual sleep portion can be made common to all the logic circuitry, so a less number of transistors is needed to apply a certain logic circuit.

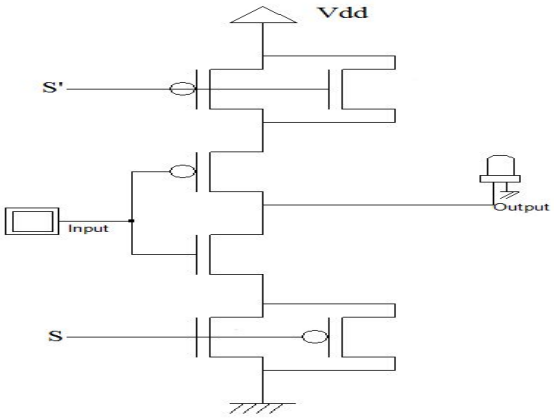

Fig. 5 Dual Sleep Approach

E. Dual Stack Technique:

In dual stack transistor approach 2 PMOS is placed in the pull down network and 2 NMOS is placed in the pull-up network. The advantage of this approach is that here NMOS degrades the high logic level while the PMOS degrades the low logic level. As compared to the previous approaches this approach requires greater area. Another disadvantage is that the delay is also increased here.

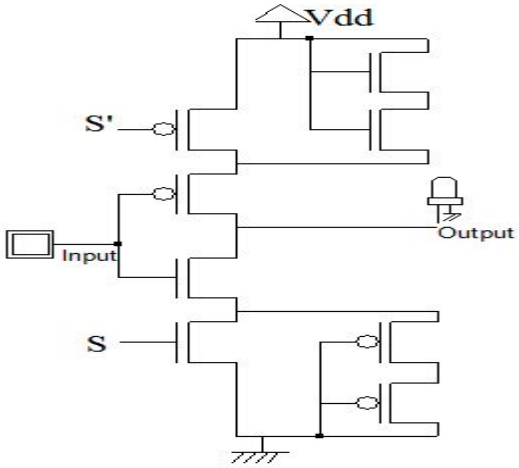

Fig. 6 Dual Stack Approach

IV. Experimental Methodology

We compare the various approaches explained earlier namely; sleep transistor approach, sleepy stack approach, sleepy keeper approach, dual sleep approach and dual stack approach. Thus, we compare five design approaches in terms of power consumption for Conditional Pair Shared Flip Flop (CPSFF). We use HSPICE for Simulation purpose to estimate delay and power consumption. Area is estimated with the help of MICROWIND. All considered approaches are evaluated for the performance by using a single, low-Vth for all transistors. Dual Vth technology is applied and tested only for the sleep, dual sleep, dual stack and proposed approaches since applying high-Vth. For the dual Vth technique, high-Vth is used for leakage reduction transistors and low-Vth is used for the other transistors. Here chosen technologies are 90 Nano meter and 45 Nano meter their supply voltages are given in Table I

Chosen Technology	90 nm	45 nm
V_{dd} value	1 v	1.2 v

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Table. I Chose Technology And V_{dd} Value

V. Experimental Results

The simulation results for all flip-flops were obtained in a 90nm CMOS technology at room temperature using HSPICE, the supply voltage is 1 V and again in 45 nm technology with voltage 1.2 V. In order to obtain the accurate results, we have simulated the circuits in the real environment, which dictates that the flip-flops' inputs (clock, data) are driven by fixed input buffers, and the outputs are required to drive an output load. The output waveform of CPSFF is shown below

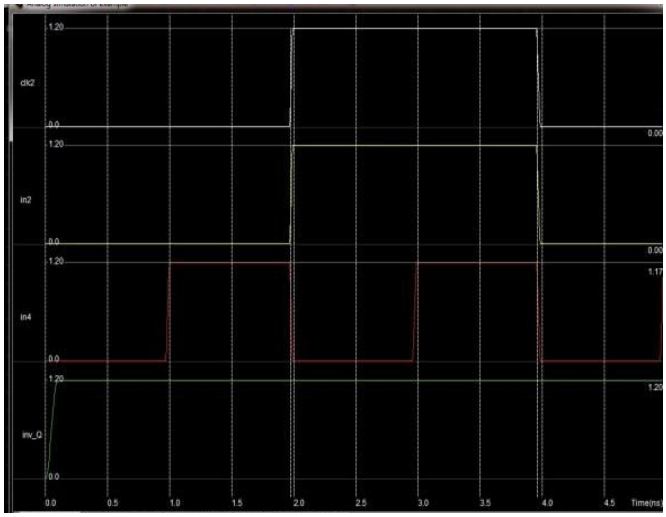

Fig 7 waveform of CPSFF

Below table shows the the comparison of the power of CPSFF flip flop in two different technology

CMOS Technology	Power (watt)
90nm	6.829E-04
45nm	8.699E-11

Table. 2 Chosen Technology And Power Value

VI. CONCLUSION

The paper surveyed various clocking system and among then the clock pared shared flip flop(CPSFF) is best suited for the using as the sequential circuit in the clocking system. Along with this clocking system various low power techniques are also surveyed which help in lowering the static power in any circuit. The comparison of the power in two technologies is also tabulated above.

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