VLSI implementation of Euclidean Geometry LDPC codes using maximum likelihood decoding

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***Abstract*-In this work ,a method was proposed to design an Euclidean geometry low density parity check codes(EG_LDPC)decoder using ML decoder algorithm.This can be useful as logic decoding can be implemented serially with simple hardware but requires a large decoding time. For memory applications, it increases the memory access time. Since most words in the memory willbe error-free, the average decoding time can be reduced.This project aims to reduce the decoding time by stopping the decoding process when no errors were detected. It is able to detect the random errors only,and butnot able to detect and correct the burst errors.Hence,in this work, we propose a modified parallel majority logic decoding with random interleaver to detect and correct the multi bit errors in LDPC receiver.The proposed LDPC Decoder is designed using Verilog HDL and simulated using Modelsim Software and Synthesized by Xilinx 9.2i.The result shows that the proposed decoder requires fewer XOR, IOBs and latency compared with existing methods.**

Index terms- low density parity check(LDPC)code, Euclidean Geometry low density parity check codes(EG-LDPC),bit error rate(BER),majority logic decoder (ML-Decoder),Field programmable gate array(FPGA).

I.INTRODUCTION

Low-density parity-check (LDPC) codes [1] [2][4] have been adopted for several data communication applications because to their superior coding performance and parallelizable decoder architecture. LDPC codes allows a fine-level parallel message-passing decoding in which all the check and variable nodes can be updated concurrently. This parallelism can bepotentially be used to build the decoder with Multi Gbit/sec throughput. The main obstacle for efficient implementation of fully-parallel LDPC decoders is theirinterconnect complexity which is the result of random location of 1's in the code's parity-check matrix. Thereforein this paper, we propose a bit-serial scheme for fully-parallelLDPC decoders. The bit-serial computation allows variable and check nodes to communicate with multi-bit messages over the single wires, there by reducing the interconnect complexity. In addition, we introduces new approximation for the check update function in min-sum decoding. In this approximation, for each check node only one of the minimum magnitude is calculated over all the check node inputs. Dependingupon the number of inputs that canshare the same minimum magnitude, a corrective constant can then be added in order to generate the proper check outputs. We canshow that with this 4-bit quantization this approximation can reduces the check node area by 48% while introducing less than 0.1 dB loss in BER performance. We illustrates the feasibility of the bit-serial LDPC decoding by implementing a (480, 355) RS-based LDPC decoder over a single Altera Stratix EP1S80 FPGA device which is based on the new proposed check node architecture. The decoder operates at maximum clock frequency of about 61 MHz, and it performs 15 decoding iterations per frame and achieves 650 Mbps throughput. In the case of amessage-passing LDPC decoding, a larger number of messages need to be updated and transfered between check and variable nodes in each iteration. Previous works of thesehave proposed several approaches for

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representing and updating these messages. In [5] analog signals are mainlyused to represent the extrinsic messages. In analog decoders the exponential voltage-current relationship of a transistor can be used to realize the message-passing update functions. Even though theanalog decoders have the advantage of low power consumption, thus they become impractical for decoding long LDPC codes because of the noise and process mismatch. More conventional LDPC decoders are often using multi-bit digital signals for representing the messages. In a partially-parallel decoders [6], [7], the messages are beingtransferred between the nodes through memory. This architecture reduces the decoder area by sharing the processingunits, but this causes the reduced throughput. Therefore to achieve higher throughput, in the fully-parallel decoder presented in [8], all check and variable nodes are directly instantiated in to the hardware. By using this architecture, a throughput of 1 Gbps with 64 iterations per frame is reported. One of the major challenges observed in the implementation of thefully parallel LDPC decoders is the complex and random interconnection between the variable and check nodes. This problem can get worsened when the multi-bit buses are used to realize the edges in the code of Tanner graph.Error correction codes are mainly used to protect memories from theso-called soft errors, that changes the logical value of memory cells but without damaging the circuit. As technology advances, memory devices are becoming larger and more powerful error correction codes are needed .To putthis end, the use of a more advanced codes has been proposed. These codes can correct a larger number of errors, but it requires complex decoders. To avoid the high decoding complexity, the use of one step majority logic decodable codes are proposed for the memory applications. This one step majority logic decoding can be implemented serially with very simple circuitry, butit often requires a larger decoding times.

II.RELATED WORK

Among thevarious decoding algorithms proposed for the LDPC codes,the Min-sum (MS) decoding algorithm have less mathematical complexity[14]. It is therefore considered as an approximation to the iterative SP (Sum-Product) algorithm[3],[5],[12]. Although the performance of Min-sum(MS) is generally few tenths of dB less than that of SP decoding, the product term present in the SP decoding thus making the architecture very complex, thereby focusing researches on MS decoding[6]. Therefore the implementation has a trade-off between decoding performance and hardware complexity. Various architectures [8–10] for implementation are considered in the literature. In the case of serialarchitecture, the area is less but it has latency overhead. While considering the case of parallel architecture, the latency overhead is overcomed but the area is getting increased as compared to the serial architecture. To optimize the trade-off between the power, latency and area overhead, the concept of wave pipelining has been introduced. Also the concept of wave pipelining has improved the performance of the LDPC encoder in terms of power, latency and area. Different from this existing work targeting the hardware implementation cost, the main focus of this paper is to reduce the hardware operational complexity in nonbinary LDPC decoder architectures.This enables asefficient decoding suitable for the emerging applications such as underwater acoustic sensor networks [17] that are under the severe resource (e.g., energy) constraints. It was reported [4] that arithmetic operations and memory access are the main two major contributors for the operating cost in LDPC decoders. A lot of research effort aims for reducing the decoding complexity of non binary LDPC codes at the algorithm level [7]–[9], [11]. In order to deal with the problem that computational complexity increases exponentially.

III.PROPOSED ARCHITECTURE

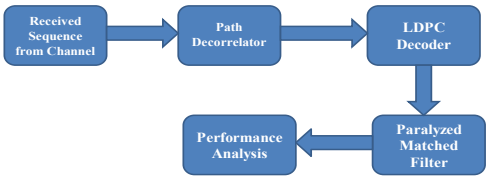

Fig 1:The proposed system architecture

The proposed system architecture includes the contents shown in fig.1.The additional components included in this are path decorrelator and paralysed matched filter. The received sequence from the channel are directly fed to the path decorrelator. The main function of the path decorrelator is to select the best path signal from received path signals.

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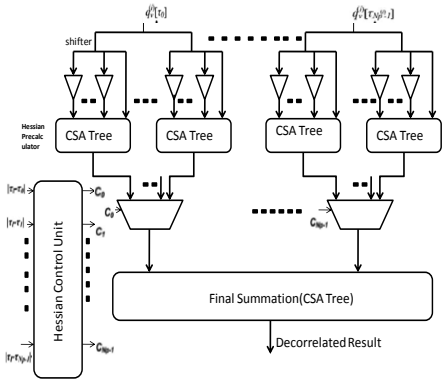

Fig 2:pathdecorrelator circuit

The output bits of the path decorrelator is fed to the LDPC decoder for further decodingThe main focus of this section is to present a modified version of the ML decoder that improves the designs. Starting from the very original design of the ML decoder introduced in [13] the proposed ML detector/decoder (MLDD) can be implemented using the difference-set cyclic codes (DSCCs) [15]–[19].The ML decoder is capable of correcting multiple random bit-flips .The Additional hardware that is needed to perform the error detection are the following:

i) the control unit which triggers a finish signal when no errors are detected after the third cycle of the decoding and

ii) the output tristate buffers.

The output tri state buffers are always in a high impedance stateunless the control unit sends out the finish signal so that the current values of the shift register are then forwarded to the output 'y'.The control unit is managing the detection process. It act as a counter that counts up to three, which distinguishes the first three iterations of the ML decoding. In the first three iterations of ML decoding, the control unit evaluates them by combining them with the OR1 function. Then this value is fed into a three-stage shift register, which holds the results of the last three cycles. In the third cycle, the OR2 gate then evaluates the content of the detection register. When the value of the result is "0," the FSM then sends out the finish signal indicating that the processed word is error-free. In the other case, if the value of the result is "1," the ML decoding process runs until the end. Thus it clearly provides a performance improvement respective to the traditional method. Since most of the words take only three cycles (five, if we consider the other two for input/output) and only those with errors (which should be a minority) are needed to perform the whole decoding process.

e number of parity check equations

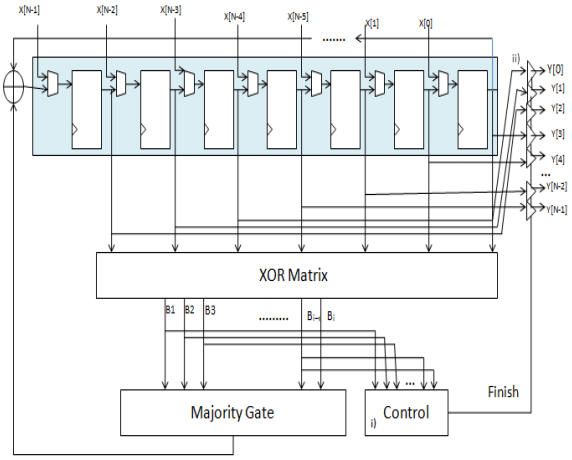

Fig 3:modified LDPC decoder

The paralysed matched filter acts as aineterleaver.It is used to remove random and burst errors in parallel manner .By this almost all the errors are corrected which is not completed by LDPC decoder.The output bits of the paralysed matched filter is given for the performance analysis. In performance analysis we can clearly see the hardware utilizations.It includes XOR.IOBs and latency.

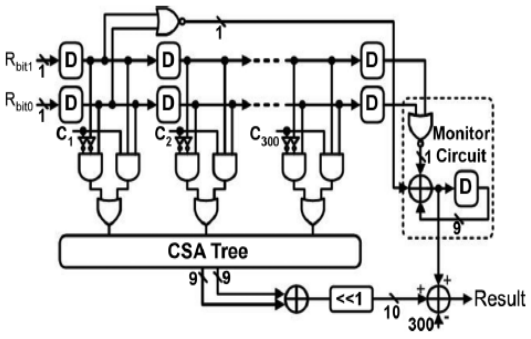

Fig 4:paralysed matched filter

IV. SIMULATION RESULTS

In theproposed architecture, the higher throughput, less power consumption and less hardware utilization were achieved .The architecture is implemented using spartan3E family and XC3S500E device in Xilinx 9.2i.The proposed system is written in Verilog HDL language and

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synthesized in Xilinx 9.2i and stimulated using Modelsim5.7.thr results are shown in fig.5.The RTL schematic view is shown in fig 6and technology schematic view is shown in fig 7

Simulation Screenshot:

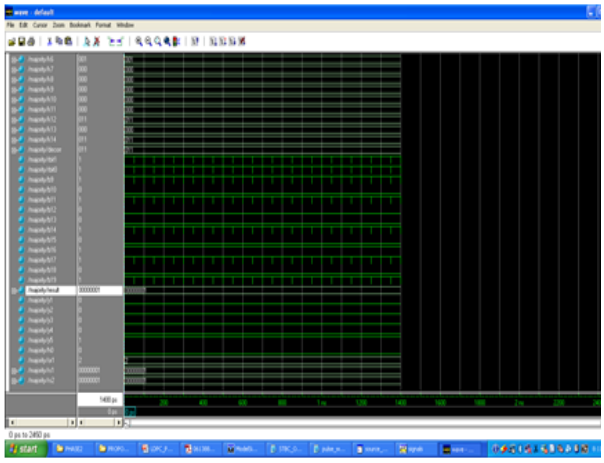


Fig 5: Simulation result

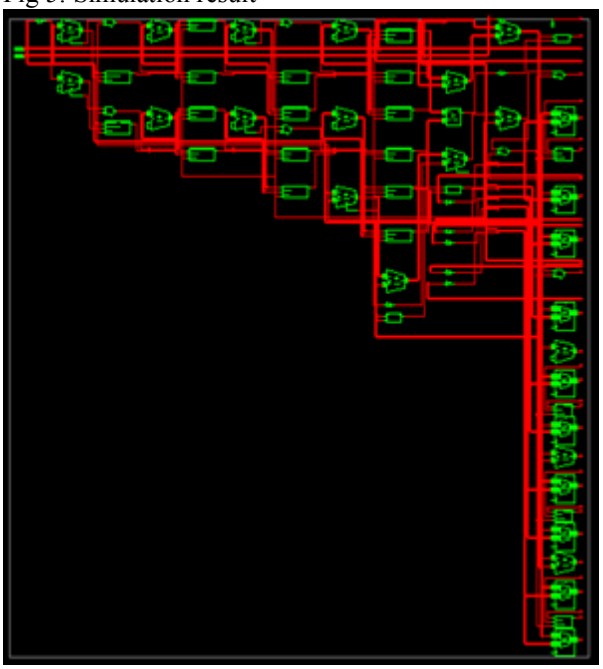


Fig 6:RTL schematic view

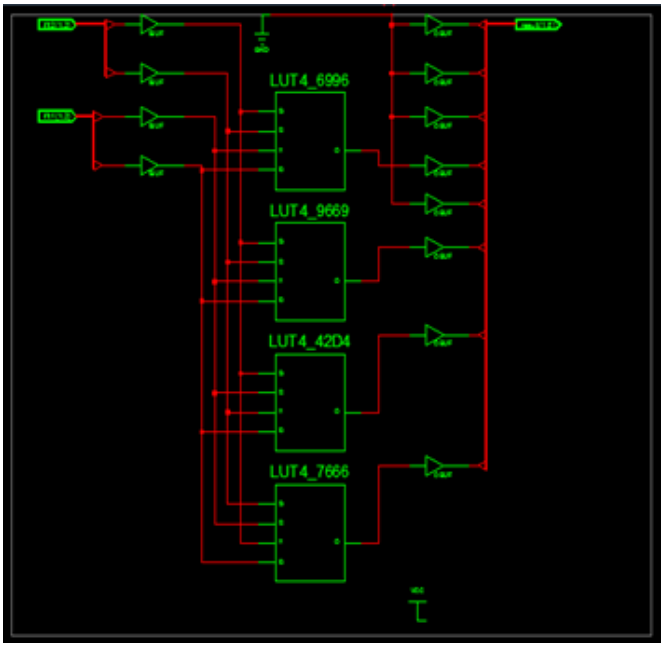
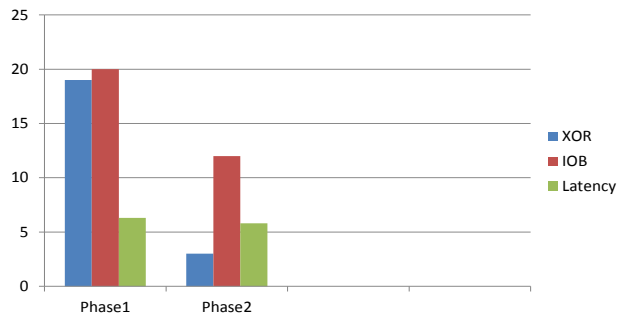


Fig 7:Technology schematic view

Performance Analysis:

Hardware Utilizations	Phase1 Results	Phase2 Results
XOR	19	3
IOBs	20	12
Latency	6.37ns	5.895ns

Graphical Comparisons:



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V. CONCLUSION

The detection of errors during thefirst iterations Ofserial one step Majority Logic Decoding ofEG-LDPC codeshave been studied.The main objective of the work is to reduce thedecoding time by stopping the decoding process when no errors are detected. The simulation results nowshows that all the tested combinations of errors affecting upto four bits are detected and corrected in the first three iterations of decoding. These results extends to ones recently presented for DS-LDPC codes, making the modified one step Majority logic decoding more attractive for memory applications. The designer now have now a large choice of word lengths and error correction capabilities.The results shows that XOR,IOBs and latency were reduced comparing to the existing method.

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