Test pattern reduction in reversible conservative register

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Abstract

There are several faults which arise in the VLSI system due to defects in system design, layout structures, design time and design cost. Faults are increasing aside when a technology grows exponentially. There are several faults which arises causes system failures. The most important and growing fault in VLSI system are stuck-at-0 fault and stuck-at-1 fault. To avoid these faults several algorithms and techniques are being developing. The fault can be detected by test vectors applied to circuit. Thus to detect the fault using only two test vector such 0's and 1's a conservative reversible fredkin gate is used. Using this gate sequential circuits like D latch, Master Slave D flip flop and Double edge triggered D latch are designed and tested for stuck-at-0 fault and stuck-at-1 fault by using only two test vectors '0' and test vector'1'.

I. INTRODUCTION

Conservative logic exhibits equal number of 1's in output and input. This logic exhibit a property of reversibility. In nature it may reversible or irreversible. When there is one –to –one mapping between input and output vector with equal numbers of 1's in input and output then the logic is reversible. If the condition is not preserved then it is irreversible. When a bit or information is transferred from one system to other system there will be KTln2 joules of heat energy loss in the system, if a system is irreversible. This heat energy loss can be eliminated in reversible logics it has been proved by many researches. This type of reversible logics can be used in emerging technologies like ultra low power technologies and nano technologies.

Testing is a process of applying inputs and comparing output with expected values, verifying the correctness of designed circuit. Circuit manufacturers must thoroughly test their products before delivering them to customers. The causes of circuit failure can be divided into two main categories namely design errors and manufacturing defects.

Design error is layout errors it can be eliminated when layout is modified. But in the case of manufacturing defects the errors cannot be eliminated easily it creates malfunctioning of components in-build in the circuit. These errors occur in different formats like stuck-at faults, bridging fault, open fault, delay fault. As the chip area increases, the probability of a defective chip increases and the yield decreases.

A stuck-at fault is a particular fault model used by fault simulators and Automatic Test Pattern Generator (ATPG) tools to mimic a manufacturing defect within an integrated circuit. Individual signals and pins are assumed to be stuck at Logical '1', '0' and 'X'. For example, an output is tied to a logical 1 state during test generation to assure that a manufacturing defect with that type of behaviour can be found with a specific test pattern. Likewise the output could be tied to a logical 0 to model the behaviour of a defective circuit that cannot switch its output pin. Not all faults can be analyzed using the stuck-at fault model.

II.CONSERVATIVE FREDKIN GATE

The Fredkin gate is a popularly used reversible conservative logic gate, first proposed by Fredkin and Toffoli. The Fredkin gate shown in Fig. 1 can be described as a mapping (A, B, C) to ($P = A$, $Q = A\_B + AC$, $R = AB + A\_C$), where A, B, C are the inputs and P, Q, R are the outputs, respectively. The truth table for the Fredkin gate is illustrated in [3], which demonstrates that Fredkin gate is reversible and conservative in nature, that is, it has unique input and output mapping and also has the same number of 1s in the outputs as in the inputs.

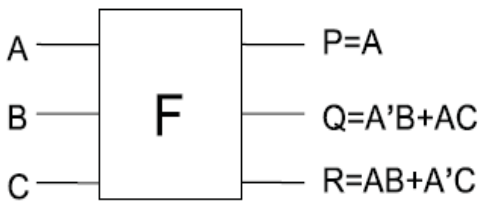

Fig 1.1 Fredkin gate

III.DESIGN OF TESTABLE LATCH

The characteristic equation of the D latch can be written as $Q+ = D \cdot E + .E \cdot Q$. In the proposed

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work, enable *(E)* refers to the clock and is used interchangeably in place of clock. When the enable signal (clock) is 1, the value of the input D is reflected at the output that is $Q+ = D$. While, when $E = 0$ the latch maintains its previous state, that is $Q+ = Q$. The reversible Fredkin gate has two of its outputs working as 2:1 MUxes, thus the characteristic equation of the D latch can be mapped to the Fredkin gate (F). Fig shows the realization of the reversible D latch using the Fredkin gate. But FO is not allowed in conservative reversible logic. Moreover, the design cannot be tested by two input vectors all 0s and all 1s because of feedback, as the output Q would latch 1 when the inputs are toggled from all 1s to all 0s and could be misinterpreted as stuck-at-1 fault.

The design can work in two modes:
1) normal mode and 2) test mode.

1) Normal Mode: The normal mode in which we will have $C1C2 = 01$ and we will have the design working as a D latch without any fan-out
problem.

2) Test Mode (Disrupt the Feedback): In test mode, when $C1C2 = 00$ it will make the design testable with all 0s input vectors as output T1 will become 0 resulting in making it testable with all 0s input vectors. Thus, any stuck-at-1 fault can be detected. When $C1C2 = 11$ the output T1 will become 1 and the design will become testable with all 1s input vectors for any stuck-at-0 fault.

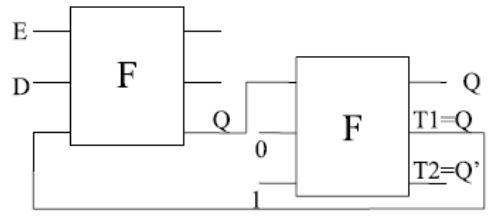

Fig 2.1 Normal mode

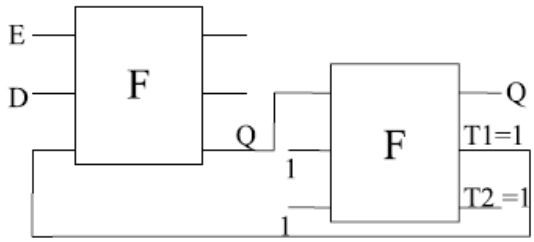

Fig 2.2 Test mode

IV.DESIGN OF TESTABLE MASTER-SLAVE FLIP-FLOPS

The testable reversible D flip-flops has four control signals $mC1$,$mC2$, $sC1$, and $sC2$. $mC1$ and $mC2$ control the modes for the master latch, while $sC1$ and $sC2$ control the modes for the slave latch.

In the normal mode,
when the design is working as a master-slave flip-flop the values of the controls signals will be $mC1 = 0$ and $mC2 = 1$, $sC1 = 0$ and $sC2 = 1$ (as similar to values of the control signals C1 and C2 earlier described for the testable D latches).
In the test mode.

1) To make the design testable with all 0s input vectors for any stuck-at-1 fault, the values of the controls signals will be $mC1 = 0$ and $mC2 = 0$, $sC1 = 0$ and $sC2 = 0$. This will make the outputs $mT1$ and $sT1$ as 0, which results in breaking the feedback and the design becomes testable with all 0s input vectors for any stuck-at-1 fault.

2) To make the design testable with all 1s input vectors for any stuck-at-0 fault, the values of the control signals will be $mC1 = 1$ $mC2 = 1$, $sC1 = 1$, and $sC2 = 1$. This will result in outputs $mT1$ and $sT1$ having a value of 1, breaking the feedback and resulting in the design testable with all 1s input vectors for any stuck-at-0 fault.

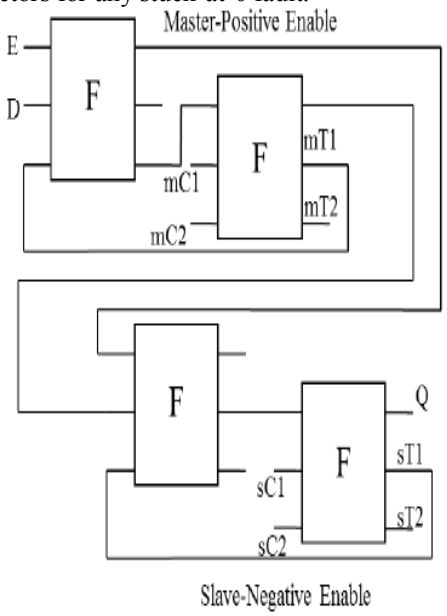

Fig 2.3 master slave flipflop

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V.DESIGN OF TESTABLE REVERSIBLE DET FLIP-FLOPS

In the proposed design of testable reversible DET flip-flop, pC1 and pC2 are the controls signals of the testable positive enable D latch, while nC1 and nC2 are the control signals of the testable negative enable D latch. Depending on the values of the pC1, pC2, nC1, and nC2, the testable DET flip-flops work either in normal mode or in the testing mode.

1) *Normal Mode:* The normal mode of the DET flip-flop is illustrated in which the $pC1 = 0$, $pC2 = 1$, $nC1 = 0$, and $nC2 = 1$. The $pC1 = 0$, $pC2 = 1$ help in copying the output of the positive enable D latch thus avoiding the FO while the $nC1 = 0$ and $nC2 = 1$ help in copying the output of the negative enable D latch thus avoiding the FO.

2) *Test Mode*: There will be two test modes.

a) *All 1s Test Vectors:* This mode is illustrated in fig 2.5 which has control signals will have value as $pC1 = 1$, $pC2 = 1$, $nC1 = 1$, and $nC2 = 1$. The $pC1 = 1$ and $pC2 = 1$ help in breaking the feedback of the positive enable D latch, while the $nC1 = 1$ and $nC2 = 1$ help in breaking the feedback of the negative enable D latch. This makes the design testable by all 1s test vector for any stuck-at-0 fault.

b) *All 0s Test Vectors:* this mode is with the control signals will have value as $pC1 = 0$, $pC2 = 0$, $nC1 = 0$, and $nC2 = 0$. The $pC1 = 0$ and $pC2 = 0$ help in breaking the feedback of the positive enable D latch, while the $nC1 = 0$ and $nC2 = 0$ help in breaking the feedback of the negative enable D latch

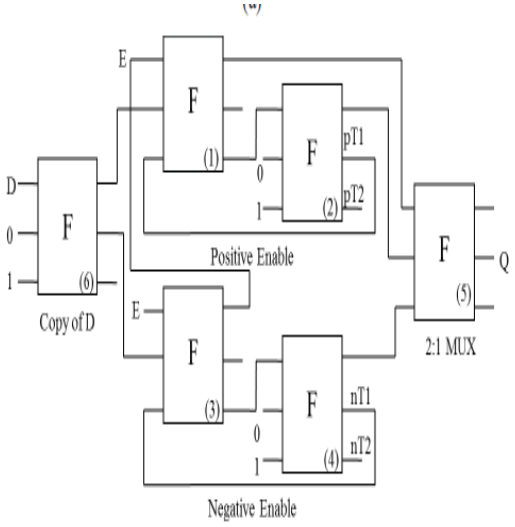

Fig 2.4 normal mode of DET

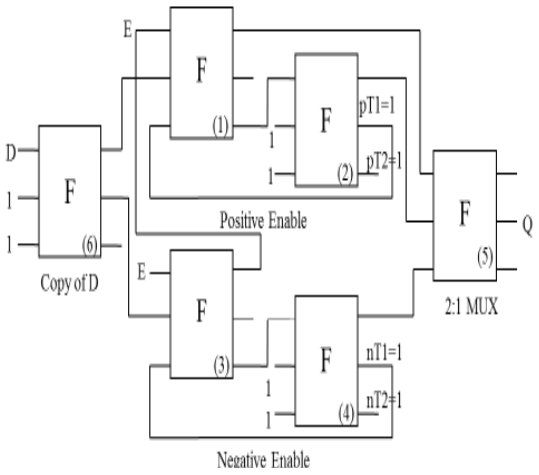

Fig 2.5 Test mode of DET

VI.CONCLUSION

Thus in this project using emerging technique such as conservative reversible gates the D Latch, Master Slave D flip flop and Double Edge triggered D Flip flop are designed and the designs are worked in normal mode and test mode for the detection of stuck-at-0 and stuck-at-1 fault in the system only using two test vectors 0's and 1's. And fault in the system is detected effectively

VII.OUTPUT WAVEFORM

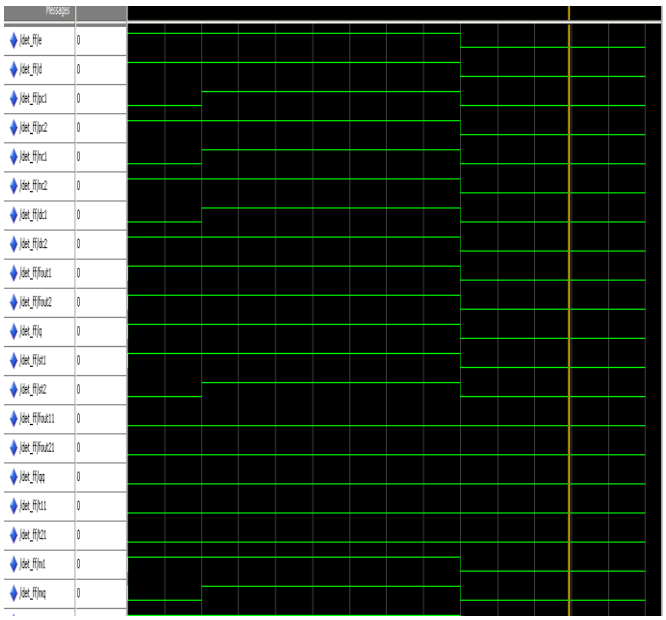

Fig3.1 output of D latch

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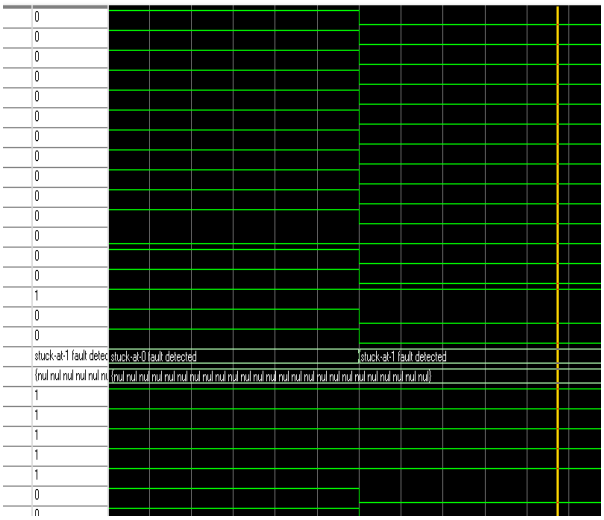

Fig 3.2 output of master slave flipflop

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