A 90 nm Static Random Access Memory in Submicron Technology

Ms. P. A. Kandalkar, Ms. K. S. Kshirsagar, Mr. Y.N. Thakre

***Abstract*— Static Random Access Memories (SRAM) and dynamic RAM (DRAM) have been the most popular technologies used to implement memory cells in computer systems. SRAM cells typically implemented with six transistors (6T cells) have been usually designed for speed, while DRAM cells, implemented with only one capacitor and the corresponding pass transistor (1T-1C cells) have been generally designed for density. Because of this reason, the former technology has been used to implement cache memories and the latter for main memory storage.**

***Index Terms*— SRAM, 6T, Non-volatile, leakage, power dissipation, speed, etc.**

I. Introduction

The power consumption has become an important consideration on the VLSI system design and microprocessor as the demand for the portable devices and embedded systems continuously increases [1, 2]. The on-chip caches can reduce the speed gap between the processor and main memory. These on-chip caches are usually implemented using SRAM cells. The write power is usually larger than the read power due to large power dissipation in driving the cell bit lines to full swing. The sum of the power consumption in decoders, bit lines, data lines, sense amplifier, and periphery circuits represents the active power consumption. The power dissipated in bit-lines represents 70 per cent of the total SRAM power consumption during a write operation [3]. Many techniques have been proposed to reduce the write power consumption by reducing the voltage swing level on the bit lines [4-6]. Especially for modern VLSI processor design, SRAM takes large part of power consumption portion and area overhead.

The fundamental building block of a static RAM is the SRAM memory cell. The cell is activated by raising the word line and is read or written through the bit line. Figure1.1 shows a 12-transistor SRAM cell built from a simple static latch and tri-state inverter.

Manuscript received Mar 28, 2014.

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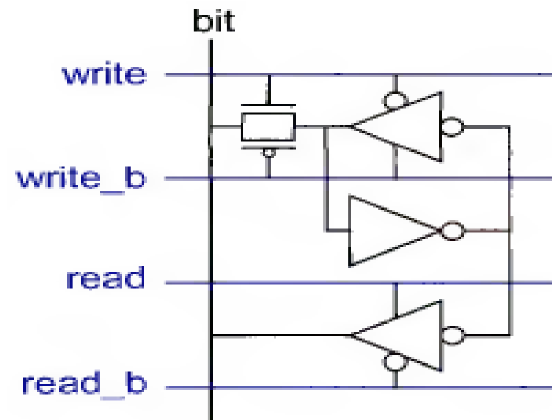

Figure1.1: 12-transistor SRAM

The cell has a single bit line. True and complementary read and write signals are used in place of a single word line. The power and ground lines can be shared between mirrored adjacent cells, but the area is still limited by the wires and is undesirably large. However, the cell is easy to design because all nodes swing rail-to-rail and it is fast when used in small RAMs and register files. Figure1.2 shows a 6-transistor (6T) SRAM commonly used in practice. Such a cell uses a single word line and both true and complementary bid lines. The complementary bit- line is often called bit or bit. The cell contains a pair of cross-coupled inverters and an access transistor for each bit line. True and complementary versions of the data are stored on the cross-coupled inverters. If the data is disturbed slightly, positive feedback around the loop will restore it to VDD or GND. The word line is asserted to read or write the cell.

Two types of SRAM cells will be considered in this paper. (i) Conventional Twelve-transistor (12T) SRAM cell, as shown in Figure1.2 (ii) Load less six-transistor (6T) SRAM Cell, as shown in Figure1.2 They will be designed and analyzed in various configurations with respect to functionality, power dissipation, area occupancy, stability and access time. True and complementary versions of the data are stored on the cross-coupled inverters.

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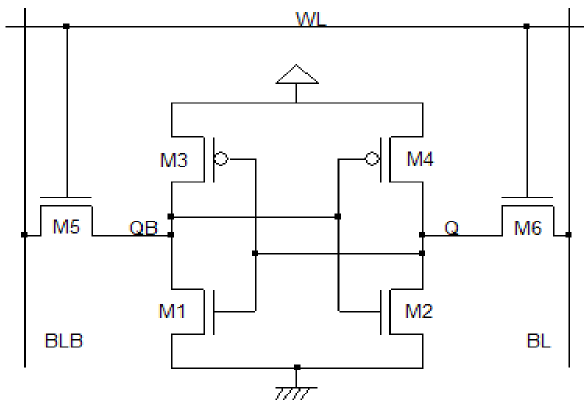

Figure1.2: Conventional 6T SRAM Cell

II. LITERATURE

Static Random Access Memory (SRAM) is a type of semiconductor memory. SRAMs are a major component of digital systems such as Embedded systems, microprocessors, reconfigurable hardware, field programmable gate arrays just to name a few. Fast memory access times and design for density have been two of the most important target design criteria for many years, however with device scaling to achieve even faster designs; power supply voltages and device threshold voltages have scaled as well leading to degradation of standby power and static noise margins of memories. SRAM exhibits data remanence, but is still volatile in the conventional sense that data is eventually lost when the memory is not powered. A typical SRAM uses six transistors to store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 4 Transistors till 10 Transistors per bit. The design explains each block of SRAM based on CMOS 32nm model file.

2.1 SRAM CELL with 10T

The 10T SRAM bit cell uses a fully differential read sensing scheme, as shown in Figure 2.1. In the read mode, WL is enabled and Vgnd is forced to 0 V while WWL remains disabled. The disabled WWL makes data nodes Q and QB decoupled from the bit line during the read access. Due to this isolation, the read SNM of the 10T SRAM cell is almost same as that of the hold SNM of the conventional 6T SRAM cell. Based on the cell data value, one of the bit lines would get discharged after the WL is enabled. It can be noticed that in this 10T SRAM cell, read value is developed as an inverted signal of cell data. Prior to the write operation, the bit lines BL and BLB are precharged to the pre-determined values. In the write mode, both the word lines WL and WWL are enabled to transfer the write data to the cell nodes from the bit lines. Since this 10T SRAM cell has series access transistors, writability is a critical issue.

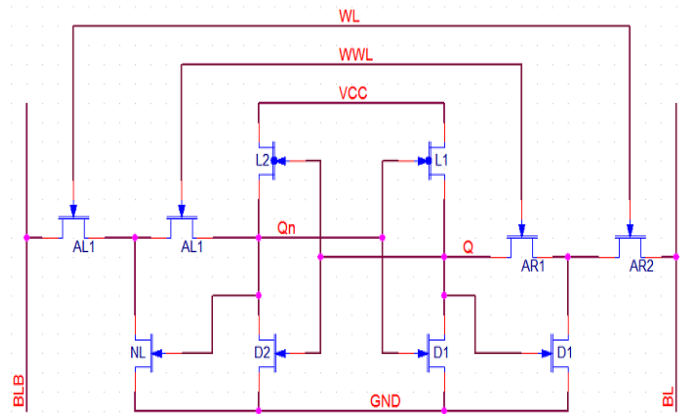

Figure 2.1: 10 T SRAM Cell

2.2 SRAM CELL with 9T

The proposed 9T SRAM cell consists of cross-coupled inverters formed by the transistors L1, D1, L2 and D2 which store a single bit of information, shown in Figure 8. The write bit line WBL and the pass transistor A2 are used for transferring new data into the cell. Alternatively, the read bit line RBL and transistors E2, E3 and E4 are used for reading data from the cell. The 9T SRAM cell enhances the read stability by employing a read discharge path that is completely isolated from the internal nodes of the cell. The data stability is thereby significantly improved when compared with the conventional 6T SRAM cell design. Based on the voltage at node “Qb”, the RBL is conditionally discharged through the E2-E4 transistor stack during a read operation.

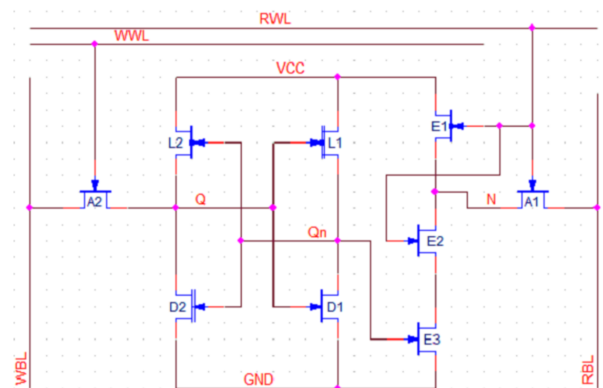

Figure 2.2: 9 T SRAM Cell

2.3 SRAM CELL with 8T

The 8T SRAM cell shown in Figure 2.3 uses a buffered read to isolate the internal nodes of the cell from the read path. Prior to the read operation the read bit line RBL is precharged to Vdd. The read operation is started by asserting the RWL. RBL either remains at Vdd (if internal node “q” contains a “0”) or is pulled down to ground (if internal node “q” contains a “1”). In either case, the internal nodes remain undisturbed. Prior to the write operation, the bit lines are precharged to the pre-determined values. The write operation is initiated by asserting the write word line WWL and the nodes attain the corresponding values from the bit lines.

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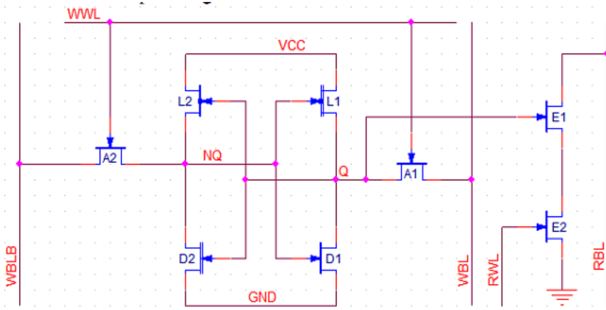

Figure 2.3: 8 T SRAM Cell

III. Typical SRAM Architecture

A typical SRAM block consists of cell arrays, address decoders, column multiplexers, sense amplifiers, input/output (I/O), and a control unit. In the following, the functionality and design of each component is briefly discussed.

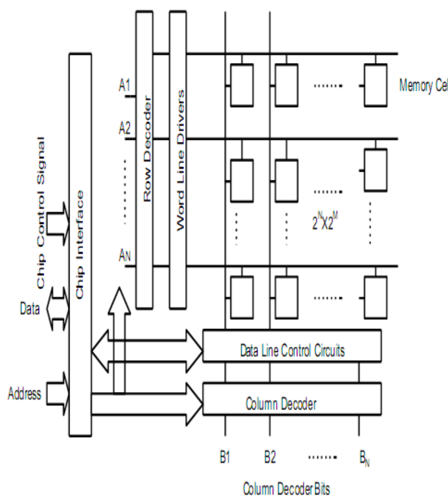

Figure 3.1 SRAM Architecture

A. Final Stage

Figure 3.1 shows a SRAM cell. In a SRAM cell, the fundamental building block of a static RAM is the SRAM memory cell. The cell is activated by raising the word line and is read or written through the bit line. The cell has a single bit line. True and complementary read and write signals are used in place of a single word line. The pull-down N-MOS transistors and the pass-transistors reside in the read path. The pull-up P-MOS transistors and the pass-transistors, on the other hand, are in the write path. Traditionally, all cells used in an SRAM block are identical (i.e., corresponding transistors have the same width, threshold voltage, and oxide thickness) which results in identical leakage characteristic for all cells. [5]

B. Cell Array

The data storage structure or core consists of individual memory cell arranged in array of horizontal rows and vertical columns. Each cell is capable of storing one bit of binary information. The size of the cell array depends on both performance and density requirements. Generally speaking, as technology shrinks, cell arrays are moving from tall to wide structures. In this structure, there are 2N rows, also called word line, and 2M columns, also called bit line. Thus the total number of memory cell in this array is 2N X 2M. [5]

C. Address Decoder

To access particular memory cell i.e. particular data bit in this array, the corresponding word line and bit line must be activated. Although the logical function of an address decoder is very simple, in practice designing it is complicated. To overcome the pitch-matching problem and reduce the effect of wire"s capacitance on the delay of the decoder, the address decoder is often broken into two pieces. The first piece, called pre-decoder, is placed before the long decoder wires and the second part, row decoder, which usually consists of a single NAND gate and buffers for driving the word-line capacitance, is pitch-matched and placed next to each row as shown in Figure.3.1[5]

IV. Proposed SRAM Cell

Figures Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote “0” and “1”. Two additional access transistors help controlling the access to the cross coupled unit formed by the inverters during read and write operations. So typically it takes six transistors to store one memory bit. The design of a basic SRAM cell is shown in Figure 5. Access to the cell is enabled by the word line (WL) which controls the two access transistors M5 and M6 which allow the access of the memory cell to the bit lines: ‘BL’ and ‘BLbar’. They are used to transfer data for both read and write operations. The presence of dual bit lines i.e. ‘BL’ and ‘BLbar’ improves noise margins over a single bit line. The operation of CMOSs based memories is very similar to that of CMOS except for minor differences in device orientation. One such difference being that the source and drain terminals of a CMOS are not interchangeable as is the case with CMOS devices. Care must therefore be taken to orient the transistors in a memory cell in a manner that will ensure correct transmission of logic levels.

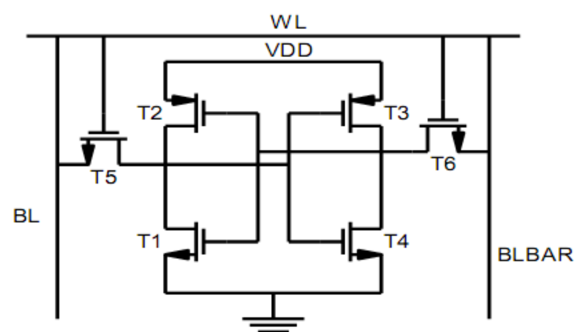

Figure 4.1: SRAM Cell with 6 Transistors

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V. CONCLUSION

The New Load Less 6t-Sram Cell Is Designed And Analyzed In Deep Submicron (130nm, 90nm And 65nm) Cmos Technologies, Which Establish The Technology Independence Of The New Load Less 4t Sram Cell And Its Consistent Performance With Respect To Conventional 6t Sram Cell In Deep Sub-Micron Regime. The New Load Less 6t Sram Array Consumes Low Power With Low Area. The Most Significant Feature Of This New Load Less 4t Sram Cell Is That There Is No Need To Modify Any Of The Fabrication Process. Thus It Can Be Used For On-Chip Caches In Embedded Microprocessors, High Density Srams Embedded In Any Logic Devices, As Well As For Stand-Alone Sram Applications.

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