

Process Variability Analysis in 14-nm SOI FinFET Inverters

Nagaratna Shanbhag, Kiran Bailey, Dr. K.S. Gurumurthy

Abstract— A comprehensive simulation analysis of process induced variations on 14-nm technology node silicon on insulator (SOI) FinFET and impact of these variations on delay and static power dissipation of FinFET inverter has been presented in this paper. Process parameters such as Gate length (L_g), Width of the fin (W_{fin}), Gate oxide thickness (T_{ox}) and Height of the fin (H_{fin}) are considered. In modelling of parameter variation, well-known statistical, DoE/RSM techniques are adapted and the analytical results are extracted from the model. It was found that, the delay is affected by fin dimension variations such as height and width of the fin. Effect of fin width variations on delay can be minimized by choosing low fin heights. The variations in gate oxide thickness imposes major impact on static power and that of gate length variation is relatively small. Variation in static power due to the L_g can be minimised by keeping thicker oxides.

Index Terms— DoE/RSM, FinFET, Process and device simulation, Process variability, Static power dissipation, TCAD.

I. INTRODUCTION

CMOS devices have been scaled down relentlessly in each technology generation to achieve faster devices and higher circuit density. As captured by Moore's law, scaling has intensified the phenomenal success of semiconductor industry. However, short channel effects (SCE), such as V_T roll-off, hot carrier effects, drain induced barrier lowering (DIBL), increase in sub-threshold swing and leakage currents, etc, make it difficult for the industry to follow the Moore's Law with bulk devices [1]. So as an alternative, FinFET [2], an innovative MOS device structure is gaining importance. This gives superior performance because they have better control of the short-channel effects (SCEs) and near ideal turn-off characteristics. Thus lower leakage level can be maintained even with very short gate length and can be practically analyzed for analog as well as digital applications and considered to be the best candidates for sub-45 nm scaling of MOSFETs [3].

The fabrication process of FinFETs suffers from some process challenges such as the precise control of the fin width and fin height and non-uniformity of the gate oxide on the

etched sidewall of the fin, which is difficult to achieve. Similarly, the channel-oxide interface condition is determined by the sidewall roughness of the fin and large parasitic resistance between the channel and source/drain is another challenge to the performance of FinFET devices. Hence there exists a tradeoff between performance and variability [4]. As real devices go through many processing steps, reliable evaluation or design optimization of final devices depend on the unit process development. As stated by Pelgrom's law, the significance and complexity of process variation increases with technology scaling or the statistical variability is inversely proportional to the transistor area. The variability can be studied between lot-to-lot, wafer-to-wafer, die-to-die and within die. Here we considered only within die (WID) variations as they are more effective at the sub-45nm technology nodes as compared to any other mentioned variabilities [5-8]. WID variations includes systematic, random and unknown variations like, Random Discrete Dopants (RDD), Line Edge Roughness (LER), Gate Oxide Thickness Fluctuations (OTF), Metal Gate Granularity (MGG). Significant timing error (17%) and performance loss takes place if variability is not properly addressed [9-10].

3D devices are prone to more complex sources of variability than conventional planar bulk and SOI MOSFETs [11]. FinFET devices can tolerate very low channel doping fluctuations because the fin, which acts as channel is lightly doped [12]. Apart from the sensitivity to channel length, the characteristics of FinFETs are highly sensitive to the fin dimensions. However, new and important source of statistical variability associated with FinFET fabrication is LER, which in turn relates to Fin edge roughness (FER) & Gate edge roughness (GER). Among many variability sources, the channel length and the fin dimensions are the critical process parameters to be modeled [13]. Therefore, most sensitive parameters are identified as, variations in Gate length (L_g), Fin width (W_{fin}), Height of the fin (H_{fin}) and Oxide thickness fluctuation (OTF). Design of experiments (DOE) is designed for the identified parameters and the simulations are carried out. This work comprises of design and simulation of the nominal device, design of experiment and running of the experiment, extraction of results, fitting the response surfaces (models) and testing of the models.

This paper investigates the effect of various process parameters of FinFET on its performance and also impact of the device parameter variations on the performance of CMOS inverter (Delay and Static power dissipation). In the section II, we describe the complete modeling and simulation of the device with realization of inverter. It covers the

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methodology used in modeling of variability. A detailed study of individual and interaction effects of all relevant variability sources on the performance of FinFET inverter is presented in Section III. Conclusion is drawn in section IV.

II. DEVICE DESCRIPTION AND SIMULATION ENVIRONMENT

This paper presents the experimental variability model for the geometrical parameters of FinFET namely, L_g , W_{fin} , T_{ox} and H_{fin} . The variability study and the modeling strategy development is carried out on a 14-nm technology node SOI FinFET which is designed using Sentaurus TCAD tool [14]. The 3-D device structure generated from Sentaurus Device Editor (SDE) is shown in Fig. 1. Table 1. summarizes the geometrical corner values of the process parameters [15]. Table 2. Gives the information of other geometrical and non geometrical (doping related) parameters. Physical and electrical specifications of the device have been taken from ITRS (Low Standby Power Technology Requirements) 2012 update [16].

TABLE I. GEOMETRIC CORNER VALUES OF PROCESS VARIATIONS FOR PROCESS PARAMETERS

| Process parameters | Nominal values (in nm) | Deviation from the nominal values [15] | Range of values (in nm) |
|--------------------|------------------------|--|-------------------------|
| L_g | 14 | 10% | 12.6 – 15.4 |
| W_{fin} | 4 | 20% | 3.2 – 4.8 |
| T_{ox} | 0.8 | 10% | 0.72 – 0.88 |
| H_{fin} | 20 | 12% | 17.6 – 22.4 |

TABLE II. NOMINAL DEVICE DOPING PROFILE AND CHARACTERISTICS

| Parameters | Values |
|-------------------------------|--------------------|
| N_{SD} (cm ⁻³) | 1×10^{20} |
| N_{FIN} (cm ⁻³) | 1×10^{16} |
| V_{DD} (V) | 0.8 |
| I_{ON} (mA) | 0.344712 |
| I_{OFF} (10^{-14} A) | 6.75907 |
| V_T (V) | 0.62510149 |
| G_m (S/ μ m) | 0.002237604 |
| DIBL(mV/V) | 19.67376 |
| S_{SUB} (mV/dec) | 62.803 |
| Gate leakage magnitude (nA) | 3.363 |

A. Process and Device Simulation

Semiconductor process simulation is the modeling of the fabrication of semiconductor devices. The ultimate goal of process simulation is an accurate prediction of the active dopant, device geometry and stress distribution. The critical process steps for FinFETs on standard SOI involve fin formation, gate oxide growth, gate formation (poly silicon), spacer formation (silicon nitride) and source-drain formation. No halo implants were used for setting threshold voltage in the nominal process flow. Process Simulation is carried out by meshing the device and generating the mesh for the further device simulation.

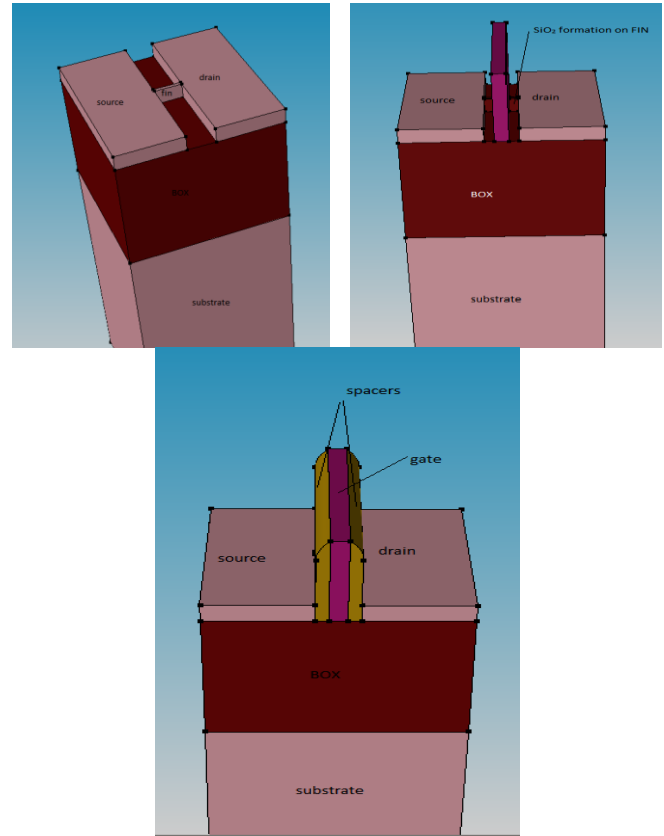


Fig. 1. Schematic showing the 3-D device simulated in SDE.

Device simulation was carried out to simulate the electrical characteristics of semiconductor devices, as a response to external electrical, thermal or optical boundary conditions imposed on the structure. This model is useful in simulating devices ranging from deep submicron heterostructure devices. For a given supply voltage, $V_{DD}=0.8V$, I_{off} was defined at $V_{GS}=0V$ and Similarly, I_{on} was defined at $V_{GS}=0.8V$.

B. CMOS Inverter realization

The performance of the SOI FinFET devices has been evaluated by implementing the devices in the basic inverter circuit comprising of a p-FinFET and a n-FinFET device with 14 nm gate length. The width ratio of p-FinFET to n-FinFET is 4:1 to obtain symmetrical characteristics [17]. The quad fin architecture provides for the necessary area factor. Mixed mode simulations are carried out to realize the inverter circuit. The necessary voltage transfer characteristics (VTC) and transient response curves of the inverter is obtained. The total gate capacitance of the device is obtained through capacitance - voltage (CV) characterization. Fig. 2, shows the Voltage Transfer Characteristics (VTC) and Transient Response of a Basic Inverter with nominal device dimensions. The main aim is to understand the impact of process variations on total delay and static power dissipation of the logic gate called inverter. They are calculated analytically and analyzed.

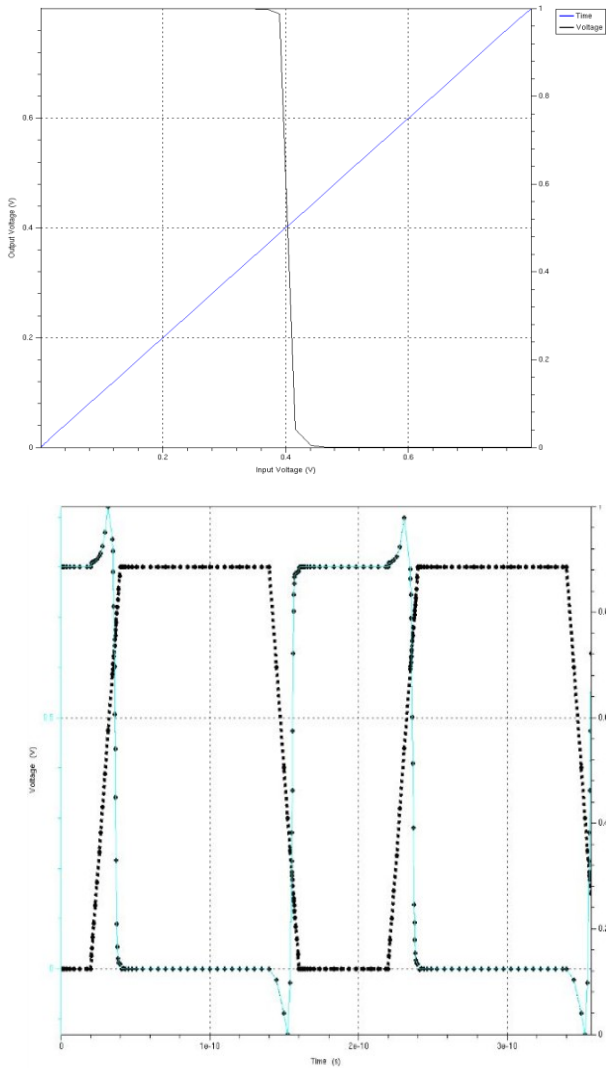


Fig. 2. Voltage Transfer characteristics (top) and Transient response (bottom) of a Basic Inverter with nominal device dimensions.

C. Methodology used

Design of Experiments (DoE) and Response Surface Modeling (RSM) are well established branches of statistics. In these techniques, systematic method for experiment planning is used in order to conduct the experiments in an efficient way and enable designers to construct empirical models from which the output responses can be determined as a function of the input parameters. The RSM methodology is a combination of mathematical and statistical methods which are useful in developing analytical models and the analysis of problems in which a response of interest is affected by several input variable parameters and the aim is to optimize this output response [18].

The DoE and RSM techniques can provide a reasonable balance between accuracy and the computational efficiency as compared to the traditional techniques, such as Monte Carlo simulations by limiting the number and hence the runtime complexity of simulations because of its non random nature. Fig. 3, Shows the flow chart of the variability analysis utilized by the DoE/RSM techniques.

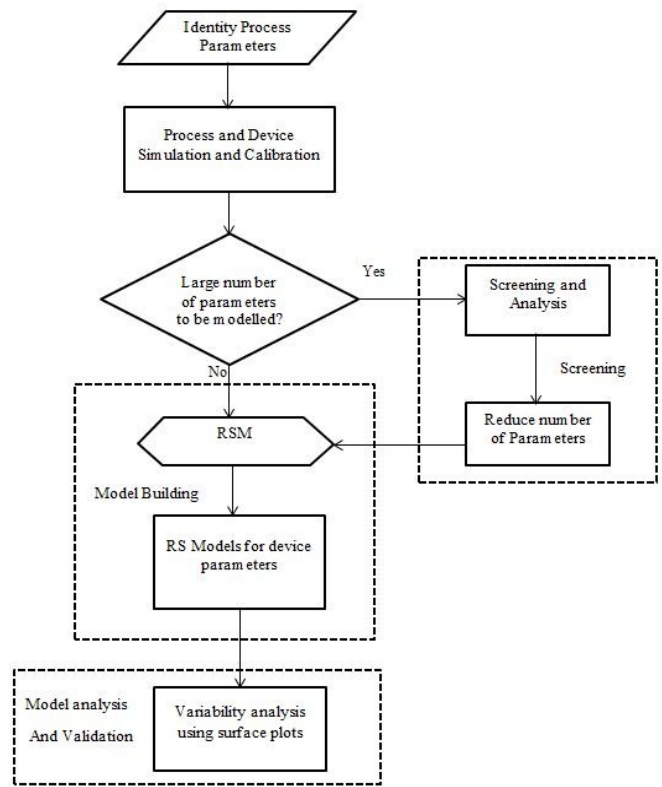


Fig. 3. Flow chart of variability analysis utilized by DoE/RSM statistical techniques.

III. DISCUSSION OF RESULTS

If variability in the process parameter affects the characteristics of the individual devices. Since the circuits consists of devices, the circuit performance is also affected by these variations [19]. As explained in the previous section, CMOS Inverter has been considered to analyze those circuit performance variations. The response parameters analyzed in this work are delay and static power dissipation, as they play a major role in optimizing the circuit performances. First section describes the individual and interaction effects of the process parameter variation on the delay of the FinFET inverter and second section describes the individual and interaction effects of the process parameter variation on the static power dissipation.

A. Effect of process variations on the Delay

Delay is a better figure of merit, since it takes into account the capacitance associated with the structure as well as the current drivability. The delay associated with inverter, T_d is given by the equation $T_d = \frac{C_{gg} \cdot V_{DD}}{I_{on}}$, where C_{gg} is the total gate capacitance which can be obtained by the Capacitance-Voltage characteristic of the inverter and V_{DD} is the supply voltage (0.8V).

Fig. 4, offers a simpler view of the relative effects via an ordered graph called a Pareto Chart. The inference from the Pareto chart is that, the variation in H_{fin} has the largest effect on the delay of the inverter. W_{fin} and T_{ox} have the second and third largest effects respectively. There is only one interaction effect that is significant i. e, H_{fin} and W_{fin} interaction.

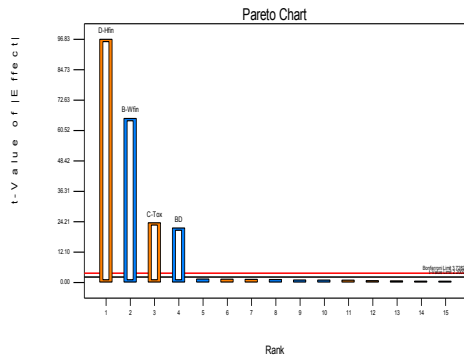


Fig. 4. Pareto chart for the delay

The interaction effect is shown by the interaction graph and contour graph in Fig. 5. The interaction graph shows that, the effect of variation in width of the fin on the inverter delay can be minimized by 21.13%, if the height of the fin is decreased by 12%. The delay of the inverter is found minimum for the low fin heights.

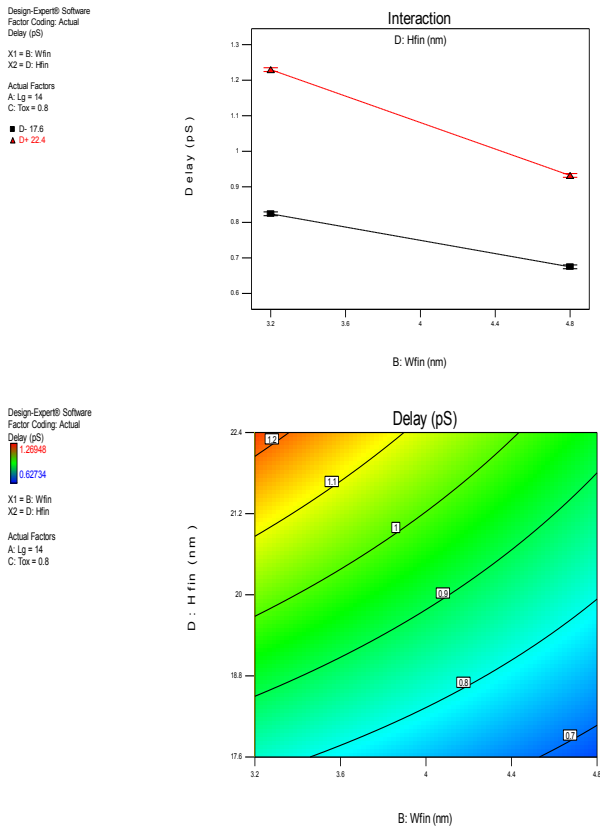


Fig 5. Interaction graph (top) and Contour graph (bottom) for Delay on the interaction effects of Hfin and Wfin.

B. Effect of process variations on the Static power dissipation

Power dissipation [20] of any logic gate in digital circuits can be expressed as:

$$P_{total} = P_{switching} + P_{static} + P_{sc} \quad (1)$$

where $P_{switching}$ and P_{sc} represents dynamic power dissipation due to charging, discharging of capacitances and dissipation due to short circuit current which flows through n and p FinFET for a fractional duration, when the output

signal of a logic gate makes a transition. P_{static} is the static power consumption due to the leakage current. The static power dissipation of the inverter is given by:

$$P_{static} = V_{DD} * I_{static} = V_{DD} * (I_{gate} + I_{off} + I_{btbt}) \quad (2)$$

In multigate SOI devices such as FinFETs, static power consumption is dominated by the subthreshold leakage and gate tunneling leakage [21]. In our FinFET devices, the body is left undoped, and the band-to-band tunneling leakage (I_{btbt}) becomes less significant. Static power consumption strongly depends on temperature, while dynamic power dissipation is weakly coupled with temperature variation, hence we do not consider the (I_{btbt}) components of leakage current in this paper.

Half normal probability plot, a graphical tool that uses the ordered estimated effects to help assess which factors are important and which are unimportant is shown in Fig. 6. Oxide thickness fluctuation has the most significant variation impact on static power dissipation. Although other individual effects of parameter variations and the interaction effects are less significant on the static power dissipation in CMOS FinFET inverter, the individual effect of variation in gate length and the interaction effect of both OTF and L_g variations are considerable. It can be shown by the Pareto chart in Fig. 7.

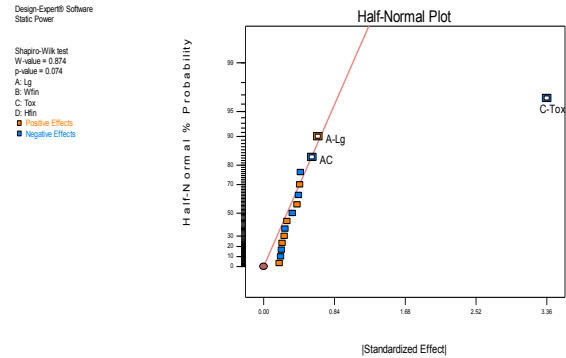


Fig. 6. Half normal plot for the standardized effects on Static power dissipation.

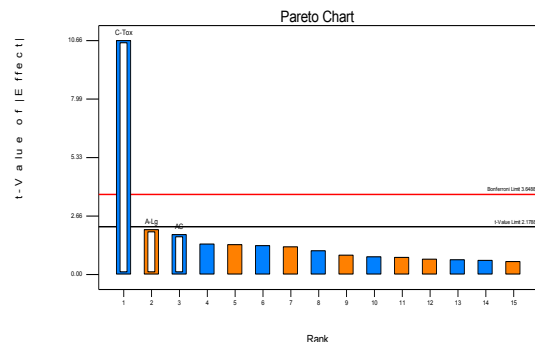


Fig. 7 Pareto chart for the Static power dissipation in FinFET Inverter.

The interaction graph and contour graph are shown in Fig 8, represents the variation of static power in regards to the interaction effect of OTF and variation in L_g . The analysis of interaction graph depicts that, the increment in gate oxide thickness by 10% can reduce the effect of L_g variability on static power dissipation by 85.28%. The static

power dissipation can be minimized by keeping the thicker gate oxide is observed from the contour graph.

Fig. 9. Comparison graph of actual and predicted values for delay (top) and static power (bottom) of Inverter.

IV. CONCLUSION

A full process flow for a 14-nm multi gate SOI FinFET has been implemented in this paper to analyze the effect of variability. The variability model is designed for different process parameter variations namely, Gate length, Fin width, Gate oxide thickness and Fin height. The impact of these process variations on the delay and the static power dissipation of a CMOS FinFET inverter are presented. Gate length variation in the devices has very less impact on the delay of the inverter gate. But the variability in fin dimension has considerable impact on it. The effect of variation in width of the fin on the inverter delay can be minimized by 21.13% if the height of the fin is decreased by 12%. So the minimization of the effects of variation in width of the fin can be accomplished by choosing the short fins.

The fin width and height variations have considerably less effect on the static power dissipation of inverter whereas fluctuation in gate oxide thickness has significant impact on it. The increment in gate oxide thickness by 10% can reduce the effect of L_g variability on static power dissipation by 85.28%. The effect of variation in static power can be minimized by choosing thicker gate oxide as it reduces the gate leakage current. Hence performance of the inverter degrades by increasing the Fin Height and with reduction in gate oxide thickness. The model provides the useful guidance to the circuit designer for low power, analog and digital applications in consideration to the importance of variation in device scalability. Further scope of work may include developing the variability model for the devices which uses high-k material for improving the performance.

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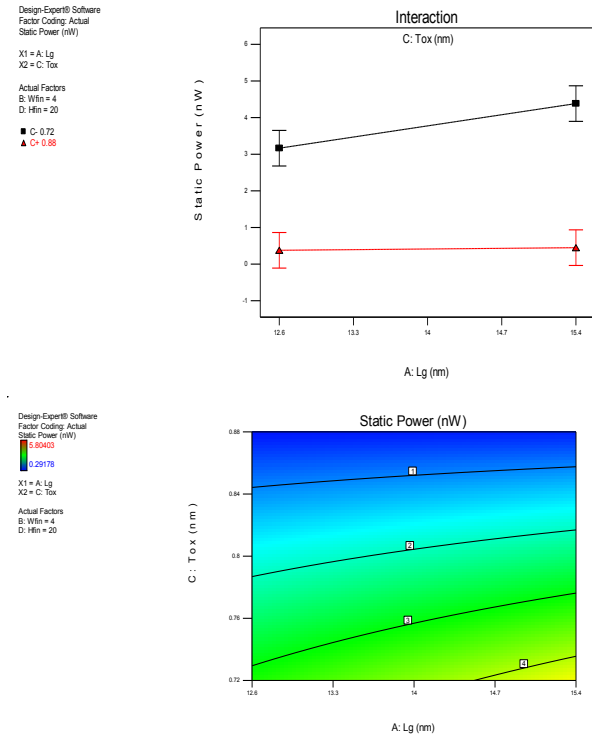
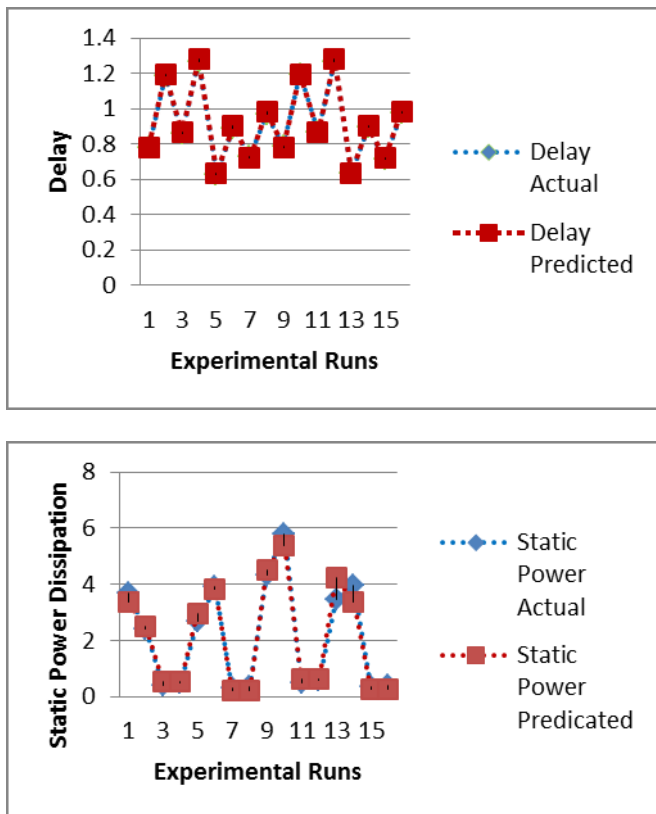


Fig. 8. Interaction graph (top) and Contour graph (bottom) showing the interaction effect of variations in L_g and Tox on Static power dissipation.

The comparison between the actual results obtained by simulation and the predicted values from the variability model is represented in Fig. 9, both for delay and static power dissipation in the inverter designed.



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