A Series-Parallel Switched Reduced Devices Multilevel dc-link Inverter Topology

Ritu Chaturvedi, Praveen Bansal

Abstract—**The paper presents a series parallel switched reduced devices multilevel dc link inverter topology. The medium voltage and high power requirements emphasize the need to carefully work out the increasing trend of using multilevel inverter in modern drives and utility application. It consists of an H-bridge and an inverter which output is multilevel voltage by switching the dc voltage sources in series and parallel. The initial aim of this paper is to achieve the reduced component count, diode for an appropriate voltage level. Circuit configuration, theoretical operation, and MATLAB-R2013a based simulations results are also discussed in this paper.**

Index Terms—Multilevel inverter (MLI), Switched series parallel, H-bridge, PWM

I. INTRODUCTION

In few years ago, electrical energy system, electric vehicles (EVs) productions are focused because of the global environment issues. The power electronics, converters and inverters, is a crucial technology is this system [1]-[6].

One of the issues raised in these studies is the limit of switching devices. If the devices which can endure high voltage are used in the inverter, their switching frequency is prohibited. On the other hand moving towards drive side the rotation speed of motor also affects the frequency of reference waveforms, as the speed of rotation gets increase than the frequency of reference waveforms also become increase. If the reference waveform frequency is close to the prohibited switching frequency the output waveform is distorted and the reliability of the motor is reduced. As legislation against the problem, a multilevel inverter which can use the low rated voltage device has been applied to Electric Vehicles (EVs), Hybrid Electric Vehicles (HEVs), HVDC, and UPS [1], [7]-[8].

The main drawback correlated with the multilevel configuration is their circuit complexities require a high number of power switches. A MLI can reduce the device voltage by increasing the number of output voltage level. On increasing the number of output voltage level, the number of switching devices is also increased, which makes a MLI more complicated [9]. MLI can be divided into three notable topologies: diode clamped MLI (DCMLI), flying capacitors MLI (FCMLI) and cascade H-bridge MLI (CHB) cells with separate DC sources [10-13]. In all of these, the diode-clamped MLI desires Complex PWM controls, because more capacitors and diodes are required for generating output level and adjusting the capacitor. When the FCMLI is applying, the circuit can consist of comparatively fewer elements. In the case of the cascade H-bridge multilevel inverter, every low voltage H-bridge module has an independent DC-link voltage source. Among these topologies, the cascaded H bridge inverter has received much attention. To increase the output voltage levels, the number of H bridges must be connected in cascade, hence greater number of power semiconductor switches is required. Each switch requires a related gate drive and protection circuits. This may cause the overall system to be more expensive and complex.

Key issue for the modulation of MLI is removal of output harmonics. Switching method in fundamental frequency essentially eliminate the certain high order harmonics by changing the switching time [14].In this paper, a new topology is composed of Voltage sources that are connected in series/parallel by the switching devices makes it easily extendible to higher number of output voltage level allied with less number of switches. The THD of the output voltage waveform are also diminished. Capacitors, batteries, and other dc voltage sources can be used as the voltage sources of the proposed inverter. Therefore, the proposed multilevel inverter can be applied to grid connected PV systems etc., with keep these benefits [15].

II. PROPOSED TOPOLOGY

Power circuit topology of the proposed multilevel inverter is shown in Fig.1. As shown in this figure, inverter is constructed from two parts. Part one is an H-bridge inverter with DC voltage source equal to V_0 and part two is an inverter with DC voltage sources equal to V_k (k = 1, 2,…, n) . DC voltage sources V_0 ~V_n are independent each other, and it is assumed that V_0: V_k = 1: 2 (k = 1, 2,…, n) . Switches S_{a1} ~ S_{an-1} and S_{b1} ~ S_{bn-1} are the switches which switch the DC voltage sources in series. The proposed inverter is driven by the hybrid modulation method [1].

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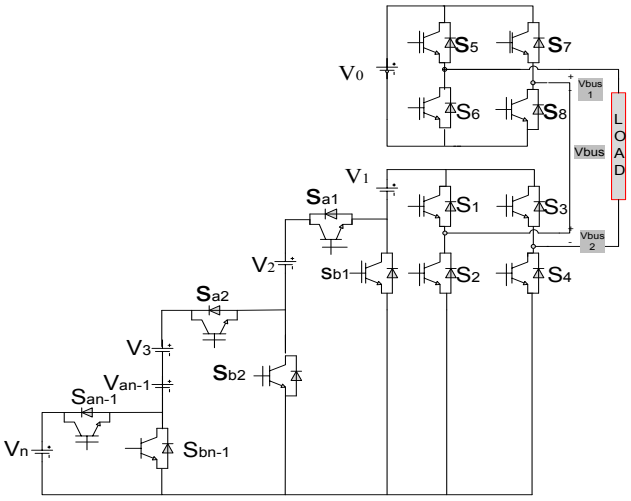

Fig.1. Structure of the proposed (4n+3) level inverter

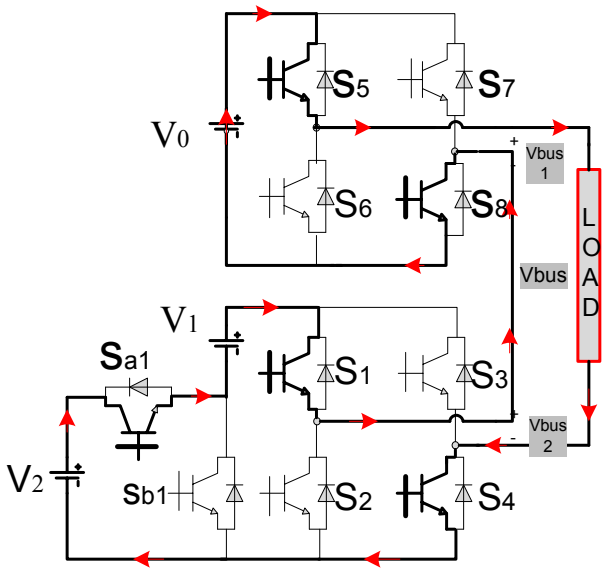

Fig (a)

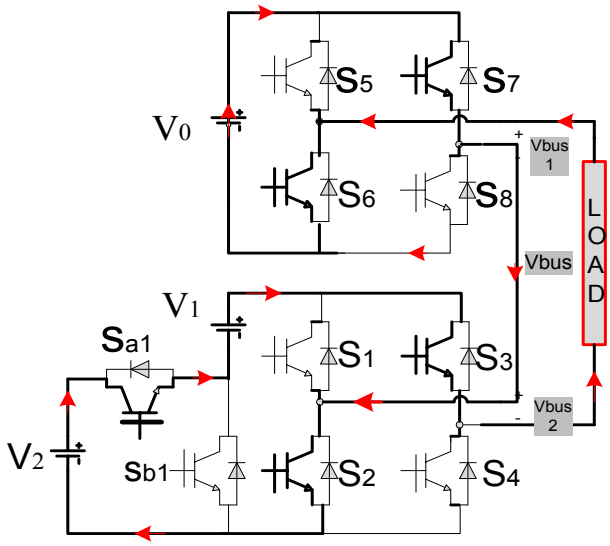

Fig (b)

Fig.2. Switching combinations of series parallel switched reduced devices multilevel dc link inverter topology for,Fig (a) +15 level and Fig (b) -15 level. [17].

The operating modes of the 15-level MLI topology are explained for one level (+15 & -15) as shown in fig.2(a) and fig.2(b). Switches Sa2 and Sb2 will be extended above 15 level in the propose topology. Using this series conversion of DC voltage sources, the lower H-bridge outputs V_{bus2} in (2n +1)-level, while the upper H-bridge outputs $V_0 = V_{bus1}$. The proposed multilevel inverter outputs (4n + 3) level by $V_{bus1} + V_{bus2}$ or $V_{bus2} - V_{bus1}$. If the conventional CHB inverter is driven by hybrid modulation method, then 12 switching devices are require for 11-level, and 16 switching devices are required for 15-level [13]. On the other hand, the proposed inverter requires 10 devices for 11-level and 10 devices for 15-level. In addition, when the ratio of the voltage of the sources V_0: V_k = 1: 3 is assumed, the proposed inverter requires 10 devices for 15 level. Therefore, the proposed inverter can increased the number of output voltage level by changing the ratio of the voltage source as like conventional CHB inverter.

In other conventional inverters such as CHB, DCMLI and FCMLI, a similar scheme can be used [16]. However, the Cascaded H-bridge, Diode clamped and Flying capacitor inverters require 28 switches for 15-level. Therefore, the proposed multilevel inverter requires the less number of switching devices than CHB, DCMLI and FCMLI. When the proposed inverter is applied to some application without reverse power flow, switches S_{b1}~S_{bn-1} can be replaced by diodes. For example, when a resistive load is connected to the output of the proposed inverter, the output current is accorded with the voltage phase.

TABLE I. COMPARISON BETWEEN TOPOLOGIES FOR 15 LEVEL

Multilevel inverter structure	Cascaded H-bridge	Diode clamped	Flying capacitor	Proposed MLI
Main switches	28	28	28	10
Bypass Diodes	-	-	-	-
Clamping Diodes	-	24	-	-
DC split capacitors	-	6	6	-
Clamping capacitors	-	-	12	-
DC sources	7	1	1	3
Total	35	59	47	13

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TABLE II. LOOK UP TABLE FOR THE PROPOSED 15-LEVEL INVERTER

VOLTAGE LEVEL	SWITCHES										Output Voltage
	SA1	*SB1*	*S1*	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*	
7	✓		✓			✓	✓			✓	$+7V_{dc}$
6	✓		✓			✓		✓		✓	$+6V_{dc}$
5	✓		✓			✓		✓	✓		$+5V_{dc}$
4		✓	✓			✓	✓			✓	$+4Vd_c$
3		✓	✓			✓		✓		✓	$+3V_{dc}$
2		✓	✓			✓		✓	✓		$+2V_{dc}$
1				✓		✓	✓			✓	$+1V_{dc}$
0				✓		✓		✓		✓	$0V_{dc}$
-1				✓		✓		✓	✓		$-1V_{dc}$
-2		✓		✓	✓		✓			✓	$-2Vd_c$
-3		✓		✓	✓			✓		✓	$-3V_{dc}$
-4		✓		✓	✓			✓	✓		$-4V_{dc}$
-5	✓			✓	✓		✓			✓	$-5V_{dc}$
-6	✓			✓	✓			✓		✓	$-6V_{dc}$
-7	✓			✓	✓			✓	✓		$-7V_{dc}$

III. MODULATION TECHNIQUES

In this section, the modulation techniques of the proposed inverter are explained 15 level inverter. Fig.3 shows the modulation techniques of the proposed 15 level inverter. In the modulation techniques, there are three alternative PWM strategies with different phase relationships for the level-shifted multicarrier modulation:

A. Phase opposition disposition (POD),

B. Alternate phase disposition (APOD), and

C. In-phase disposition (IPD)

A. Phase opposition disposition pulse width modulation (POD PWM):- In this modulation scheme all carrier waveform above zero reference are in phase and below zero reference are 180˚out of phase as shown in Fig 3.1.

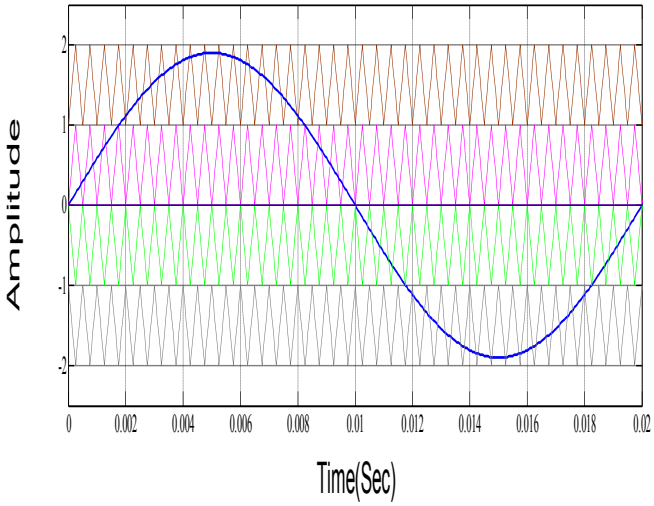

Fig. 3.1

B. Alternate phase opposition disposition pulse width modulation (APOD PWM):- In this modulation scheme every carrier waveform is in out of phase with its neighboring carrier wave by 180˚ shown in Fig. 3.2

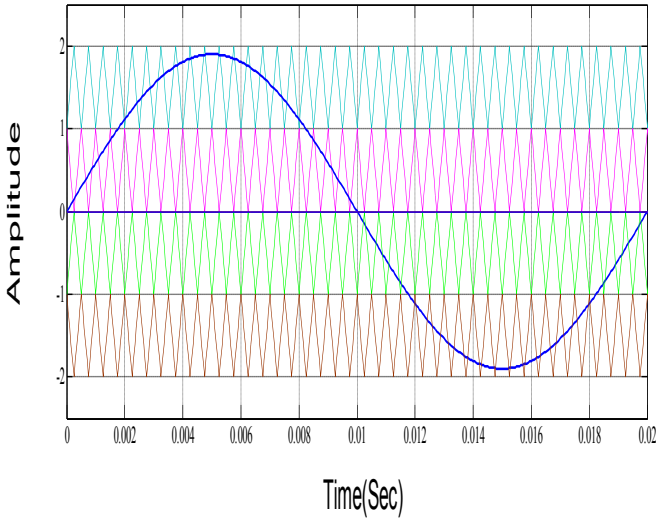

Fig.3.2

C. In Phase disposition pulse width modulation (PDPWM):-In this modulation scheme all carrier waveforms are in same phase shown in Figure 3.3 for N-1 carriers where N is number of level. In proposed, a multilevel inverter with m level requires m-1 triangular carriers. In phase disposition PWM, all the triangular carriers have same frequency.

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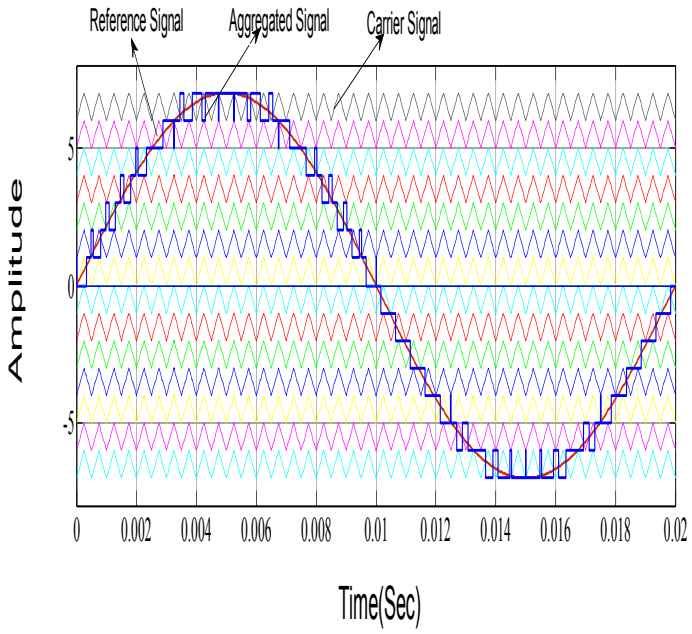

Fig.3.3 Associated waveforms for control and modulation of the proposed inverter for n=3

IV. SIMULATION RESULT

In this section, the simulation results of the 15-level and 11-level for the proposed multilevel inverter, using series- parallel switching multilevel dc-link inverter topology are simulated by MATLAB R2013a software module. The parameter of the simulation are as following R=2 ohms, L=5Mh, dc source voltage is 70V; Frequency of carrier signal is 2 kHz. In this topology, in the carrier based implementation, the phase disposition PWM scheme is used.

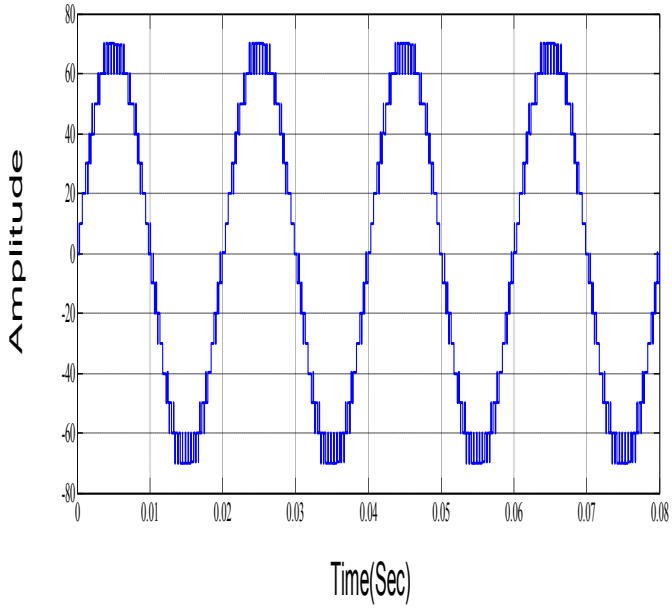

Fig. 4 Simulated 15-level phase voltage generated by PDPWM technique for RL-load

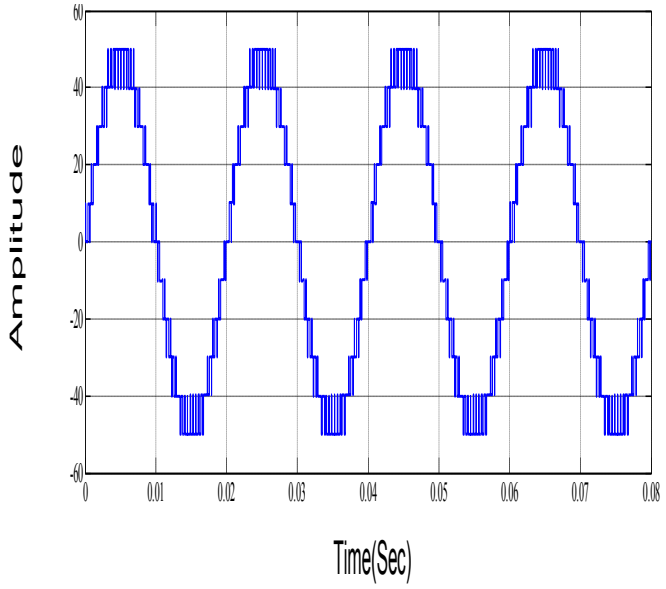

Fig. 5 Simulated 11-level phase voltage generated by PDPWM technique for RL-load

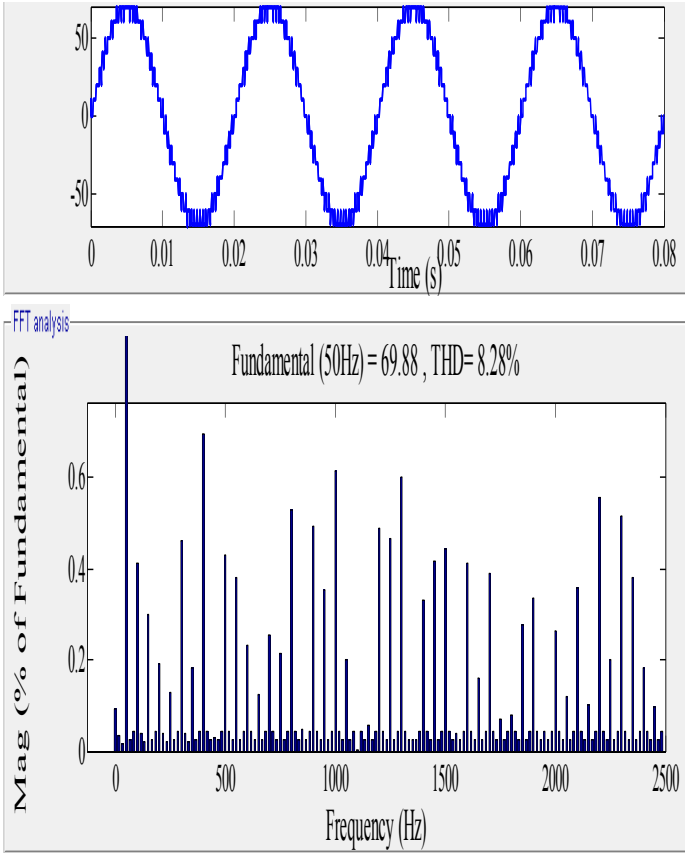

Fig. 6 FFT - Harmonic spectrum output of PDPWM strategy at ma=1

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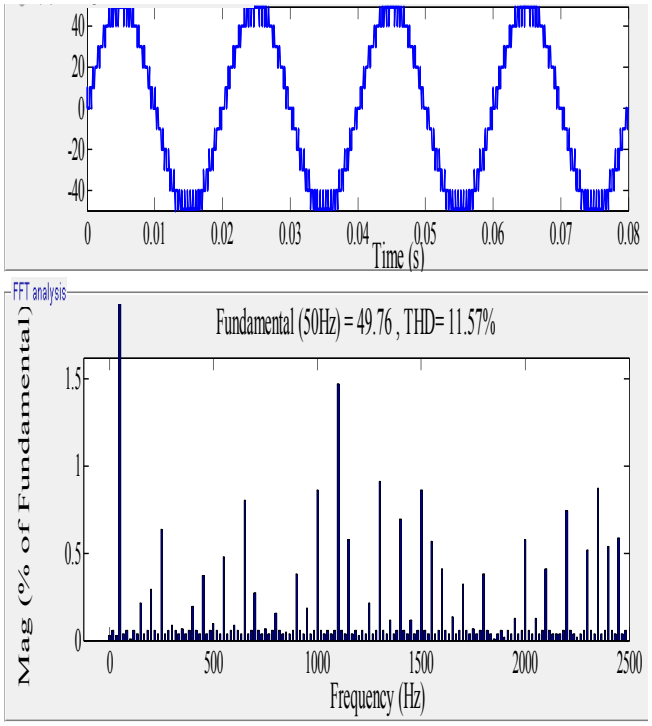

Fig.7 FFT - Harmonic spectrum output of PDPWM strategy at $m_{a=1}$

TABLE III. COMPARISON OF THE CALCULATED THD

Modulation index	% THD 11-level	% THD 15-level
1.1	10.45	7.65
1	11.57	8.28
0.95	13.03	9.13
0.90	13.40	9.37
0.85	13.66	9.93
0.80	14.46	10.77

V.CONCLUSION

A series-parallel switched reduced devices multilevel dc-link inverter topology with reduced number of switches and low output harmonics proposed. This topology is simulated with the help of MATLAB-SIMULINK at different value of modulation index m_a. For 15-level at m_a=1, THD is 8.28% and for 11-level at m_a=1, THD is 11.57%, which is less than as comparison to DCMLI. The proposed inverted can produce more number of voltage level with the same number of switches compared to the conventional inverters. Therefore, the size and power consumption of driving circuit of the proposed inverter are reduced. The simulation result and modulation method are shown in this paper. The proposed inverter can also reduce the THD of its output waveform. So the output waveform of inverter is better than the conventional multilevel inverter from THD point of view and mostly used in high power application like EV and HEV drives.

ACKNOWLEDGMENT

The authors sincerely acknowledge the Director, MITS, Gwalior, India to carry out this work.

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