Biased Charge Reuse Technique in Non Parallel Circuits with Efficient Logic Gates

Syed.Saba tharunam,G.MuniRatnam

*Abstract:***This paper presents Biased Charge Reuse (BCR) Technique in non parallel circuits with efficient logic gates.Non parallel circuit consists of n-pipeline stages.Each pipe line stage in Non parallel circuit consists of 2-input OR gate which will detects whether the code is valid or not,hand shake controller which will provide power to Efficient logic gates by hand shaking with neighbouring stages.Efficient logic gates (AND, NAND) or (OR,NOR) gates which implement the logic function of the stage,unused efficient logic gates are powered off and thus have less leakage power dissipation,BCR technique is used in Non parallel circuits due to which part of the charge on the output node of Efficient Logic gate entering in to liberation phase can be reused to charge the output of another Efficient logic Gate which is being weigh up decreasing power dissipation required to complete the evaluation of efficient logic gate,in addition instead of C-element in handshake controller we are going to use enhanced c-element due to which Efficient Logic gate will be powered off when its output is received by downstream pipeline stage.**

***Index Terms*—Biased Charge Reuse,Efficient Logic Ga tes,Low power VLSI,Non Parallel Circuis.**

I. INTRODUCTION

Reducing power dissipation is a major anxiety in now a days.power dissipation is classified in to two types i.e,static power dissipation,dynamic power dissipation.Dynamic power dissipation is power dissipated when the device is active. Static power dissipation is nothing but power dissipated when the device is power-driven but no signals are changing the values,i.e. Static power dissipation is due to the leakage currents ,most probably we will face this problem in Non parallel circuits.

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To reduce this problem in Non parallel circuits (Asynchronous) in Existing method they introduced Efficient AND,NAND logic gates in each pipeline stage of Non parallel circuit, which implement the logic function of the stage.unused efficient logic gates are powered off and thus have less leakage power dissipation,two-input OR gate which will detects whether the code is valid or not,Hand shake controller which will provide power to Efficient logic Gate by handshaking with neighbouring stages.

To reduce more leakage power dissipation and power dissipation required to complete the evaluation of efficient logic gate we proposed a Biased Charge Reuse (BCR) Technique in Non parallel circuits with efficient logic gates(AND,NAND as well as OR,NOR). Due to BCR with efficient logic gates part of the charge on the output node of Efficient Logic gate entering in to liberation phase can be reused to charge the output of another Efficient logic Gate which is being weigh up decreasing power dissipation required to complete the evaluation of efficient logic gate,in addition instead of C-element in handshake controller we are going to use enhanced c-element due to which Efficient Logic gate will be powered off when its output is received by downstream pipeline stage.

The remaining paper is organized as follows.In section II we present the Non parallel circuits(Asynchronous) with efficient AND,NAND logic gates and explain about hand shake controller, two-input OR gate, efficient AND,NAND logic gates,C-element.In section III we present the Non parallel circuits with efficient OR,NOR logic gates & Biased Charge Reuse (BCR) Technique in Non parallel circuits with efficient logic gates(AND,NAND as well as OR,NOR) and explains about enhanced C-element.In section IV we present the simulation results .Lastly in section V we present the conclusion.

II. EXISTING METHOD

Non parallel circuit with efficient (AND,NAND) Logic gate is as shown in fig 1.consists of three pipeline stages.Each pipe line stage consists of Efficient logic gate which implement the logic function of the stage, hand shake controller which will provide power to Efficient logic gates by hand shaking with neighbouring stages, hand shake controller consists of 2-input OR gate ,C-element.2-input OR gate which will detects whether the code is valid or not, unused efficient logic gates are powered off and thus have

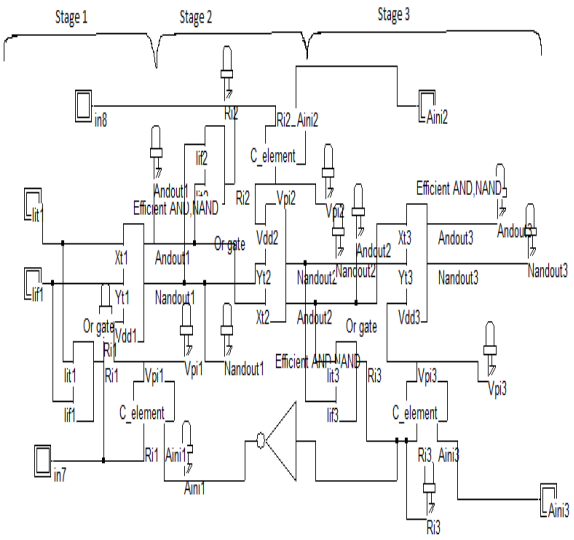
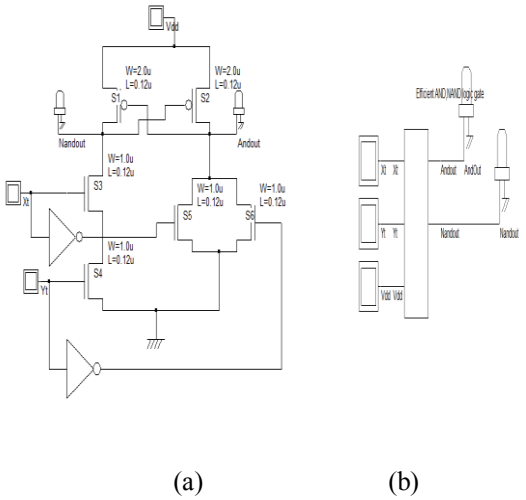


Fig. 1.Non parallel circuit with Efficient AND,NAND logic gate



(a) (b)

Fig.2.Efficient Logic Gate.(a)Structure of Efficient AND, NAND Logic Gate.(b)Symbol of Efficient AND,NAND Logic Gate.

less leakage power dissipation.

A. *Operation*

Case i) For inputs(1,1 or 1,0 or 0,1) Ri1=1,Let us consider the inputs as 1,1 then Ri1=1,if Aini1=0 i.e, if acknowledgement is zero from the third stage then Vpi1 is high.The power from Vpi1 is supplied to Vdd1,then the Efficient(AND,NAND) Logic Gate in first pipeline stage computes its logic function. .i.e, And out1=1,Nand out1=0**.**Next the outputs of first stage will be given to the efficient Logic Gate in stage 2 as well as they are detected by two input or gate in stage 2.As Ri2=1,Aini2=0 then the output of C-element Vpi2 in second stage will be given to Vdd of efficient Logic Gate in stage 2.then the logic gate computes its logic function then the output of the logic gate will be given to to the Efficient Logic Gate in stage 3 as well as they are detected by two input or gate in stage 3. As Ri3=1,Aini3=0 then Vpi3 will be high then output of Efficient Logic Gate in stage 3 is zero for And out3,1 for Nand out 3 as stage 2 outpus are zero for And out2 ,one for Nand out2.

Case ii)For inputs(0,0) Ri1=0,if Aini1=1i.e, if acknowledgement is one from the third stage then Vpi1 &Vp3 will be low. i.e,leakage power is reduced by switching off the first two stages to evaluate the stage 3.

B. *Efficient AND,NAND Logic Gate*

Efficient AND,NAND Logic Gate is as shown in fig 2. Among other logic families they are simple,charge reusable and Efficient .so we had selected these gates in non parallel circuits.Efficient Logic Gate adopts double-rail information encoding i.e.each input to Efficient Efficient Logic Gate requires together polarities to be present,and every Efficient Logic gate computes both a logic function and its compliment.Efficient Logic gate get their power from Vpi instead of dc supply.i.e.in each stage of Non parallel circuit with Efficient Logic gate the output of hand shake controller VPi is connected to vdd.

When vdd is 0(wait phase)then the output will be zero independent of inputs,when Vdd is in between 0 to Vdd(evaluation phase) then Efficient Logic gate will performs the operation and generates the outputs.when Vdd is from Vddto 0(Discharge phase) then the output will discharges to zero. when Vdd is at Vdd(hold phase) output becomes valid even though the inputs are low.Let us assume Vdd is in between 0 to Vdd and both Xt,Yt both are high in fig2 then s3 is high,S4 is high and nand out clamped to zero, then S2 will be on so And out will be high.Then the outpUt of Efficient Logic gate will given as input to next stage Efficient Logic gate.

C. *Hand shake controller*

Hand shake controller will provide power to Efficient logic gates by handshaking with neighbouring stages. Hand shake controller consists of two components one is c-element another is two input or gate.

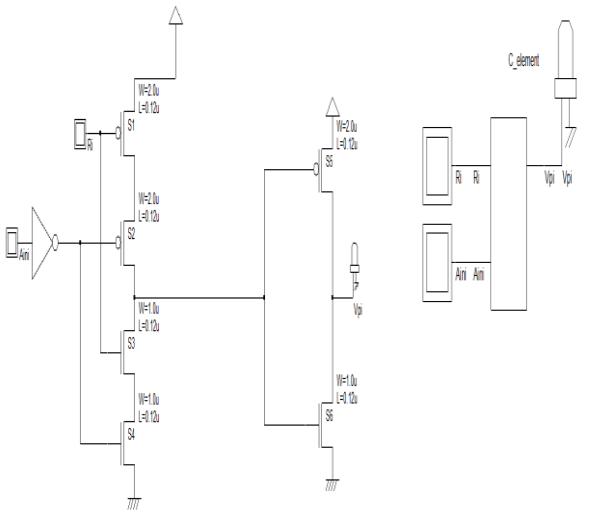


Fig. 3. C-element (a) construction of C-element.(b) C-element symbol

1. C-element

C-element is as shown in Fig.3.Case i:when Ri=1,Aini=0 then output Will be high.

Case ii:when Ri=0,Aini=1 then output will be low,in remaining cases output will be in high impedance state.let us consider the first case i.e, when Ri=1,Aini=0 then s3,s4 will be ON and S1,S2 will be off then S5 will be on then output Will be high.

2. Or gate

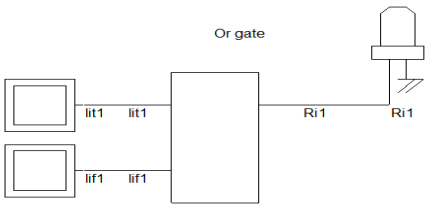


Fig. 4.Or Gate Symbol

The Or gate is as shown in above fig. 4.Or gate is used to detect the inputs.when any one of the input is high then it will detects the valid code word i.e Ri=1. Else it will shows Ri=0.

III. PROPOSED METHODS

1.Non Parallel Circuit With Efficient OR,NOR Logic Gate

Non parallel circuit with Efficient OR,NOR Logic Gate is as shown in fig. 5..consists of three pipeline stages.Each pipe line stage consists of Efficient logic(OR,NOR) gate which implement the logic function of the stage, hand shake

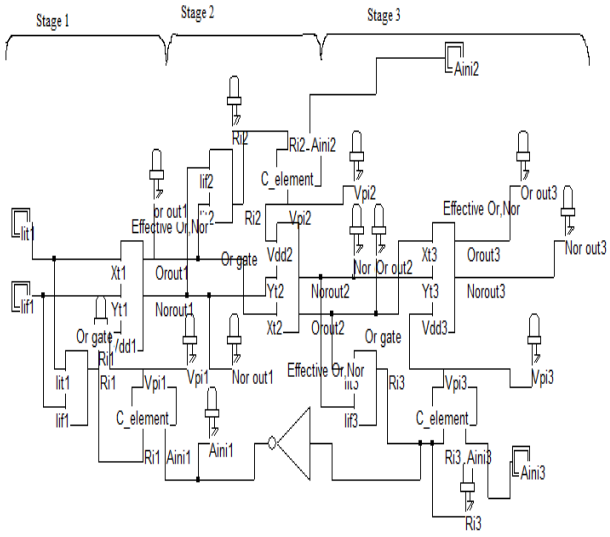


Fig. 5.Non parallel circuit with Efficient OR,NOR Logic Gate

controller which will provide power to Efficient logic gates by hand shaking with neighbouring stages, hand shake controller consists of 2-input OR gate ,C-element.2-input OR gate which will detects whether the code is valid or not, unused efficient logic gates are powered off and thus have less leakage power dissipation.

A. Operation

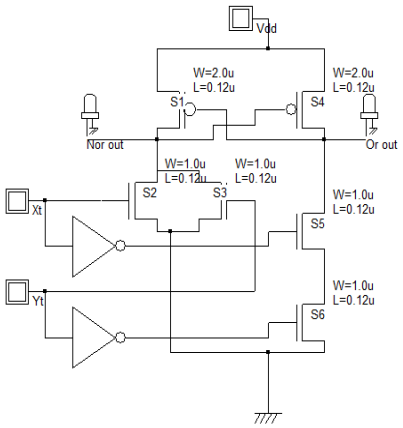
Case i)For inputs(1,1 or 1,0 or 0,1) Ri1=1.

Let us consider the inputs as 1,1 then Ri1=1,if Aini1=0 i.e, if acknowledgement is zero from the third stage then Vpi1 is high.The power from Vpi1 is supplied to Vdd1,then the Efficient or,nor logic gate in first pipeline stage computes its logic function i.e, Or out1=1,Nor out1=0.Next the outputs of first stage will be given to the Efficient logic gate in stage 2 as well as they are detected by two input or gate in stage 2.As Ri2=1,Aini2=0 then the output of C-element Vpi2 in second stage will be given to Vdd of efficient logic gate in stage 2.then the logic gate computes its logic function then the output of the logic gate will be given to to the Efficient logic gate in stage 3 as well as they are detected by two input or gate in stage 3. As Ri3=1,Aini3=0 then Vpi3 will be high then output of Efficient Logic gate in stage 3 is one for OR ,0 for NOR as stage 2 outpus are zero for And ,one for Nor.

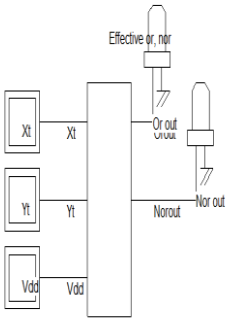
Case ii: For inputs(0,0) Ri1=0.

if Aini1=1 i.e, if acknowledgement is one from the third stage then Vpi1&Vp3 will be low.i.e,leakage power is reduced by switching off the first two stages to evaluate the stage 3.

B. Efficient OR,NOR Logic Gate



(a)



(b)

Fig.6 .Efficient OR,NOR Logic Gate.(a)Structure of Efficient OR,NOR Logic Gate.(b)Symbol of Efficient OR,NOR Logic Gate

The working of efficient OR,NOR Logic Gate is same as Efficient And,Nand Logic Gate but here we have to implement Or ,nor logic in pull down network i.e, S2,S3 must and should be connected in parallel,S5,S6 must be connected in series.

2. Biased Charge Reuse Technique In Non Parallel Circuits With Efficient AND,NAND Logic Gates

The Structure of Biased Charge Reuse Technique In Non Parallel Circuits With Efficient And ,Nand Logic Gates is as shown in fig is same as Non parallel circuit with efficient AND,NAND logic gates. but Enhanced C-element is used instead of C-element because of Enhanced C-element the Efficient And,Nand Logic Gates can get early discharging if its outputs are not required due to which leakage dissipation is reduced.as well as BCR technique is used due to which we are going to reduce power dissipation.

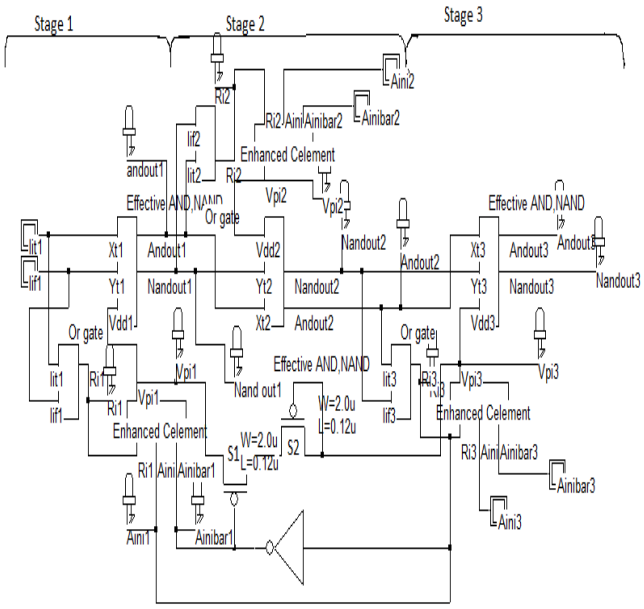
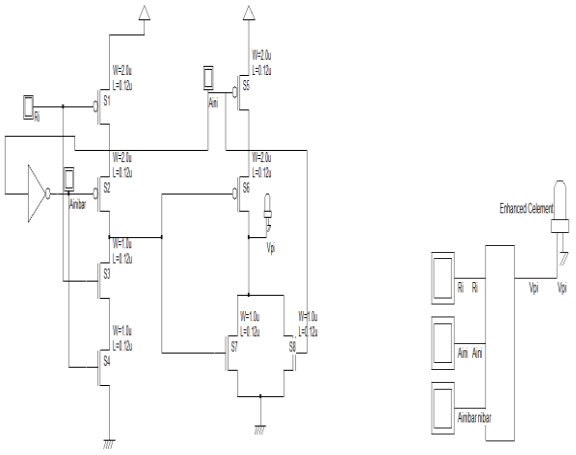


Fig. 7. Biased Charge Reuse Technique In Non Parallel Circuits With Efficient And ,Nand Logic Gates

A. Enhanced C-element



(a) (b)

fig.8.EnhancedC-element.a)Structure of Enhanced C-element b)Symbol of Enhanced C-element.

Operation:Casei:whenRi(Request)=1,Aini(Acknowledgement)=0 then output Will be high.
Caseii: whenRi=0 or1,if Aini (Acknowledgement) =1 then output will be low.let us consider the second case i.e, when Ri=1,Aini=1 then s1, S4,S5,s6 will be off and S2, s3,S7, S8will be ON then the output Will be low.i.e,request may be high or low but if the Acknowledgement is 1 then the output will be low(discharges to zero fastly than C-element) reducing more leakage dissipation than the C-element.

B. Biased Charge Reuse Technique

Due to BCR with efficient logic gates part of the charge on the output node of Efficient Logic gate entering in to liberation phase can be reused to charge the output of another Efficient logic Gate which is being weigh up decreasing power dissipation required to complete the evaluation of efficient logic gate.as shown in above fig BCR technique consists of two transistors S1,S2.S1 is used as key which will be turned ON when charge reuse is activated.S2 is used as a diode which allows the current to flow in only one direction i.e, from Vpi1 to Vpi3,S2 will be ON when Vpi1 is greater than Vpi3.

Operation:Let us consider lit1=1,lif1=1 When Ri=1,Aini=1 if acknowledgement is one from the third stage then Vpi1 is low reducing more leakage dissipation.As Vpi1 is low then the S1 transistor will be ON i.e, charge reuse is activated i.e due to which part of the charge on the output node of Efficient Logic gate in first stage entering in to liberation phase can be reused to charge the output of another Efficient logic Gate in stage 3 which is being weigh up decreasing power dissipation required to complete the evaluation of efficient logic gate and S2 will be off Because Vpi1 is Less than Vpi3.As Ri3=1,Aini3=0 Vpi3 will be high then the then output of Efficient AND,NAND Logic Gate in stage 3 is zero for AND,1 for NAND because the inputs of Second stage are 1,0.

3. Biased Charge Reuse Technique In Non Parallel Circuits With Efficient Or,Nor Logic Gates

Biased Charge Reuse Technique In Non Parallel Circuits With Efficient Or,Nor Logic Gates which is shown in fig 9. is Same As Biased Charge Reuse Technique In Non Parallel Circuits With Efficient And,Nand Logic Gates but here we are using Efficient Or,Nor logic gates in each pipeline stage instead of Efficient And,Nand Gate.

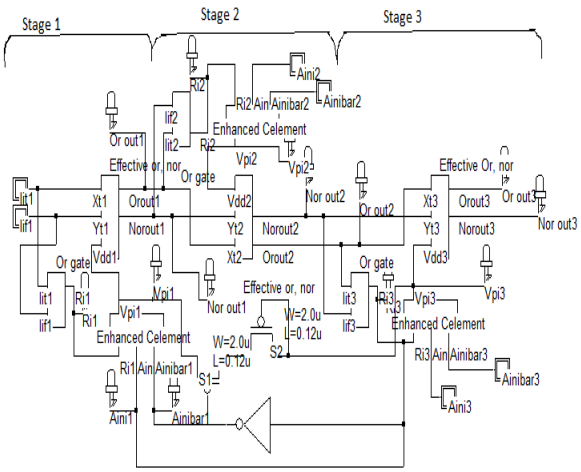


Fig.9 Biased Charge Reuse Technique In Non Parallel Circuits With Efficient Or,Nor Logic Gates

IV. SIMULATION RESULTS

Simulations are performed in Digital Schematic tool,power dissipation is Observed in Microwind tool

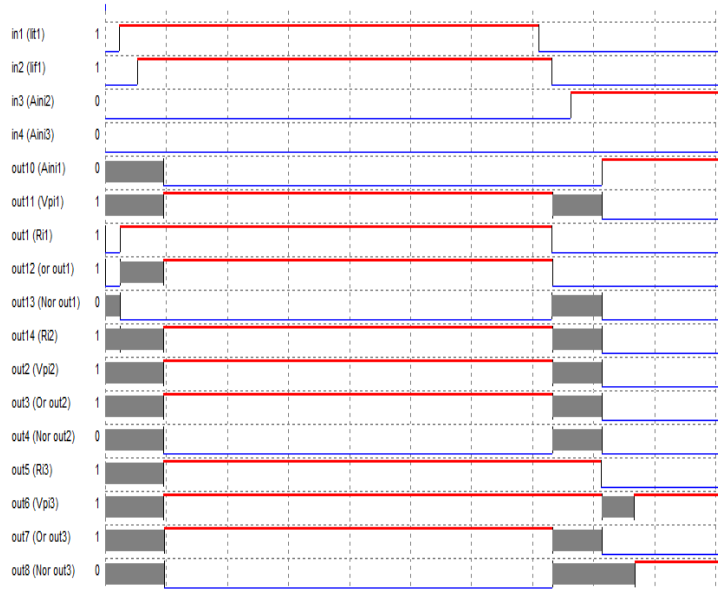


Fig.10 . Simulation Wave Forms For Non Parallel Circuit With Efficient OR,NOR Logic Gate

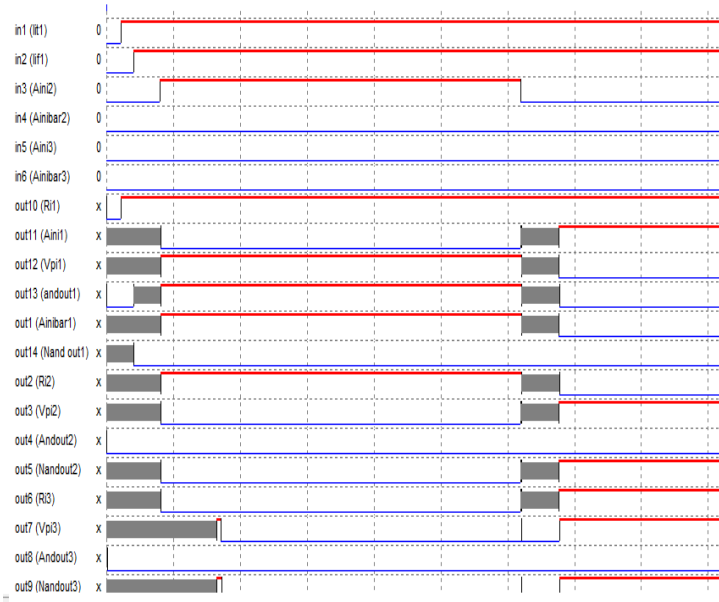


Fig.11 .Simulation Wave Forms Of Biased Charge Reuse Technique in Non Parallel Circuits With Efficient And,Nand Logic Gates

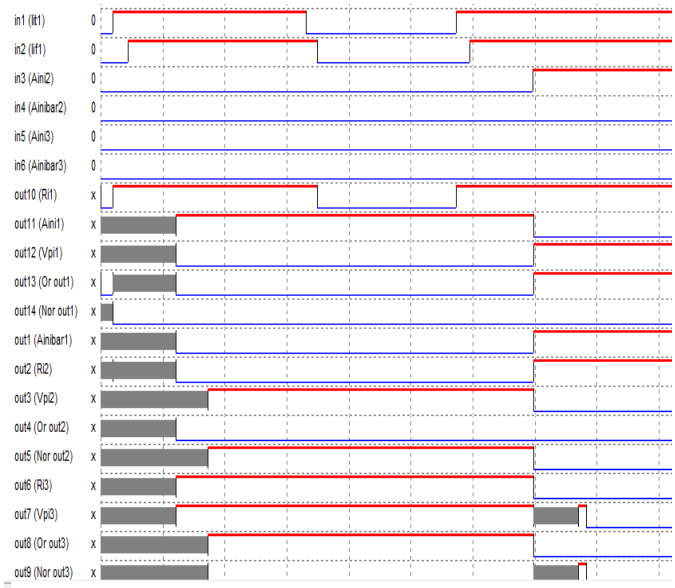


Fig.12 .Simulation Wave Forms Of Biased Charge Reuse Technique In Non Parallel Circuits With Efficient Or,Nor Logic Gates.

V. CONCLUSION

In this paper we presented Non parallel circuit with Efficient Or,Nor Logic Gate,Biased Charge Reuse (BSR)Technique In Non Parallel Circuits with Efficient

Logic Gates.The BSR Technique In Non Parallel Circuits With Efficient And,Nand Logic Gates Will have 15.819 % Less Power Dissipation Compared With Non Parallel Circuit With Efficient And,Nand Logic Gate for a time Scale of 100 ns. The BSR Technique in Non Parallel Circuits With Efficient Or,Nor Logic Gates Will have 6 % Less Power Dissipation Compared With Non Parallel Circuit With Efficient Or,Nor Logic Gate For a time Scale of 100 ns.

Future Scope:

We can implement Carry look ahead adder by using this logic to reduce the leakage dissipation as well as power dissipation.

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