Bridgeless Buck Converter with Average Current Mode control for Power Factor Correction and Wide Input Voltage variation

Vidhya K.G, Neethu K. paul, Binitha T.M.

Abstract— **In universal-line voltage (90-264 V) applications, maintaining a high efficiency across the entire voltage range poses a major challenge for ac/dc rectifiers that require power factor correction (PFC). Bridge diode rectifier followed by a boost converter is the most commonly used circuit for power factor correction in universal line application because of its simplicity and good performance. However, a boost PFC front-end exhibits 1%-3% lower efficiency at 100 V line compared to that at 230 V line. Bridgeless Buck converter with Voltage Doubler configuration can improves efficiency at low line of the universal line range compared with boost converter. This circuit reduces the number of diodes conducting each half cycle .Moreover, the rectifier doubles its output voltage ,which extends useable energy of the bulk capacitor after a dropout of the line voltage.**

Index Terms—**; Average Current Mode Control ; THD.**

I. INTRODUCTION

The rise in the industrial, commercial and residential consumers of electronic equipments has resulted in growing use of computers and electronic devices requiring mains supply. Rectification circuits incorporated with these devices act as nonlinear load to the power system and draws non-sinusoidal input currents. It results in the injection of current harmonics and causes low power factor operation of the power system.

Power Factor is an important performance parameter of a system and improving power factor is very much essential for the better and economical performance of the system. If the power factor of a system at a given power requirement is poor, then large value of Volt -Amperes or large amount of current is required by the system. Hence various measures should be taken to improve the power factor of a system

Moreover portable products are usually designed to operate at universal input voltages (90-264V).This wide input-voltage range has significant impact on the cost and efficiency of the power factor correction circuits. When these products are designed for universal input voltage, the efficiency will be several percentages lower than when operated at the local input range. Consequently, in addition to the loss of power, costs will be incurred for more expensive components and extra thermal management that are not necessary if the equipment is operated at the local input range.

Bridge diode rectifier followed by a boost converter has been the most commonly used power factor correction circuit .It has many advantages like very low THD; offers probably the best possible power factor ;High output voltage –volumetrically-efficient energy –storage capacitors ,good hold –up easy gate drive and switch current sense

Its drawback are that output voltage must always be set higher than the instantaneous AC input voltage-for universal or high-line AC input (up to 264 V), bus voltage must be set at about 400 V DC .This high voltage has detrimental effect on the switching losses of the boost converter and primary switches of the downstream dc/dc output stage.[2]Switching Losses causes the light-load efficiency to exhibit a steep fall off as the load current decreases .It requires a subsequent high-voltage primary regulation/isolation stage to step down to practical voltage levels required by most electronic loads. Common mode noise will also be high due to high bus voltage.

Moreover, a boost PFC front-end exhibits 1%-3% lower efficiency at 100 V line compared to that at 230 V line. This drop of efficiency at low line can be attributed to an increased input current that produces higher losses in semiconductors and input electromagnetic interference filter components.

At lower power levels, i.e., below 850W, the drawbacks of the universal line boost PFC front-end may partly be overcome by implementing the PFC front end with a buck topology. Lower input voltage to the dc/dc output stage has beneficial effects on its light-load performance. Lower voltage rated semiconductor devices can be used for the dc/dc stage and lower input voltage reduces the loss. Lower downstream.

voltages, improving robustness and reliability.Low bus voltage results in lower Common mode noise. In this paper, a bridgeless buck PFC rectifier that further improves the low-line (115 V) efficiency of the buck front-end by reducing the conduction loss through minimization of the number of simultaneously conducting semiconductor components is introduced. Because the proposed bridgeless buck rectifier also works as a voltage doubler, it can be designed to meet harmonic limit specifications with an output voltage that is twice that of a conventional buck PFC rectifier. As a result, the proposed rectifier also shows better hold-up time performance. Although the output voltage is doubled, the switching losses of the primary switches of the downstream dc/dc output stage are still significantly lower than that of the boost PFC counterpart.

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VidhyaK.G*,,M Tech Power Electronics,Vidya academy of Science and Technology, Thrissur, Kerala, India.*

Neethu K Paul*, M Tech Power Electronics,Vidya academy of Science and Technology, ,Kerala India,*

Binitha T.M*,Asst.Professor ,Vidya academy of Science and Technology, Thrissur, Kerala, India.*

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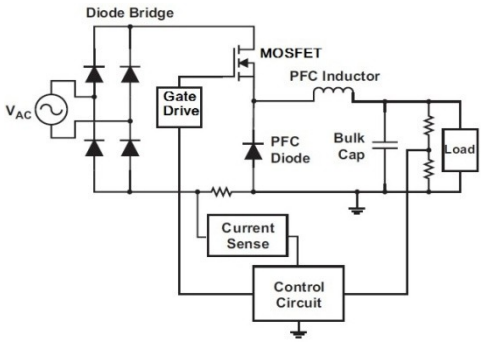

Figure 1:Bridge Rectifier followed by Buck Converter

II. CIRCUIT CONFIGURATION

A. *Bridgeless Buck with Voltage Doubler*

The circuit shown in Fig: 2 employs two back-to-back connected buck converters that operate in alternative halves of the line-voltage cycle. The configuration seems like consist of a full-bridge diode rectifier followed by two buck converters connected in parallel in series output manner. This configuration acts like a bridgeless configuration and full bridge losses are reduced. The process of shaping the input current is done by the Buck converter, which is properly controlled by the related circuitry

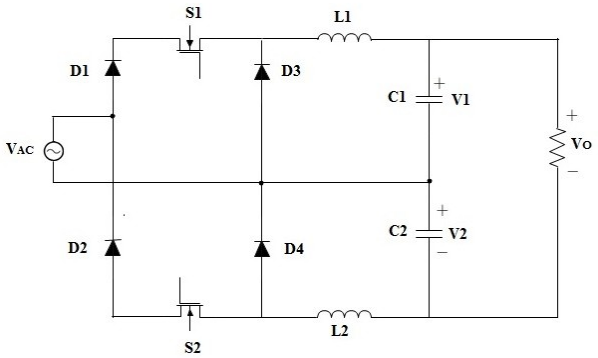

Figure 2:Proposed Circuit Topology.

B. *Positive half cycle operation.*

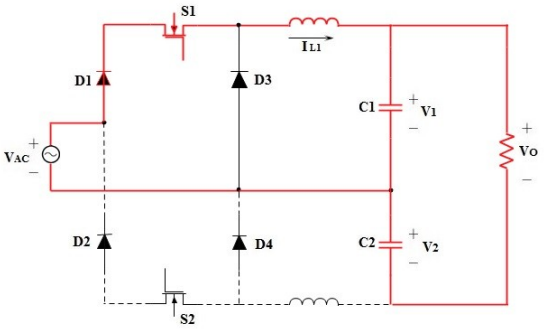

Figure3:Positive half cycle mode1

The buck converter illustrated in Fig. 3 only operates during positive half-cycles of line voltage V_{ac} and consists of a unidirectional switch implemented by diode D_1 in series with switch S_1, freewheeling diode D_3, filter inductor L_1, and output capacitor C_1. During its operation, the voltage across capacitor C_1, which must be selected lower than the peak of line voltage, is regulated by pulse width modulation (PWM) of switch S_1 .When the switch gets turned off the inductor current free wheels through the path D2,L1,C1.Inductor current flows through L1 only.

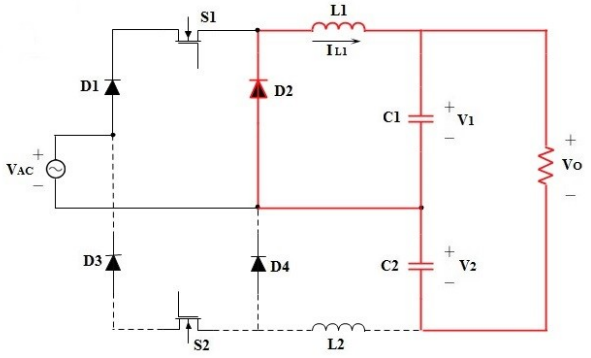

Figure 4: Positive half cycle mode 2

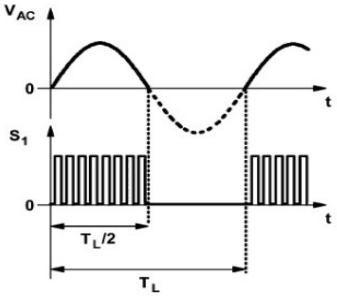

Figure 5: PWM for positive half cycle operation

C. *Negative Half cycle operation*

During the negative half cycle period the switch S1 gets turned off as diode D1 is reverse biased.The buck converter of this half cycle consist of a unidirectional switch implemented by diode D_2 in series with switch S_2 , freewheeling . diode D_4 , filter inductor L_2 , and output capacitor C_2 operates only during negative half-cycles of line voltage V_{ac} , as shown in Fig. 6. During its operation, the voltage across capacitor C_2 is regulated by the PWM of switch S_2 .Input current flows through the inductor L2.

When the switch gets turned off the current in inductor freewheels through D4,L2 and C2.

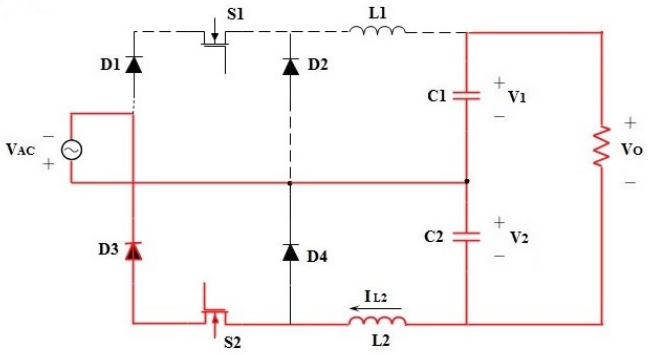

Figure 6: Negative half cycle Mode 3

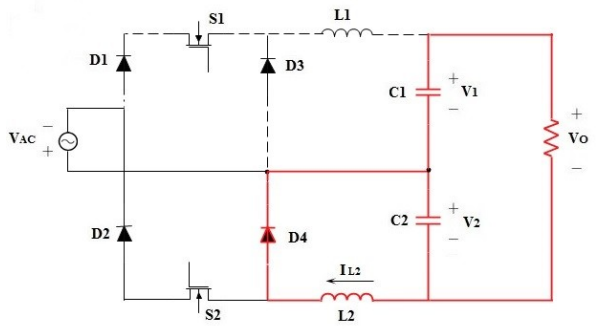

Figure 7: Negative half cycle Mode 4.

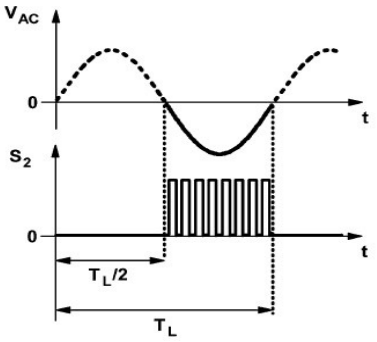

Figure 8: PWM for negative half cycle operation..

Input current always flows through only one diode during the conduction of a switch, i.e.,either D_1 or D_2 .

Efficiency is further improved as the circuit eliminates one of the input bridge diodes during conduction.

An additional advantage of the proposed circuit is its inrush current control capability. Since the switches are located between the input and the output capacitors, switches S_1 and S_2 can actively control the input inrush current during start-up. Output voltage V_{out} of the PFC rectifier, which is the sum of the voltages across output capacitors C_1 and C , is given by

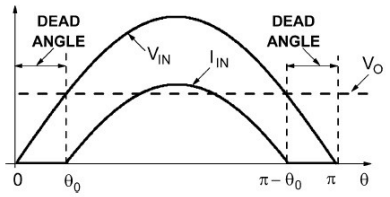

Figure 9: Ideal input voltage and input current waveforms of a PFC buck rectifier.

$$V_{out} = 2DV_{in} \qquad (1)$$

where D is the duty cycle and V_{in} is the instantaneous rectified ac input voltage. Relationship shown in (1) is valid for input voltages V_{in} greater than half the output voltage, i.e., for $V_{in} > V_{out}/2$.

When input voltage V_{in} falls below $V_{out}/2$, the converters do not deliver energy from the input to the output so the load current is maintained solely by the output capacitors. Because the PFC buck rectifier does not shape the line current during the time intervals when the line voltage is lower than the output voltage.[1]

The THD of the circuit will be high but less than 800W power levels the THD can be limited within acceptable limit.

III. CONTROL METHOD

Control method used in this circuit configuration is Average Current Mode Control. In this method, the buck regulator input current is forced or programmed to be proportional to the input voltage waveform for power factor correction. Feedback is necessary to control the input current.

Average current mode control for a Buck converter is as shown in figure 10.The inductor current passes through the sensing resistor and provides a voltage signal proportional to the inductor current. This voltage signal is fed to the current compensator as the average current feedback signal.

In Average current mode control multiplier/divider is used to generate the current reference signal Iref. Signal B is the voltage error amplifier output of the feed-back loop. Signal A is a signal representing the waveform of the rectified input current reference signal Iref in the current error amplifier which filters the inductor current. Output current error amplifier drives a PWM modulator.

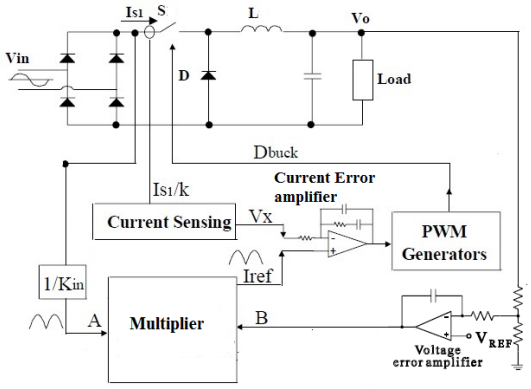

Figure 10 : Average Current Mode Control for Bridged buck converter

IV. SIMULATION

A. Parameters of simulation

Input dc voltage Vin : 90-260V,Output dc voltage Vo : 160 V, Output power : 700 W, Switching frequency : 60 kHz, Switches :MOSFET, Load: 36 Ω

Capacitors :C1=C2=6000µF, Inductors:L1=L2=60µH

B. Control circuit simulation diagram

Simulation diagram for Average current mode control used here is as shown in Figure 12.Output voltage of the load and the reference value are compared and given to a PI controller. The error generated is then multiplied with a unity reference of input voltage to create current reference.

Inductor current sensed is given to a switch which will pass I_{L1} through it if Vin is greater than zero otherwise I_{L2}. During each half cycle corresponding inductor currents sensed is averaged and compared with current reference value to generate control voltage for the PWM modulator.

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Output is given to a relational operator and output of relational operator is given as a gate pulse to the main switch. During positive half cycle of input voltage switch S1 must be on and during negative half cycle S2 must be controlled. For that the output of PWM modulator is given to switches 1 and 2.If Vin is greater than zero then gate signal will pass through the switch1.Other wise it passes the other input. Switch 2 will select the input if Vin is less than zero i.e. negative.

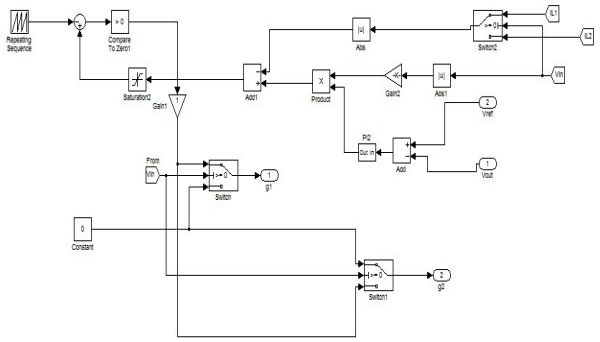

Figure 12: Simulation Diagram for ACMC

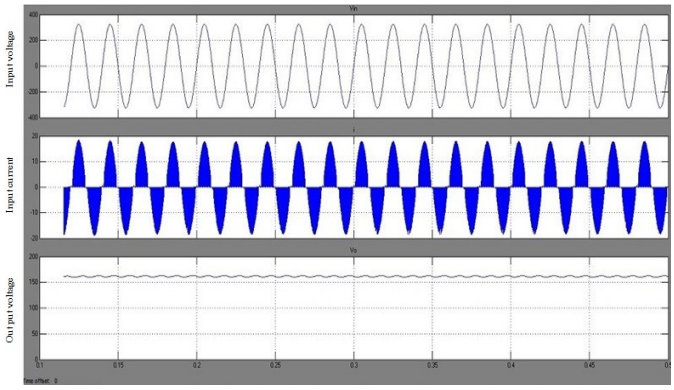

Figure 13: Input voltage ,Input current and output voltage

Output of 160V is obtained from simulation for 90-260V input voltage variations. The ripple voltage is within 2 %.Pf is about 0.98.THD is within acceptable range 0.32.efficiency variation is within 1% for lower and higher level input voltages.

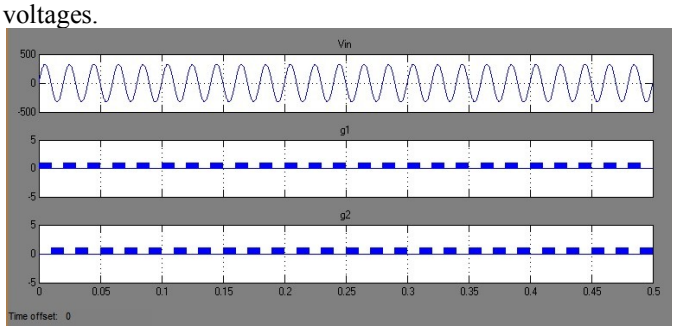

Figure 14: Input voltage, Gate pulses for S1 and S2

Gate pulses are obtained for alternate half cycles. As the input voltage changes. The duty ratio gets adjusted to charge the capacitors and maintain constant voltage.

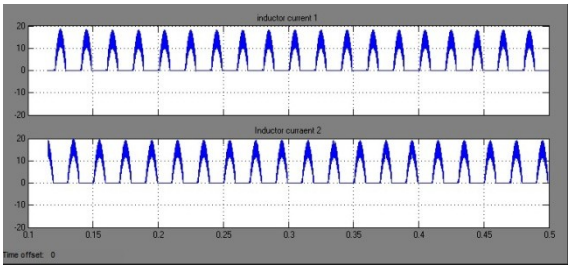

Figure 13 : Inductor current waveforms I_{L1},I_{L2}

V. Hardware Implementation

Hardware implementation of 25W prototype is made .Output voltage is selected as 120V for the design, switching frequency is 15kHz.

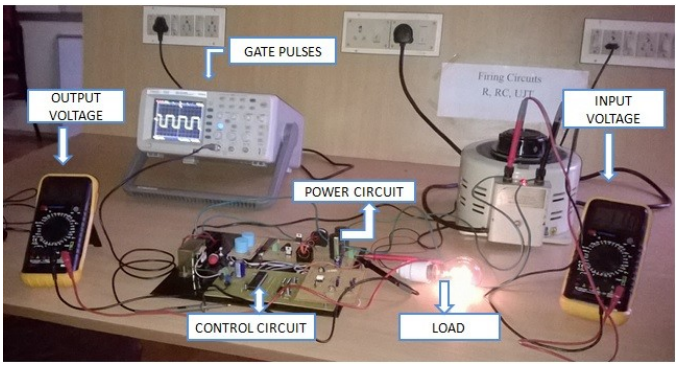

Figure 14 :Experimental setup

The circuit uses an PIC18F4550 for gate pulse generation .MOSFET IRF840 is used as switches and 6A4 diodes, The voltage level of pwm signals from PIC is not sufficient to drive the gate circuit of MOSFET. By using driver IC FAN7392 5V signals are raised to 10V level and fed to gate using pulse transformer.

Average current mode control is used here so feedback circuit has to sense the inductor currents , output voltage and rectified input voltage. Inductor currents are sensed by means of current transformers. Output voltage sensing is done by using a potential divider circuit. For providing isolation between power circuit and control circuit TLP250 is used. Input voltage is stepped down by means of a 230V/12V transformer and rectified .By using a potential divider the rectified input voltage is limited to a range suitable for the control circuit fed to microcontroller for providing input voltage reference.

The output voltage obtained is constant over 100-240 V input voltage ranges. power factor is about 0.97 and THD is less than 0.33.

VI. Conclusion

Design, simulation and hardware implementation of bridgeless buck converter rated 25W,120V output for wide input voltage variation(90-240) is done. It was observed from the simulation that the efficiency variations are very small for high and low voltage ranges .Power factor and THD are wthin acceptable range.

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Vidhya KG Received B.Tech from Govt .Rajiv Gandhi Instituite of Technology,Kottayam,Kerala in 2008.Worked at MG UCE,Kerala from 2009-2012.Done M Tech in Power Electronics in Vidya Academy of Science &Technology 2012-2014,Thrissur ,Kerala.

Neethu K. Paul Received B.Tech Degree in Electrical and Electronics from MET's School of Engineering, Thrissur,Kerala in 2012.M.Tech Student of Power electronics, Vidya Academy of science and Technology, Thrissur,, Kerala 2012-2014 batch.

BinithaT.M Assistant Professor Vidya Academy of Science &Technology,Thrissur Kerala .Received B.Tech Degree from Vidya academy of Science and Technology 2007.Completed M Tech from Anna University in 2013.

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