Architecture and Implementation of OFDM Transmitter and Receiver

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Abstract: **Orthogonal Frequency Division Multiplexing (OFDM) is a multi carrier modulation technique. It provides high bandwidth efficiency because the carriers are orthogonal to each other and multiple carriers share the data among themselves. It has been adopted by most wireless and wired communication standards. The idea is to utilize a number of carriers, spread regularly over a frequency band, in such a way so that the available bandwidth is utilized to maximal efficiency. The main advantage of this transmission technique is its robustness to channel fading in wireless communication environment. The main objective of this project is to design and implement a baseband OFDM transmitter and receiver. The implementation has been carried out in hardware using Field Programmable Gate Array (FPGA). Both the transmitter and the receiver are implemented on a single FPGA board with the channel being a wired one. The designing has been done in Verilog HDL. Modelsim 6.4b has been used to simulate the design.**

***Keywords*- OFDM, FPGA.**

I. INTRODUCTION

The OFDM is the modulation scheme having multi carrier transmission techniques here the available spectrum is divided into many carriers each one being modulated at a low rate data stream. The spacing between the carriers is closer and the carriers are orthogonal to one another preventing interferences between the closely spaced carriers hence OFDM can be thought of as a combination of modulation and multiplexing techniques, each carrier in a OFDM signal has very narrow bandwidth so the resulting symbol rate is low which means that the signal has high tolerance to multi path delay spread reducing the possibility of inter symbol interference (ISI)which is the requirement for today's communication systems.

OFDM is similar to FDM but much more spectrally efficient by spacing the sub-channels much closer together (until they are actually overlapping). This is done by finding frequencies that are orthogonal, which means that they are perpendicular in a mathematical sense, allowing the spectrum of each sub-channel to overlap another without interfering with it. In Figure 1.1 the effect of this is seen, as the required bandwidth is greatly reduced by removing guard bands (which are present in FDM) and allowing signals to overlap.

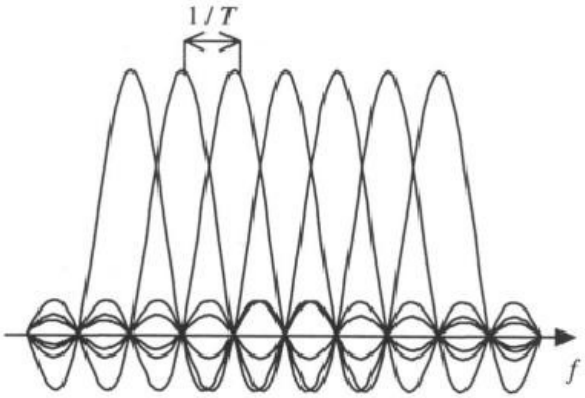

Figure 1.1 Spectrum overlap in OFDM

A. Orthogonality

The key to OFDM is maintaining orthogonality of the carriers. If the integral of the product of two signals is zero over a time period, then these two signals are said to be orthogonal to each other. Two sinusoids with frequencies that are integer multiples of a common frequency can satisfy this criterion. Therefore, orthogonality is defined by:

$$\int_0^T \cos(2\pi nft)\cos(2\pi mft)\,dt = 0 \qquad (n \neq m)$$

where n and m are two unequal integers; f is the fundamental frequency; T is the period over which the integration is taken. For OFDM, T is one symbol period and f set to 1/T for optimal effectiveness.

B. Field Programmable Gate Array

By modern standards, a logic circuit with 20000 gates is common. In order to implement large circuits, it is convenient to use a type of chip that has a large logic capacity. A field programmable gate arrays (FPGA) is a programmable logic device that support implementation of relatively large

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logic circuits [6]. FPGA is different from other logic technologies like CPLD and SPLD because FPGA does not contain AND or OR planes. Instead, FPGA consists of logic blocks for implementing required functions. An FPGA contains 3 main types of resources: logic blocks, I/O blocks for connecting to the pins of the package and interconnection wires and switches.

The logic blocks are arranged in a two-dimensional array, and the interconnection wires are organized as horizontal and vertical routing channels between rows and columns of logic blocks [7]. The routing channels contain wires and programmable switches that allow the logic blocks to be interconnected in many ways.

FPGA can be used to implement logic circuits of more than a few hundred thousand equivalent gates in size [7]. Equivalent gates is a way to quantify a circuit's size by assuming that the circuit is to be built using only simple logic gate and then estimating how many of these gates are needed. Figure 1.2 a clear picture of the FPGA design flow.

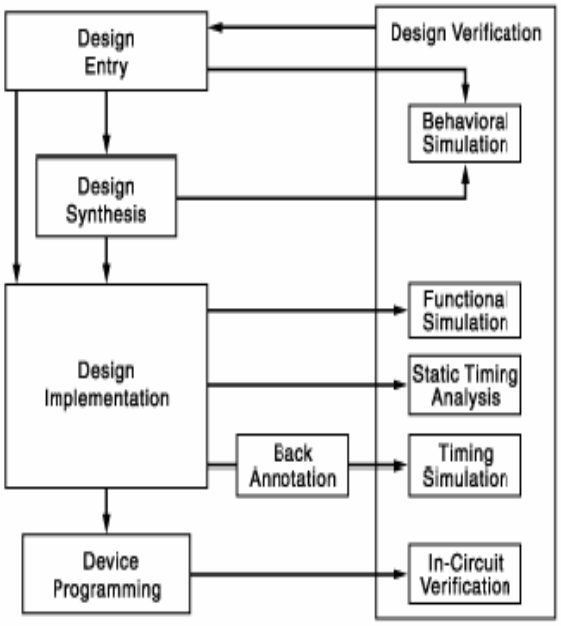

Figure 1.2FPGA design flow

II. OFDM TRANSMITTER & RECEIVER

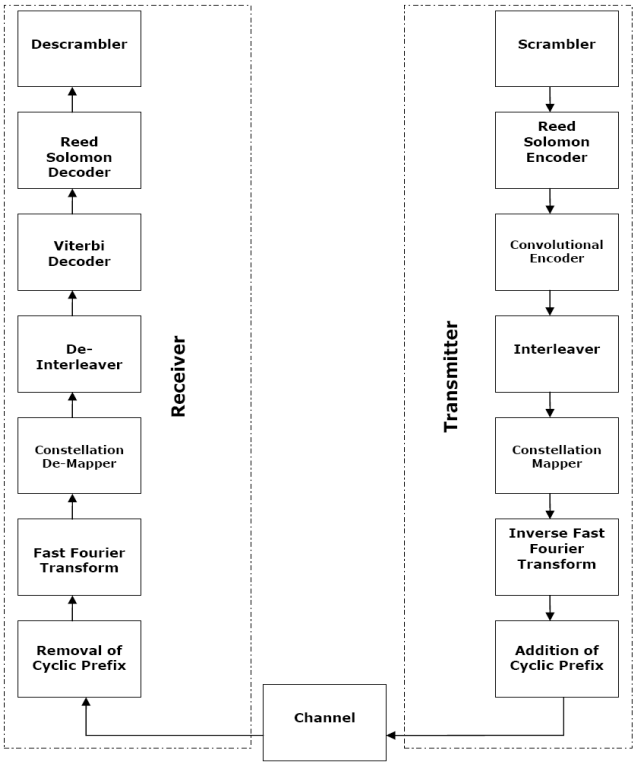

Fig 2.1 block diagram of OFDM transmitter and receiver

A. Scramble/Descramble

Data bits are given to the transmitter as inputs. These bits pass through a scrambler that randomizes the bit sequence. This is done in order to make the input sequence more disperse so that the dependence of input signal's power spectrum on the actual transmitted data can be eliminated. At the receiver end descrambling is the last step. Descrambler simply recovers original data bits from the scrambled bits.

B. Reed-Solomon Encoder/Decoder

The scrambled bits are then fed to the Reed Solomon Encoder which is a part of Forward Error Correction (FEC). Reed Solomon coding is an error-correction coding technique. Input data is over-sampled and parity symbols are calculated which are then appended with original data[3]. In this way redundant bits are added to the actual message which provides immunity against severe channel conditions. A Reed Solomon code is represented in the form RS (n, k), where

$n=2^m - 1$ 1
$k=2^m - 1-2t$ 2

Here m is the number of bits per symbol, k is the number of input data symbols (to be encoded), n is the total number of

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symbols (data + parity) in the RS codeword and t is the maximum number of data symbols that can be corrected. At the receiver Reed Solomon coded symbols are decoded by removing parity symbols.

C. Convolutional Encoder/Decoder

Reed Solomon error-coded bits are further coded by Convolutional encoder. This coder adds redundant bits as well. In this type of coding technique each m bit symbol is transformed into an n bit symbol; m/n is known as the code rate. This transformation of m bit symbol into n bit symbol depends upon the last k data symbols, therefore k is known as the constraint length of the Convolutional code. Viterbi algorithm is used to decode convolutionaly encoded bits at the receiver side. Viterbi decoding algorithm is most suitable for Convolutional codes with k≤10.

D. Interleaver/De-Interleaver

Interleaving is done to protect the data from burst errors during transmission. Conceptually, the in-coming bit stream is re-arranged so that adjacent bits are no more adjacent to each other. The data is broken into blocks and the bits within a block are rearranged. Talking in terms of OFDM, the bits within an OFDM symbol are rearranged in such a fashion so that adjacent bits are placed on non-adjacent subcarriers. As far as De-Interleaving is concerned, it again rearranges the bits into original form during reception.

E. Constellation Mapper/De-Mapper

The Constellation Mapper basically maps the incoming (interleaved) bits onto different sub-carriers. Different modulation techniques can be employed (such as QPSK,BPSK, QAM etc.) for different sub-carriers. The De-Mapper simply extracts bits from the modulated symbols at the receiver.

F. Inverse Fast Fourier Transform/ Fast Fourier Transform

This is the most important block in the OFDM communication system. It is IFFT that basically gives OFDM its orthogonality. The IFFT transform a spectrum(amplitude and phase of each component) into a time domain signal. It converts a number of complex data points into the same number of points in time domain. Similarly, FFT at the receiver side performs the reverse task i.e.conversion from time domain back to frequency domain.

G. Addition/Removal of Cyclic Prefix

In order to preserve the sub-carrier orthogonality and the independence of subsequent OFDM symbols, a cyclic guard interval is introduced. The guard period is specified in terms of the fraction of the number of samples that make up an OFDM symbol. The cyclic prefix contains a copy of the end of the forthcoming symbol. Addition of cyclic prefix results in circular convolution between the transmitted signal and the channel impulse response.

Frequency domain equivalent of circular convolution is simply the multiplication of transmitted signal's frequency response and channel frequency response, therefore received signal is only a scaled version of transmitted signal (in frequency domain),hence distortions due to severe channel conditions are eliminated**.** Removal of cyclic prefix is then done at the receiver end and the cyclic prefix–free signal is passed through the various blocks of the receiver.

III. SPECIFICATION OF TRANSMITTER & RECEIVER

Figure 2.1 shows a top-level block diagram of the OFDM transmitter and receiver. Single-Clock operation speaks itself for the synchronous operation of the system. The Reset input must be asserted for at least one clock cycle for the system to reset. Output of the transmitter is fed to the host PC via the serial port and also to the OFDM receiver.

Specifications are listed below:

· OFDM with 64 sub-carriers (all data sub-carriers)
· All the sub-carriers are modulated using QPSK
· IFFT: 64-point. Implemented using FFT radix 22 algorithm
· Channel coding: Reed Solomon code + Convolution code
· Reed Solomon Encoder: RS (15, 9)
· Convolution Encoder: m=1, n=2, k=7. Code rate = ½
· Block Interleaver and 1/8 Cyclic Prefix

IV. RESULTS

Transmitter:

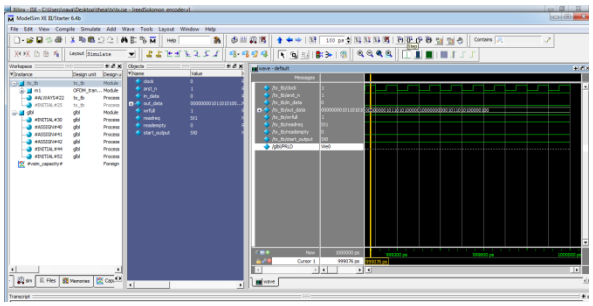

Fig:4.1.a. simulation result of transmitter

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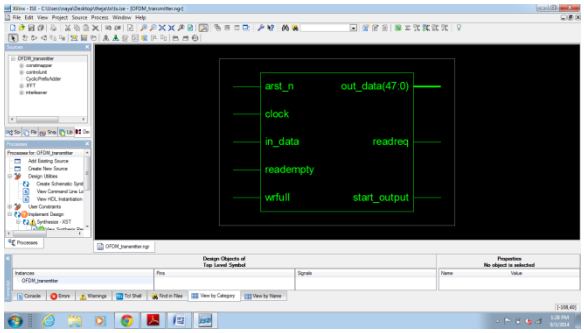

Fig:4.1.b. RTL schematic of transmitter

Receiver:

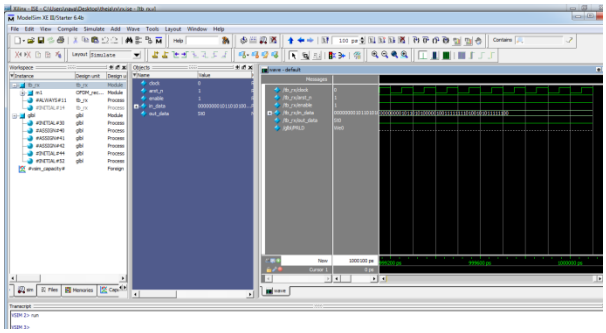

Fig:4.1.c. simulation result of receiver

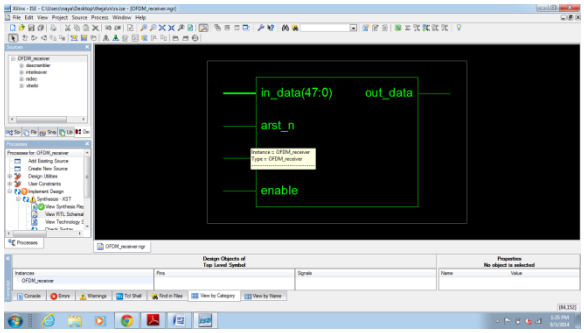

Fig:4.1.d. RTL schematic of receiver

IV. CONCLUSION

Orthogonal Frequency Division Multiplexing (OFDM) transmitter and receiver have been design using Quartus II t0ool and Simulation have been carried out using Altera Modelsim simulation tool. By using channel coding & decoding methods and error detection & correction methods synthesis and analysis has been done and how exactly OFDM system works, is verified. Verilog is used as Hardware Description Language (HDL) to program all the components of the OFDM Transmitter and Receiver and verification of functionality of all components has done by giving different input and output is verified.

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