Dynamic CMOS Design With Enhanced Noise susceptible power

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Abstract:
Dynamic CMOS circuits are especially used for high-performance very large-scale integrated (VLSI) systems , basically like circuits designed using microprocessor. But there are certain limitations which hinders the performance of dynamic CMOS namely noise tolerance, charge leakage, power consumption etc. With the escalating impact of process variations on design performance, aggressive technology scaling, noise in dynamic CMOS circuit has become an imperative design challenge. The noise induce in circuits will affect the performance of dynamic circuits, which has to be first improved for reliable operation of VLSI systems.

Introduction:
The purpose of this paper is to review fundamental noise sources of interest to circuit designers, bringing in some results from statistical physics that may be less familiar to design engineers. In addition to the low cost and high levels of integration for digital circuit design offered by advanced CMOS processes, MOSFETs have become very attractive for radio-frequency (RF) integrated circuit (IC) applications because of their very high unity-gain frequencies of tens of GHz resulting from their down scaling to deep sub-micron dimensions. However, when

working at high frequencies, the noise generated within the device itself will play an increasingly important role in the overall system sensitivity characteristics, dynamic range and signal-to-noise ratio, especially for a frontend receiver. Therefore, a physics-based noise model which can accurately predict the noise characteristics of deep submicron MOSFET's is crucial for the low noise, RF IC design. Before developing a new noise model, how to design a device-under-test (DUT) and how to obtain the intrinsic noise information from the using dynamic logic . As the device gate length (L) is less than 100nm, further reduction in L has yielded limited improvements in performance due to velocity saturation and source velocity limit. For this reason, the strained silicon technology has been put into production. The scaling of gate dielectric also poses a challenge. As the physical thickness of the SiO2 gate dielectric (T_{ox}) is scaled beyond 1.2nm, quantum mechanical tunnelling current from the gate into the channel becomes significant. Further reduction in T_{ox} will result in large static leakage current and large power consumption even when the

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device is turned off. Therefore at around the 45nm node, a high-K gate dielectric is often used to scale down the effective oxide thickness (*EOT*) without increasing the gate tunnelling current. Metal gate electrodes are also used to eliminate the unwanted poly-silicon gate depletion effect.

Figure 1 shows a conceptual view of an n-channel MOSFET, operating in saturation. A cross-sectional view of the channel is shown, with inversion layer between the source and drain formed by the gate voltage v_G. Also shown is a conceptual plot of the electron potential energy along the source-drain channel.

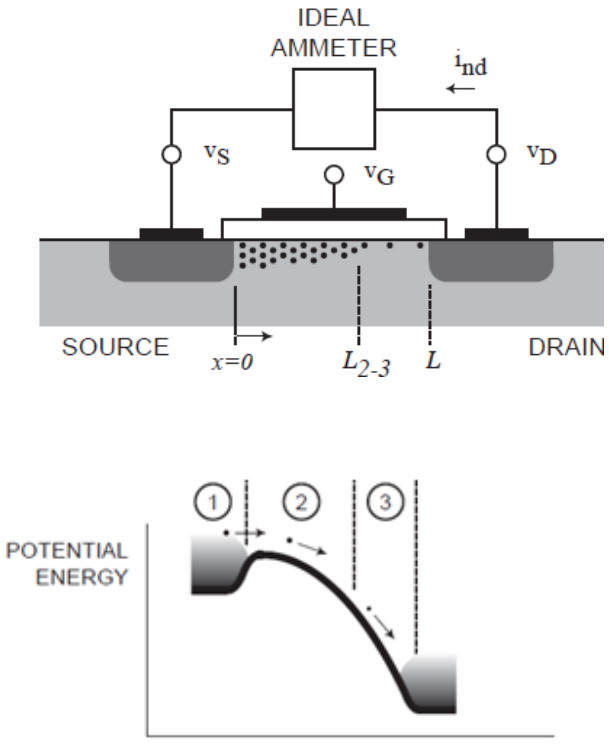

Fig.1- Carrier flow, potential energy for general MOSFET

We consider only effects relevant to wideband drain current noise, not 1/f noise or induced gate noise. Although we will consider velocity saturation, we will neglect the carrier multiplication role of "hot" electrons since the effect on wideband noise is not significant. As described in there are three types of carrier motion as an electron moves from source to drain:

1) Injection over potential barrier into channel: For a carrier to enter the source-drain channel, it must have enough energy to overcome the potential barrier (shown in Fig..1 at x = 0) at the source-channel p-n junction. The height of the barrier depends on several factors including the potential profile in the channel as well as other dimensional effects not represented in the simple picture of Fig. 1.

2) Low field motion according to drift: At the source end of the channel ($0 < x < L_{2-3}$), the x-direction component of the electric field is below the critical value at which velocity saturation occurs. The carrier undergoes scattering collisions and exchanges energy with the lattice, is in thermal equilibrium with its environment, and its average velocity is adequately described by the mobility relationship. In this region, the thermal noise relationships of section III apply.

3) High field motion with velocity saturation: At the drain end of the channel ($L_{2-3} < x < L$) the x-direction component of the electric field exceeds its critical value and velocity saturation occurs.

As described in, carrier motion in the velocity saturated region (3) will not contribute appreciably to noise: since the velocity is limited to v_{sat}, the carriers do not respond to any external influence and the statistics of carrier arrival at the drain

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are determined by behaviour in regions (1) and (2).

Flicker Noise

Flicker noise dominates the noise spectrum at low frequency. Flicker noise was first observed in vacuum tubes over seventy-fifty years ago. It gets its name from the anomalous flicker" that was seen in the plate current. Flicker noise is also commonly called 1\f noise, because the noise spectrum varies as 1\f where the exponent Θ is very close to unity

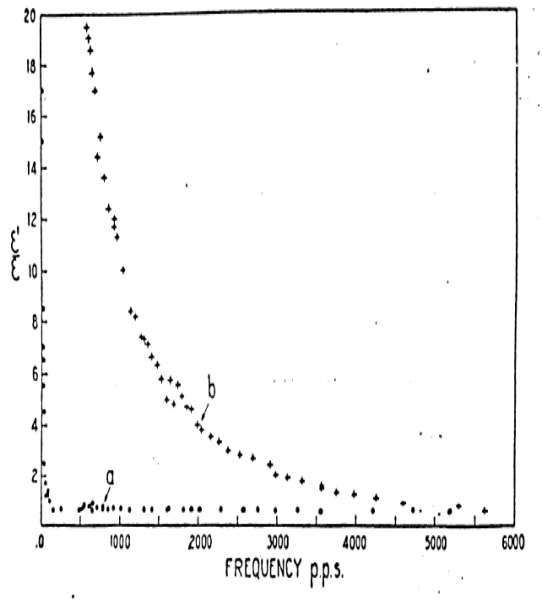

Figure 2: Plot of noise amplitude versus frequency (on linear scales) as measured in two dissimilar

(Θ = 1 +0.2) vacuum tubes by Johnson in 1925. The vertical axis has been normalized by the expected shot noise amplitude. Fluctuations with a 1\f power law have been observed in practically all electronic materials and devices, including homogenous semiconductors, junction devices, metal ¯lms, liquid metals, electrolytic solutions, and even superconducting Josephson junctions. In addition it has been observed in mechanical, biological, geological, and even musical systems. No entirely satisfactory physical explanation has been developed, and in fact, available evidence seems to suggest that the origins of flicker noise in different devices may be quite different. Two competing models have appeared in the literature to explain flicker noise: the McWhorter number fluctuation theory and the Hooge mobility fluctuation theory. There is experimental evidence to support both theories, and thus the literature is mostly split into two camps over the issue.

Thermal Noise

Thermal noise is the voltage fluctuations caused by the random motion of electrons in a resistive medium. It is broadband white noise, and it gets worse with increasing resistance and temperature. The spectral density of the thermal noise across a resistor with resistance R is given by

$$V_t^2=4kTR$$

The device filled with many electrons, with an average carrier concentration of n mobile electrons per unit volume, the carriers undergo scattering collisions, exchanging energy and momentum with the medium. It undergoes collisions and is randomly scattered. The random motion of electrons in a conductor introduces fluctuation in the voltage measure across the conductor even if the average current is zero.

IMPLEMENTATION OF KEEPERS

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It is found that , If we implement keepers in our CMOS circuits the performance of circuit is enhanced. To increase the noise tolerance of dynamic CMOS logic gates is to employ a weak transistor, known as keeper, at the dynamic node as shown in Fig.3

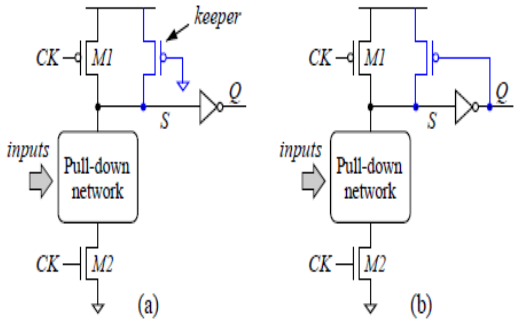

Figure 3 Improving noise immunity of Dynamic CMOS by using keepers (a)Weak always on keeper (b)Feedback keeper

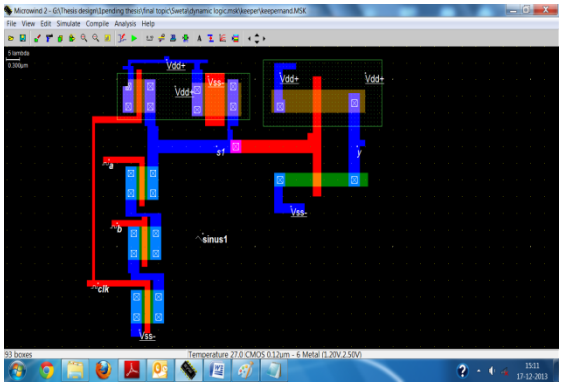

Figure 4 Layout of fig 3(a) Weak always on keeper

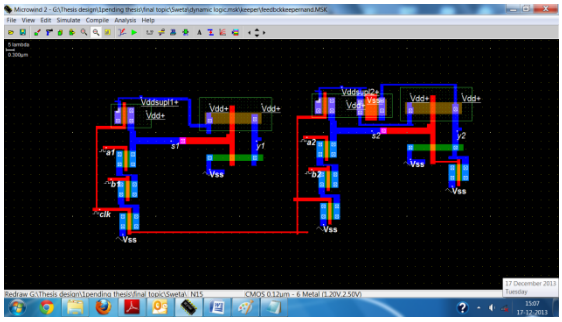

Figure 5 Layout of fig 3(b) Feedback keeper

The keeper transistor supplies a small amount of current from the power-supply network to the dynamic node of a gate so that the charge stored in the dynamic node is maintained. In the original domino dynamic logic work, the gate of the PMOS keeper is tied to the ground, Therefore, the keeper is always on. Later, feedback keepers, illustrated in Fig.3 (b),

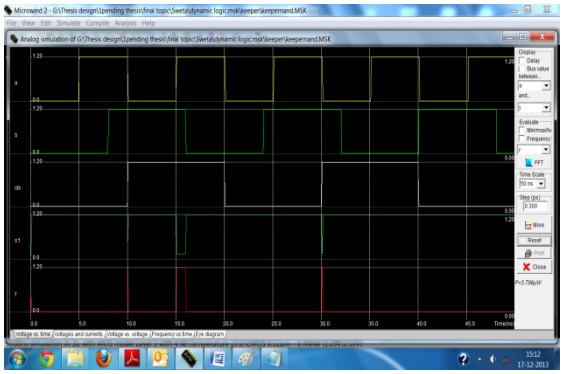

Fig 6 simulation of fig 4 weak always on keeper

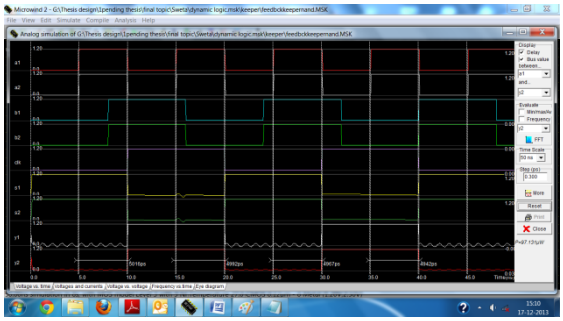

Fig 7 simulation of fig 5 Feedback keeper

became more widely used because they eliminate the potential DC power consumption problem using the always-on keeper in the evaluation phase of domino gates. In figure 6 and 7 ,simulation of weak always on keeper and Feedback keeper is shown , and which clearly express the reduction of noise in circuit.

CONCLUSION

In this paper the problems of process variations, timing, noise tolerance, and power are investigated together for

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performance optimization. We propose a process variation-aware load-balance of multiple paths transistor sizing algorithm to: 1) improve worst-case delay, delay uncertainty, and sensitivity due to process variations in dynamic CMOS circuits, and 2) optimize dynamic CMOS circuits with MOSFET-based keepers to improve the noise tolerance. compared to their initial performances.

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