Design of an ALU with a low power LFSR using Clock gating

Anuja Aravind, Raseena K.A

Abstract— **This paper proposes a method to reduce the power consumption of the popular linear feedback shift register. The proposed scheme is based on data driven clock gating approach and it can offer significant power reduction based on the technological characteristics of the employed gates compared to the traditional gated design approach. Reduction of dynamic power is done by effective management of the utilization of clock signal for the FFs present in the LFSR circuit. The gating of clock signals can be coordinated with grouping of flip flops present in the 32 bit LFSR circuit, hence reducing the utilization of the master clock signal all the time. The total power consumption is reduced by means of reducing the dynamic power consumption.The LFSR designed so can be used in the design of an arithmetic and logic unit (ALU) and hence reduce the power consumption of the overall system.**

Index Terms— **DDCG, gated clock, group size, sequential circuit, toggling.**

I. INTRODUCTION

About 30% to 70% of the total dynamic power consumption in consumer electronics is the system's clock signal. Many techniques to reduce the usage of clock signal have been devised as in [1]. [2] uses multiple supply voltages to reduce to clock tree power.[3] is based on the idea of adopting a reduced-swing clock signaling scheme. Grouping of FFs present in the sequential circuit is an effective method of reducing clock power. FF grouping in [4] is mainly driven by the physical position proximity of individual FFs.

The principle of data driven clock gating as explained in [5] can be efficiently implemented in linear structured circuits such as Linear feedback shift registers. In this paper a 32 bit LFSR is presented in which flip flops are organized into different groups based on the toggling probability and different clocks are given to each group. So we need not have to supply master clock all the time.

II. DATA DRIVEN CLOCK GATING

When a logic unit is clocked, the sequential elements contained in the logic unit receive the clock signal, regardless of whether or not they will toggle in the next cycle. In clock gating technique, the clock signals are ANDed with explicitly predefined enabling signals. Clock gating can be employed at all levels including system architecture, block design, logic design, and gates.

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Fig. 1 shows how a FF can find out that whether its clock can be disabled or not in the next cycle. The XOR gate as shown in Fig.1(a) compares the FF's current output with the present data input that will appear at the output in the next cycle. The XOR gate's clk_en output shows whether a clock signal will be required in the next cycle. The clock driver in Fig. 1(a) is then replaced by a 2-way AND gate called *clock gater* in Fig.1(b).

Additional power reduction for a sequential circuit can be achieved by lowering the number of clock gaters [6]. It is possible to drive several FFs with a common gater if we knew that they are toggling simultaneously most of the time, thus achieving almost the same power reduction, but with fewer gaters. Fig. 2 shows how to join k clk_en signals generated by distinct FFs into one gating signal where k indicates the number of FFs combined to form the group.

The grouping saves the individual clock gaters at the expense of an OR gate and a negative edge triggered latch that is required to avoid glitches of the enable signal. The combination of a latch and an AND gate is commonly used by commercial tools and is called integrated clock gate (ICG).The hardware savings increases with k, but the number of disabled clock pulses is decreasing. Hence, for the scheme proposed in Fig. 2 to be beneficial, the clock enabling signals of the grouped FFs must be highly correlated.

The data-driven gating proposed in [5]is illustrated in Fig. 3. A FF finds out that its clock can be disabled in the next cycle by XORing its output with the present data input that will appear at its output in the next clock cycle. The outputs of *k* XOR gates are ORed inorder to generate a joint gating signal for *k* FFs, and is then connected to the integrated clock gate (ICG) unit.

In the physical implementation of the data driven clock gating circuit, the XOR gate is integrated into the FF, while the OR gate, AND gates and the latch are integrated into the clock gater. Two distinct clock signals are there:clk_g is the ordinary gated signal driving the registers, while clk is driving the latches of the clock gaters.

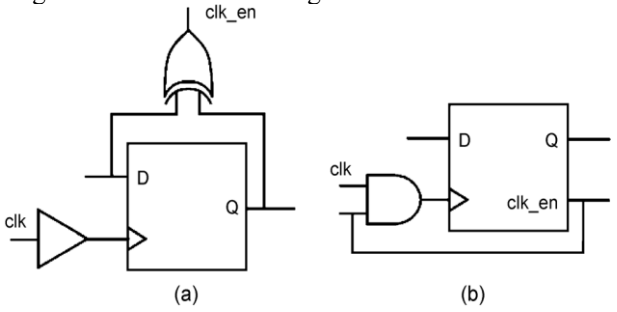

Fig 1:Enabling of clock signal into one gating signal

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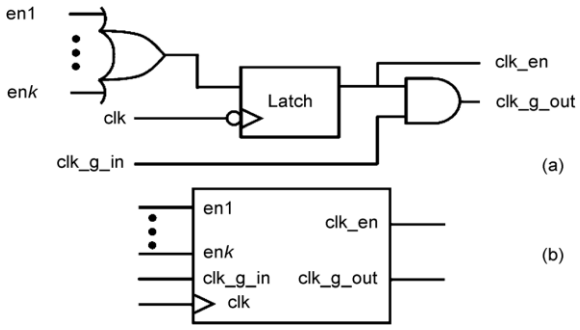

Fig.2 Joining of k enabling signals

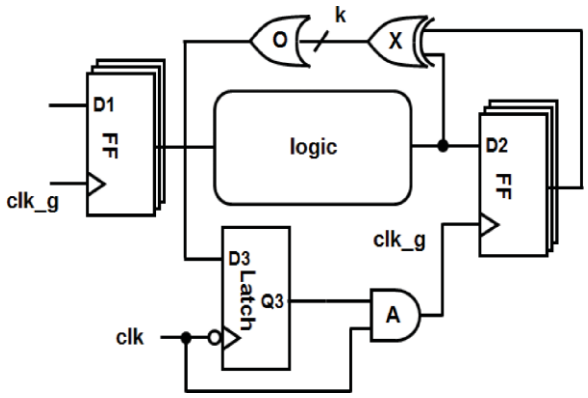

Fig. 3. Practical data-driven clock gating. The latch and gater (AND gate) overheads are amortized over k ffs.

A. *Linear Feedback shift register*

A Linear Feedback Shift Register is a sequential shift register with combinational logic that causes it to pseudo-randomly cycle through a sequence of binary values. Linear feedback shift registers have various uses in digital systems design. It is a shift register whose input bit is a linear function of its previous state and is obtained with an array of FFs with a linear feedback performed by several XOR gates [7]. They can be efficiently described through an nth-order polynomial;

$$P_n(x)=x^n+b_{n-1}x^{n-1}+\ldots\ldots+b_1x+1$$

where the binary coefficients bi define the well-known polynomial characteristic which the generator main properties depends on.

Fig.4 shows a traditional LFSR circuit into which the Data driven clock gating approach is going to be implemented. As it is well known, LFSRs exhibit a high-speed bit generation and they also have very good statistical properties. However, the main drawback for these generators is the high power consumption given as,

$$P_{TR}=nP_{FF}+t.P_{XOR}$$

where n is the register's length (i.e., the order of the generator), t is the number of the inner taps (i.e., the number of the terms of the polynomial characteristic except x^n and 1). The terms PFF and PXOR are the dynamic power consumption of DFF and XOR gates respectively. Both the terms P_{FF} and P_{XOR} are proportional to Vdd^2fck, where Vdd is the supply voltage and fck the clock frequency.

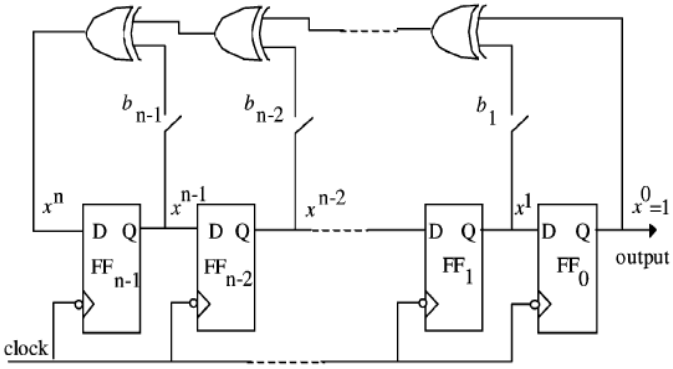

Fig. 4. Simplified circuit of a generic n-bit LFSR.

The clock path toggles at every clock cycle, hence dissipating a significant amount of power especially at high clock rate. Vice versa, power consumption of the D-path and the XOR gates depends upon the switching activity at the inner node.

B. *LFSR with Data Driven Clock Gating*

Fig.6 shows a 32 bit LFSR using Data driven clock gating technique.The LFSR uses a gated clock for each of the 8 groups so that the each clock may drive four FFs simultaneously.

III. DESIGN AND SIMULATION OF 32 BIT LFSR

The proposed design of 32-bit LFSR using Data driven clock gating has been validated through simulations run in Xilinx 14.1. Here we implemented 32 bit LFSR using Xilinx ISE. Xilinx provides automation tools for designing and implementing any logical as well as hardware on a single chip to get faster prototype, so it is widely used to implement any digital logic on FPGA. In this design, we describe the RTL-level of the LFSR using VHDL language.

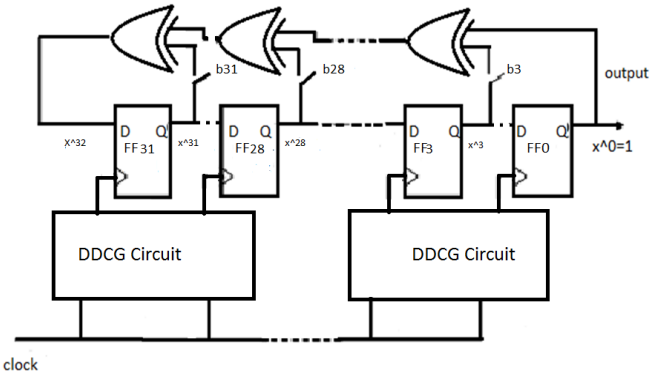

Fig.6. LFSR circuit with data driven clock gating

The detailed circuitry is shown in the Fig.7. Clk 1 feeds flipflops 1-4,Clk2 feeds flip flops 5-8 and so on.

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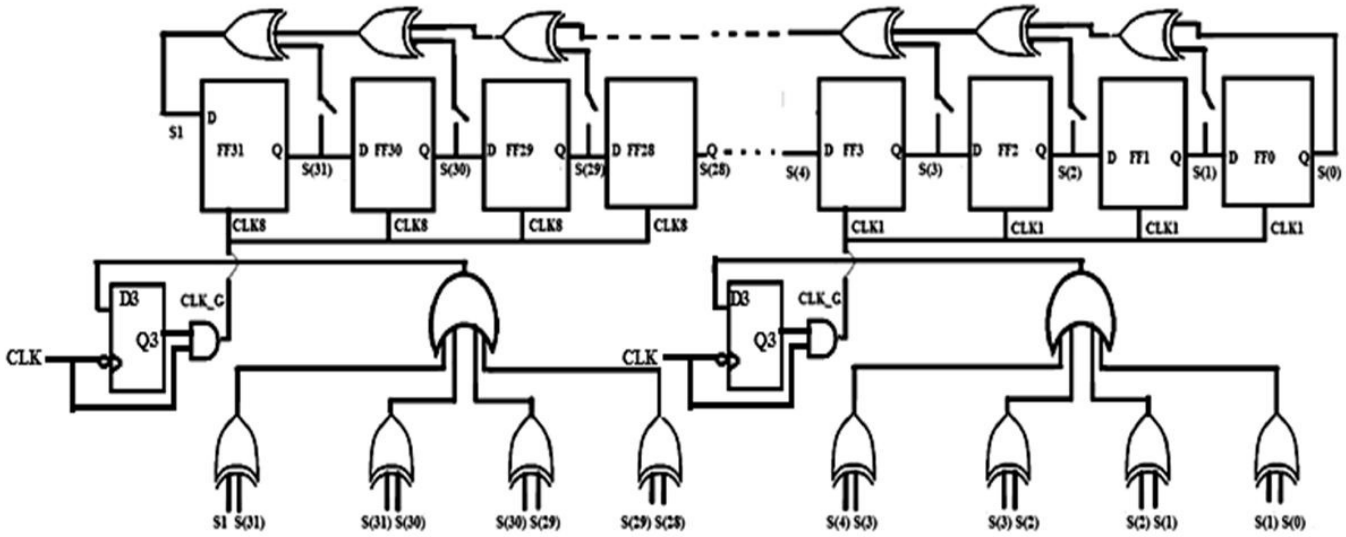

Fig.7. Detailed circuitry of the 32bit LFSR

A. *Simulation waveforms of LFSR*

The simulation waveforms show the reduced clock utilization of the master clock signal.Clock 1 to clock 8 are gated at certain point of time depending on the value on the enabling signal, thereby reducing the clock domain power consumption.

Fig.5 shows the simulation waveforms.

A. *Power Consumption*

Power consumption is estimated by means of XPower Analyzer in Xilinx. An ordinary 32 bit LFSR has a dynamic power consumption of 21 mW and total power consumption of 64 mW. The approach proposed in this paper is found to be more power efficient compared to the former one.The dynamic power consumed is found to be 12mW and hence yield a total power of 54mW.Thus about 16% power savings is obtained. However the quiescent power consumption is same for both cases (since its value is independent of switching activity).It is obtained as 42mW.

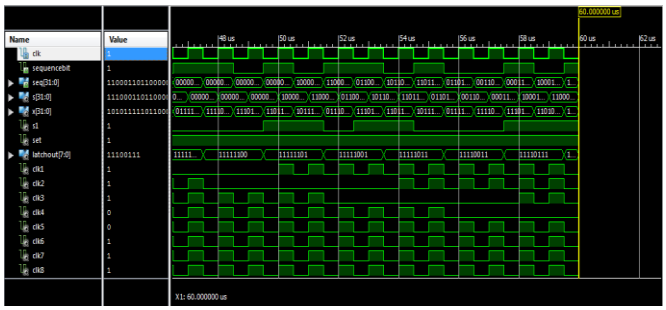

Fig.5.Simulation waveforms

Table I shows the power reports generated by XPower Analyzer tool.

Table1: Comparison of Power reports

Power consumption (mW)	LFSR without Clock gating	LFSR with DDCG (k=16)	LFSR with DDCG (k=8)	LFSR with DDCG (k=4)
Dynamic powerconsumption	21	16	14	12
Quiescent power consumption	42	42	42	42
Total power consumption	64	58	57	54

IV. DESIGN AND SIMULATION OF 32 BIT ALU

This section describes the design of a 32-bit Arithmetic Logic Unit (ALU). An ALU is the brawn of the computer, the device that performs the arithmetic operations like addition and subtraction or logical operations like AND and OR. This section illustrates an ALU which carryout such operations using the inputs applied to each of the 1-bit ALUs used to construct the 32 bit ALU. Because the input word is 32 bits wide, we need a 32-bit-wide ALU. Hence we will connect 32 1-bit ALUs to create the desired ALU and explains how the combinational logic works. Table III shows the various operations done by the ALU designed.Further power reduction can be achieved by means of introducing power saving modes into the ALU. The ALU will enter into sleep mode when both the inputs remain unchanged during the next clockcycle after executing the desired operation in the current cycle. Otherwise it may enter active mode if either of the inputs got changed.

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Table II: ALU Operations

Select line inputs				Operation
S0	S1	S2	S3	
0	0	0	0	a+b
0	0	0	1	a+b+1
0	0	1	0	transfer a
0	0	1	1	transfer b
0	1	0	0	inc a
0	1	0	1	dec a
0	1	1	0	a-b
0	1	1	1	a and b
1	0	0	0	a or b
1	0	0	1	a xor b
1	0	1	1	shift right
1	1	0	0	shift left
1	1	0	1	a-b with borrow

A. Simulation waveforms of 32 Bit ALU

One out of two operands given as inputs to each of the ALU is supplied by the proposed 32 bit LFSR. At each clock cycle, the words at each input is compared and the operations are performed. The state of the ALU can be driven as either 'Sleep' or 'Active' depending on the change in the outputs in the next clock cycle. If the input (other than the 32 bit word generated by LFSR) applied to the ALU remains the same during the next clock cycle then the ALU retains the result since it is not subjected to any change. Hence the state of the ALU will be 'Sleep'.The operation to be performed is determined by the word on the select line. If we choose another operation for the next clock cycle the ALU may enter the 'Active' state since the select inputs has changed. Fig. 6 shows the waveforms of the ALU obtained during simulation.

B.Power Consumption

The dynamic power consumption of the 32 bit ALU has been reduced by 12 mW and the total power reduction is 51 mW. The quiescent power consumption is estimated to be remain the same as that for an ALU without using an LFSR.

Table III compares the power consumed by the ALUs under concern.

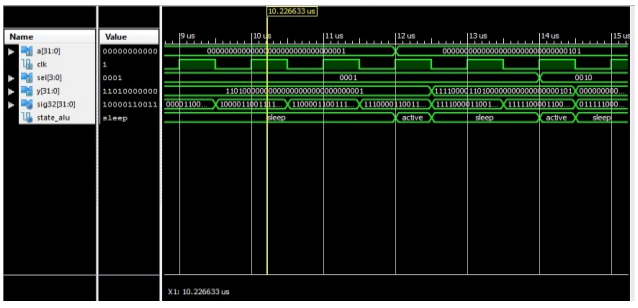

Fig.6.Simulation waveforms of ALU

Table III: Comparison of Power of various ALUs

Type	Dynamic power(mW)	Total power(mW)
ALU with ordinary LFSR	17	59
ALU with DDCG LFSR	15	57
ALU with Power saving modes applied	12	54

CONCLUSION

This paper studied the grouping of FFs for joint clocking by a common gater to yield maximal dynamic power savings in a 32 bit LFSR circuit. The combinational power increases with Data Driven Clock Gating as a result of the extra logical component, the gaters. But the sequential power and the clock power decreases more significantly because of the clock disabling techniques. The proposed LFSR is used as an input register for a 32 bit ALU, providing 32 bit word as one of its operands. The proposed LFSR and ALU is found to be power efficient than an ordinary LFSR or an ALU which is driven by the output of an LFSR circuitry at its input. The LFSR can be applied to reduce the power consumption of other circuits such as pseudo random number generators as well. Since the Lfsr output changes at every clock cycle, the application of power saving modes in which the ALU is driven to sleep when the inputs are unchanged is not much efficient. The applicability of the data driven clock gating approach can be hence extended to other linear circuits such as counters. This may help to find room for analyzing the power savings done by the Data driven technique more efficiently.

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