A Survey on Design of Content Addressable Memories

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Abstract—**We survey the recent developments in the design of large-capacity content addressable memory (CAM). A CAM is a memory unit that process single clock cycle content matching instead of addresses using well dedicated comparison circuitry. CAM's are widely used in look-up table functions, network routers for packet forwarding. Since basic lookups are performed over the complete stored memory information, there the consumption of power will be high and the speed will be reduced with the rise of look-up data size. The most critical design challenge in CAM is to reduce power consumption associated with reduced area and increased speed. Here review of CAM-design techniques at different levels are carried out. It includes low energy match-line sensing and search-line driving methodologies. At the architectural level we review different methods for increasing the throughput and optimizing the power consumption.**

Index terms—**Content-addressable memory (CAM), WOS, RWOS, POP**

I. INTRODUCTION

CONTENT ADDRESSABLE MEMORY (CAM) is also called an associative memory that compares input search data with the look-up table, and the address of the matching data is returned. CAMs have a single clock cycle through-put making them faster than other software-based and hardware searching schemes. CAMs can be used in huge applications requiring increased search speed with reduced energy consumption. These applications include parametric curve extraction [1], Hough transformation [2], Huffman coding/decoding, Lempel–Ziv compression [3], human body communication controller [4], a periodic event generator, cache memory [5], a virus detection processor [6] and image coding.

CAM is a best choice for implementing large capacity lookup operation due to its advantage of fast searching capability. However, the speed of CAM can be increased at the cost of enlarged silicon area and power consumption, challenge of the designer is to improve the speed of search without increasing the area and power requirement. As CAM applications grow, the need for larger CAM size rises, the power related problems also gets exacerbated. In this paper, we survey developments in the CAM using circuit level and architecture level. Before entering into the paper, we first briefly introduce the basic CAM types and their operations. The CAM design contains an input controller for search data, look-up data or look-up table for comparison and an encoder for locating the address of the data.

In CAM each word circuit contains several dozens of CAM cells. Each input-search bit is compared with its CAM-cell bit and if the comparison matches then the pass transistor in the CAM cell attached to the match line (ML) of a word circuit is in on state, else it will be in off state. CAM cells are classified into two types: NOR [7] and NAND [8], [9]. There are modified cell structures such as XOR cells, the combination of NAND and NOR cells called NAND-NOR cell design are also reviewed. A NOR-type word circuit operates at high speed because the pass transistor in the CAM are connected between Match Line to a ground line in parallel.it consumes large power because mismatched word circuits discharge their ML capacitances to the ground line, where almost all except one or two of the word circuits will not be in matched state. Whereas in NAND-type word circuit works in average speed, it is because pass transistors are connected in series between a ML and a ground line. Here very few are matched word circuits and they discharge their ML capacitances. Thus a NAND-type word circuit requires less power in match-line sensing compared to the NOR-type word circuit.Some more approaches to reduce the power dissipation of the ML's have been proposed using low-voltage-swing current-mode circuits with an advantage of low noise immunity [10], [11]. In [12], a power-gated ML is also reviewed to improve the speed of the CAM. To improve the throughput of the NAND-type word circuit, some techniques at the circuit level have been proposed [13], [14], [15].A pipelined approach or the parallel processing methodology is a general solution to improve the throughput [16]. To improve the throughput word overlap search mechanism, re-ordered word overlap search mechanism are studied. It also includes the combination of re-ordered word overlap search mechanism with asynchronous circuit are designed which includes the self-timed local clocking mechanism instead of global one. This methodology reduces the active time of the clocking signal leads to the reduction of the power and the performance improvement

II. REVIEW OF CONTENT-ADDRESSABLE MEMORY

Fig 1 shows a block diagram of a CAM [23]. A search-word is given to search-lines (SLs) which are compared with the tale of stored data. The number of bits in a CAM search-word is usually large. The existing implementations ranging from 36 to 144 bits.The table size of a typical CAM ranging between a

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few hundred entries to 32K entries where the address space ranging from 7 bits to 15 bits. Each stored word has a match-line that compares the search word and stored word. Then it checks whether theyare same or different. The match-lines are fed into the encoder that provides a binary match location with respect to the match-line that is in the match state. An encoder is used in a system which expects only one match. In CAM applications with more than one match, a priority encoder is used instead of a simple encoder. A priority encoder is used to select the matching location with highest priority to map to the match result. The words in lower address locations receive the higher priority. In addition, there is a hit signal which is executed when there is no matching location is find in the CAM. The function of a CAM is to take a search word, process it and executes the matching memory location.

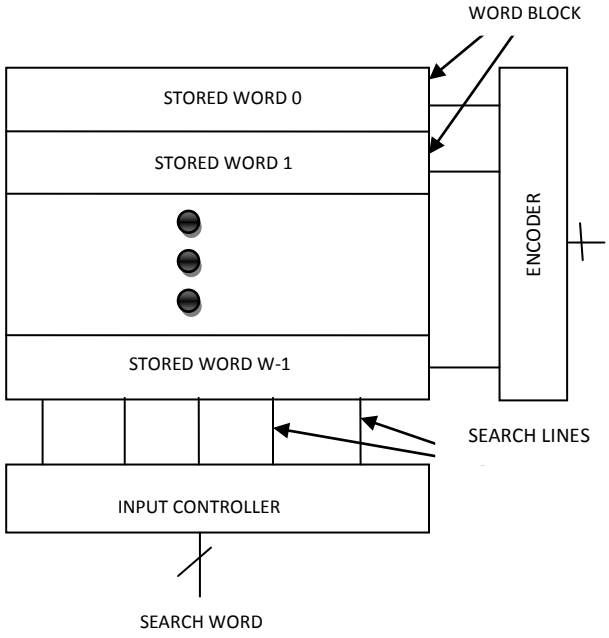

Fig 1.Block diagram of Content Addressable Memory (CAM).

III. CORE CELLS AND MATCHLINE STRUCTURE

A CAM cell does two functions. They are bit storage and bit comparison. The bit storage in NOR and NAND cells done by an SRAM cell where cross-coupled inverters implement the bit-storage nodes.

The nMOS access transistors and bit-lines are used to read and write the SRAM storage bit. The bit comparison is carried out using pass-transistor logic (PTL) which compares the stored data with search data. The bit comparison, which is logically equivalent to an XOR function of the stored bit and the search bit is implemented using the NOR and the NAND cell [7].

A. NOR cell implementation

Traditionally, there are two types of CAM cell implementations [17]. As shown in Fig.2, one is NOR-type design and the other is NAND-type cell design. In NOR-type CAM design, The CAM cell isusually of XOR-type and the nMOS transistors of each CAM cell are not arranged in NOR type cell (the nMOS are connected in parallel).During thepre-charge phase, the match line is initially pre-charged to high and when a mismatch occurs, the match line would be discharged to 0. Only when all cells are matched, i.e. for every mismatch there occurs, the capacitance to discharge most ofthe cells will be mismatched and thus consumes high power. The pull-down path is very short, so discharge occurs quickly.The pull-down transistors arranged in NOR type is good for searching, but they add drain capacitance to the match line. This results in high power dissipation in match line switching. Thus NOR cell provides the best performance with increased power consumption

In contrast to the NOR-type CAM design, the NAND-type CAM cell aims in the reduction of the power dissipation

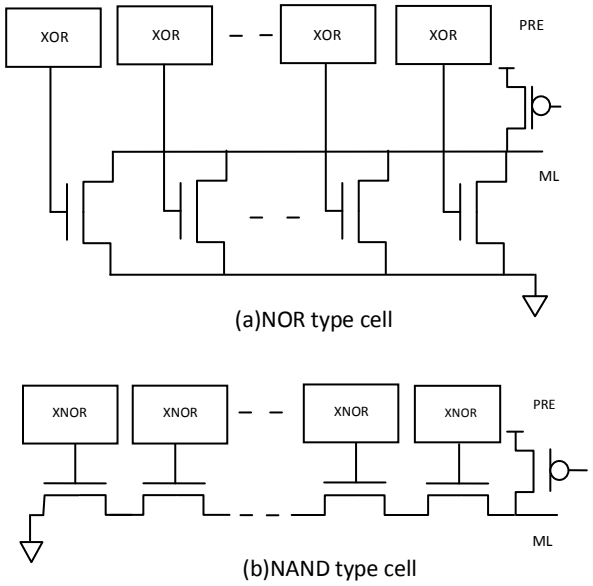

Fig2. CAM cell implementation on (a) NOR cell,(b) NAND cell

.during the search operation, here the CAM cell is implemented using XNOR-type instead of XOR-type, and the

B. NAND cell implementation

nMOS transistors of each CAM cell in the same word are arranged in NAND type[22], as shown in Fig. 2(b). The match line is initially pre-charged to high as in NOR cell, and discharged to 0 only when all CAM cells are matched else they will remain in the pre-charge phase itself. The load

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capacitance of match line is small (because the nMOS cells are connected in series) and only one match line is discharged to 0 during a search.so the power consumption is minimum. However, the pull-down path is too long, so the match line discharge is very slow for a match. Thus, the NAND-type CAM operates in medium speed with extreme power saving.

IV. HYBRID-TYPE CAM DESIGN

Due to the parallel comparison feature large numbers of transistors arein on state for all lookup [18]. However, the energy consumption of CAM is usually reasonable. Here a hybrid-type CAM is designed which aims to combine the performance advantage of the NOR-type CAM with the power efficiency of the NAND-type CAM. The CAM word is divided into two segments. By reducing both the match line capacitances and switching activities, the energyconsumption is diminished roughly by 89% compared to the NOR-type CAM. It is because the hybrid-type CAM offers a fast pull-down path to accelerate the light weight match-line discharge, the search-line performance of the hybrid design is also better than that of the NOR-type CAM. The CAM implementation is carried out in two stages. They are:

Pre-charge Phase: In the pre-charge phase, the control signal PRE is low state. Thus the match-line (ML) is firstly pre-charged to high. It is because the pull-down transistors T1, T2 and T3 are discharged bynMOS transistors N1, N2, and N3 respectively and there is no path to ground, therefore no need for discharging all bit lines to 0 to prevent the unexpectedshort-circuit during the pre-charge phase. Compared to the traditional CAM implementation, this design is more efficient in bit line power saving.

Match Evaluation Phase: After the pre-charge phase, the control signal PRE is asserted high and the search data have to be loaded on the bit lines to start the matching process. This phase is called match evaluation phase. Here the CAM word is divided into two segments, i.e., SEG_1 and SEG_2 depending on the match results of each segment there are four possible cases in the match evaluation:

Case 1:SEG_1 Is Mismatched and SEG_2 Is Mismatched/ Matched.

Case 2:SEG_1 Is Matched and SEG_2 Is Mismatched.

Case 3:SEG_1 is Matched and SEG_2 Is Matched.

VI. SELF-TIMED WORD OVERLAPPED SEARCH MECHANISM

In the proposed methodology it uses the self–timed overlapped search mechanism for improving the throughput with low power search-line implementation [22]. The word The real match occurs only when both SEG_1 and SEG_2 matches.

V. SYNCHRONOUS OVERAPPED SEARCH MECHANISM

Synchronous overlapped search mechanism is a high speed data search mechanism [19]. Here it moves to next search only after completing the current search. The current word search speed is improved by including some pre-computation methodologies[20],[21].it does not contains any delay elements, hence it provides good timing variation and also maintains high through-put under process variation.in this paper a 128 X 64 bit CAM is designed under 45 nm CMOS technology with 30% threshold voltage variation. It operates 42 times faster than the conventional hybrid type CAM with 12% energy overhead.

The proposed methodology it is executed using 1) synchronous word overlapped searchmechanism 2) synchronous phaseoverlappedprocessing. Each sub-word has its self-pre-charge circuitry. In this CAM architecture the input controller has the input search data and a comparator compares the search word with the data stored in the CAM.

The search mechanism is carried out segmenting the search data and stored data with k sub-word with minimum size and the sub-sequent sub-word with remaining (n-k) bits. Here the k is set as 5-bit 1st sub-word circuit and (n-k) set as 59-bit sub-word circuit. The input controller sends a search word to the CAM at both high and low transitions of the clock signal. The 1st segment operates at all m transitions, whereas 2ndsegment requires only (m-1) transitions along with this the pre-charge operation takes one transition. Once 1st segment matches the MLR10 goes high, else remains low. The ML is charged through pass transistor (PMOS) once the current search is completed and is used to connect with the 2nd segment.

A feedback transistor is used to avoid the problem due to charge sharing while using NAND type of cell [7]. In the 2nd segment it has 12 local match circuits and one global match circuit.it is activated only when the 1st sub-word circuit matches. The 59 bits in the 2nd segment are divided into 5-bit 11 sub-sub words and one 4-bit sub-sub word. If it matches in the local search, LML1 becomes high and the global clock signal MLR20 goes high. The high output signal is sent to encoder or priority encoder to find the location of match.

circuit is divided into two segments and most of the mismatch can be found by searching first few bits itself improves speed and the unused 2nd segment can be used to improve the throughput. It can be achieved by initializing the unused match-line as soon as 1st stage search is completed.

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The overlapped search mechanism is realized using a self-timed word circuit which uses local control signal that reduces power consumption by using global clock. The circuit implementation is as follows: it contains an 8-bit 1ddt stage sub-word circuit, a segmentation circuit, a pre-charge circuitry and a 136-bit 2nd stage sub-word circuit. The 8-bit 1st stage is implemented using a series of 8 NAND type cells, a pre-charge circuit [7], and a week feedback PMOS transistor for avoiding the problem due to charge sharing.

The input controller compares the 1st stage with the 8-bit stored data. If it matches ML10 signal goes high else remains low. The PMOS transistor acts as the pass transistor which connects ML10 to 136-bit 2nd stage. The 136-bit is divided into 17 local and 1 global match circuits. Once ML10 is initiated all the 17 local match circuit operates in parallel and is partitioned into 8-bit 17 sub-sub-words. LMLi (i=0, 1... , 17) is high when match occurs. Each LMLi is connected to global match circuit. When all LMLi goes high the global output signal ML20 also goes high.

VII. ASYNCHRONOUS RE-ORDERED WORD OVERLAPPED SEARCH MECHANISM

The proposed methodology introduces a re-ordered word overlapped search mechanism for low power and high throughput [23]. To reduce the power consumption the word circuit is divided into two segments that are searched sequentially or in parallel. Since most of the search is carried out in the first stage search itself. Then 2nd stage remains unused. The 2nd stage is initiated asynchronously and searching is done by using the unused match-lines. Thus the throughput can be improved. Each word circuit is controlled independently by a clocking signal generated locally. This allows the circuit to be in the required phase for its own operation. The phases includes evaluate and pre-charge instead of synchronous operation thus lowers the cycle time. Here it uses the 128 X 64 bit CAM under 90 nm CMOS technology.The circuit implementation is based on the RWOS and POP scheme. It includes the k bit 1st stage sub-word, asegmentation circuit, a self-pre-charge circuit and a (n-k) bit 2nd stage sub-word circuit. The 1st stage is implemented using a series of NAND type cells, a pre-charge PMOS transistor and a week feedback PMOS transistor. Initially the last k bits are compared with the last k bits of the stored data and MLS10 is high when the 1st segment matches. The weak feedback PMOS transistor is added to solve the problem due to charge sharing. The 2nd stage contains ((n-k) /k) local match circuits and a global match circuit. Each LMLi ($0 \leq I < ((n - k) / k)$) goes high when its sub-sub-word matches or low when mismatch occurs. All outputs LMLi are connected to global match-line when the word matches and ML20 is asserted. Here the delay element and a combinatorial block are designed separately called bundled-data logic style. The delay element is designed using the dummy word circuit of the sub-word circuit and several AND gates. The dummy word reduces the delay difference between the delay element and the sub-word circuits.

VIII. COMPARISON

In this paper we have reviewed four types of CAM designs for improving the throughput and reducing the power consumption without losing the performance. According to the table I the hybrid type CAM [18], the power consumption is 1.3fj/bit/search that is 89% less than the traditional CAM designs. This is achieved by reducing the energy consumption for search-line implementation. The cycle time is also increased much compared to the traditional technologies. The transistor count is also reduced from 11 to 9. But the cycle time is not at most optimized.

In the synchronous CAM [19], the energy consumption is 0.227 fJ/bit/search which is 18% lessthan the hybrid type CAM and the cycle time is increased to 1.025 ns from 0.6 ns with 8% area overhead. It is better than hybrid CAM, but the cycle time is high. To improve the throughput we move to the synchronous WOS with POP mechanismIn the synchronous WOS with POP mechanism [22] the 128 X 64 bit CAM is designed using the binary CAM in 45 nm technology. Here the throughput is increased 45 times than the conventional type CAM. The energy consumption is 0.255 fj/bit/search with an energy overhead of 12.3%. By using the re-ordered word overlapped search mechanism the performance and threshold can be optimized further.In the asynchronous CAM design using the re-ordered word overlapped search mechanism [23], based on Phase overlapped processing the cycle time is reduced to0.26ns under a 90 nm CMOS technology. This asynchronous CAM operates 5.98 times more rapidly than a synchronous with 14.2% reduced energy dissipation. The post-layout proposed CAM achieves 385-ps cycle delay time and 0.773 fJ/bit/search and under different PVT variations. it

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TABLE I

COMPARISON ON VARIOUS TYPES OF CAM

	Hybrid CAM	**Sync CAM**	**Sync WOS CAM**	**Async RWOS CAM**
Configuration	128 X 32	128 X 64	128 X 64	256 X 144
CAM type	TCAM	TCAM	BCAM	BCAM
Technology used	0.13 μm	45 nm	45 nm	90 nm
Cycle time(ns)	0.6	1.025	0.242	0.26
Energy metric(fj/bit/search)	1.3	0.227	0.255	0.162
No: of transistors	9	9	9	9

operates properly. Hence the asynchronous CAM design is the best compared to the synchronous type and hybrid type CAM.

IX. CONCLUSION

In this paper we have reviewed the different CAM architectures including the hybrid type CAM, Synchronous CAM, synchronous WOS CAM with POP mechanism and the asynchronous self-timed re-ordered overlapped CAM with POP mechanism. The asynchronous self-timed re-ordered overlapped CAM including the POP mechanism is efficient than other three architectures in both energy consumption and throughput. The energy consumption is 0.162 fj/bit/search, which is 42.7% higher than the previous type and the throughput, is also improved with cycle time 0.26 ns. Hence we conclude that the asynchronous RWOS with POP mechanism is the best of the reviewed papers.

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