IMPLEMENTATION OF SIGNED AND UNSIGNED MULTIPLIER USING EFFICIENT MODIFIED BOOTH ENCODER

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Abstract-- This paper presents the design and implementation of signed-unsigned Modified Booth Encoding (SUMBE) multiplier. The present Modified Booth Encoding (MBE) multiplier and the Baugh-Wooley multiplier perform multiplication operation on signed numbers only. The array multiplier and Braun array multipliers perform multiplication operation on unsigned numbers only. Thus, the requisite of the modern computer system is a dedicated and very high speed unique multiplier unit for signed and unsigned numbers. Therefore, this paper presents the design and implementation of SUMBE multiplier. The modified Booth Encoder circuit engenders half the partial products in parallel. By elongating sign bit of the operands and engendering an adscititious partial product the SUMBE multiplier is obtained. The Carry preserve Adder (CSA) tree and the final Carry Look ahead (CLA) adder used to expedite the multiplier operation. Since signed and unsigned multiplication operation is performed by the same multiplier unit the required hardware and the chip area reduces and cost of a system.

Index Terms: Modified Booth Encoding multiplier, Baugh Wooley multiplier, Array multiplier, Braun array multiplier, CSA, CLA, partial products, Signed-unsigned.

I. INTRODUCTION

In digital computing systems multiplication is an arithmetic operation. The multiplication operation consists of engendering partial products and then integrating these partial products the final product is obtained. Thus the speed of the multiplier depends on the number of partial product and the speed of the adder. Since the multipliers have a consequential impact on the performance of the entire system, many high performance algorithms and architectures have been proposed. The very high speed and dedicated multipliers are utilized in pipeline and vector computers. The high speed Booth multipliers and pipelined Booth multipliers are utilized for digital signal processing (DSP) applications such as for multimedia and communication systems. High speed DSP computation applications such as Fast Fourier transform (FFT) require integrations and multiplications. The papers presents a design methodology for high speed Booth encoded parallel multiplier. For partial product generation, an incipient Modified Booth encoding (MBE) scheme is utilized to ameliorate the performance of traditional MBE schemes. But this multiplier is only for signed number multiplication operation. The conventional modified Booth encoding (MBE) engenders an aberrant partial product array because of the extra partial product bit at the least consequential bit position of each partial product row. Therefore papers presents a simple approach to engender a conventional partial product array with fewer partial product rows and negligible overhead, thereby lowering the involution of partial product reduction and reducing the area, delay, and power of MBE multipliers. But the drawback of this multiplier is that it functions only for signed number operands. The modified-Booth algorithm is extensively utilized for high-speed multiplier circuits. Once, when array multipliers were utilized, the reduced number of engendered partial products significantly amended multiplier performance. In designs predicated on reduction trees with logarithmic logic depth, however, the reduced number of partial products has a inhibited impact on overall performance. The Baugh-Wooley algorithm is a different scheme for signed multiplication, but is not so widely adopted because it may be perplexed to deploy on eccentric reduction trees. Again the Baugh-Wooley algorithm is for only signed number multiplication. The array multipliers and Braun array multipliers operates only

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on the unsigned numbers. Thus, the requisite of the modern computer system is a dedicated and very high speed multiplier unit that can perform multiplication operation on signed as well as unsigned numbers. In this paper we designed and implemented a dedicated multiplier unit that can perform multiplication operation on both signed and unsigned numbers, and this multiplier is called as SUMBE multiplier.

2. CONVENTIONAL MBE MULTIPLIERS

The incipient MBE recorder was designed according to the following analysis. Table1 presents the truth table of the incipient encoding scheme. The Z signal makes output zero to compensate the in correct X2_b and neg signals. Fig. 1presents the circuit diagram of the encoder and decoder. The encoder engenders X1_b, X2_b,Z signals by encoding the three x-signals. The y LSB signal is the LSB of the y signals and the amalgamation with x -signals to determine the Row_LSB and the Neg_cin signals. Similarly,y msb Is coalesced with x-signals to determine the denotement extension signals. Fig. 2 shows an overview of the partial product array for an 8 * 8 multiplier. The designation extension circuitry developed. The convention al MBE partial products array has two drawbacks: 1) a supplemental partial product term at the (n-2)th bit position; 2) poor performance at the LSB-part. To remedy the two drawbacks,thenewequations for the Row_LSB and Neg_cin can be indited as(1) and (2) respectively

$$Row\_LSB = y_{LSB}(x2i + x2i) \quad (1)$$

$$Neg\_cin_i = x_{2i+1}\overline{(\overline{x_{2i-1} + x_{2i-1}})\,(\overline{x_{2i-1} + y_{LSB}})\,(\overline{x_{2i} + y_{LSB}})} \quad (2)$$

TABLE 1: Truth Table of MBE Scheme

b_{i+1} b_i b_{i-1}	Value	X1_a	X2_b	Z	Neg
0 0 0	0	1	0	1	0
0 0 1	1	0	1	1	0
0 1 0	1	0	1	0	0
0 1 1	2	1	0	0	0
1 0 0	-2	1	0	0	1
1 0 1	-1	0	1	0	1
1 1 0	-1	0	1	1	1
1 1 1	0	1	0	1	1

Fig. 2(a) has widely been adopted in parallel multiplier

Since it can reduce the number of partial product rows to be integrated by a moiety, thus reducing the size and enhancing the speed of reduction tree. However, as shown Fig. 1(a), the conventional MBE algorithm engenders n/2 + 1 partial product rows rather than n/2 due to the extra partial product bit (neg bit) at the least consequential bit position of each partial product row for negative encoding, leading to an anomalous partial product array and an intricate reduction tree. Therefore the modified booth multiplier with a conventional partial product array engenders a very customary partial product array, as shown in Fig. 3. Not only each Neg is shifted to left and superseded by Ci but additionally the last neg bit is abstracted this approach reduces the partial product n/2+1 to n/2 by incorporating the last neg bit into the designation extension bits of the first partial product row, and virtually no overhead is introduced to the partial product array and fewer partial product rows result in a diminutive and expeditious reduction tree, so that area, delay, and power of MBE multipliers can further be reduced.

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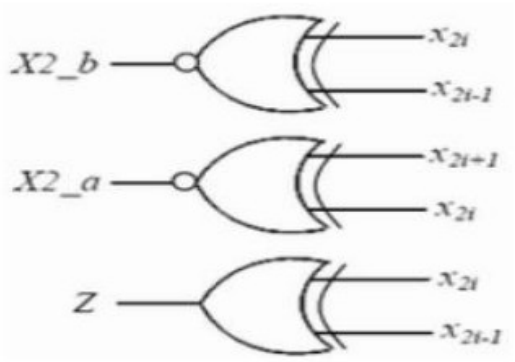

Fig: Decoder For MBE

3. PROPOSED SUMBE MULTIPLIER

The main goal of this paper is to design and implement 16x16 multiplier for signed unsigned numbers utilizing MBE technique. Table2 shows that truth table of MBE scheme. From table2 the MBE logic and considering other conditions the Boolean expression for one bit partial product engenderer is given by equation 3.

b_{i+1} b_i b_{i-1}	Value	X1_a	X2_b	Z	Neg
0 0 0	0	1	0	1	0
0 0 1	1	0	1	1	0
0 1 0	1	0	1	0	0
0 1 1	2	1	0	0	0
1 0 0	-2	1	0	0	1
1 0 1	-1	0	1	0	1
1 1 0	-1	0	1	1	1
1 1 1	0	1	0	1	0

Fig: Truth table of MBE scheme

$$P_{ij} = \overline{(\overline{a_i + b_{i+1}} + \overline{b_{i-1} + b_i})\,(\overline{a_{i-1} + b_{i+1}} + \overline{b_i + b_{i+1}} + b_{i-1} + b_i)}$$

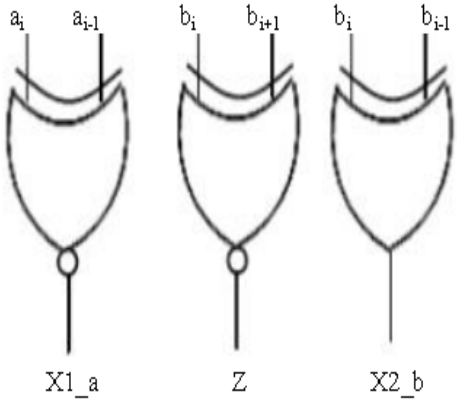

Fig: Logic Diagram of MBE

Equation 3 is implemented as shown in Fig. 3.The SUMBE multiplier does not discretely consider the encoder and the decoder logic, but instead implemented as a single unit called partial product engenderer as shown in Fig. 3.The negative partial products are converted into 2's complement by integrating a negative (Ni) bit. An expression for negate bit is given by the Boolean equation4. This equation is implemented as shown in Fig. 4. The required signed extension to convert 2's complement singed multiplier into both signed-unsigned multipliers is given by the equation 3 and 4. For Boolean equations 5 and 6 the corresponding logic diagram is shown in Fig. 5.

$$N_i = b_{i+1}\,\overline{(b_{i-1}\,b_i)}$$

$$a_{16} = s\_u.a_{15}$$

$$b_{16} = s\_u.b_{15}$$

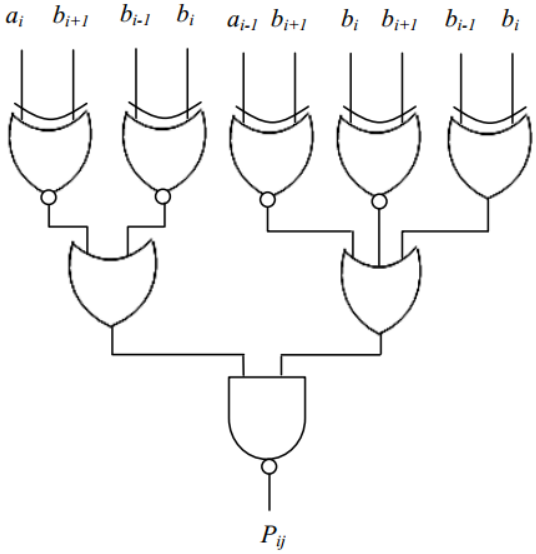

Fig: Logic diagram of 1-bit partial product generator

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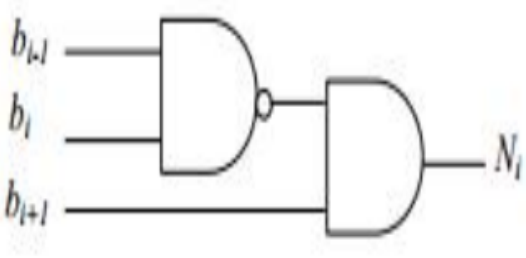

Fig: Logic Diagram of negate bit generator

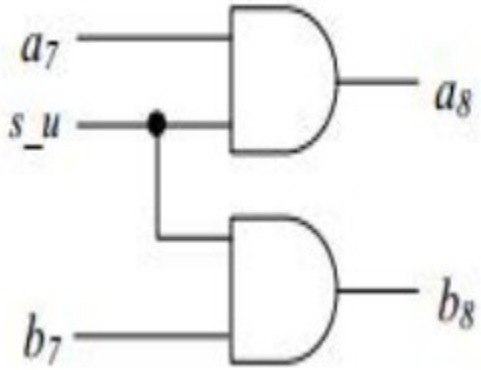

Fig: Logic Diagram of sign converter

The working principle of designation extension that converts signed multiplier signed - unsigned multiplier as follows. One bit control signal called signed-unsigned (s_u) bit is utilized to designate whether the multiplication operation is signed number or unsigned number. When sign - unsigned (s_u) = 0 it designates unsigned number multiplication, and when s_u=1, it denotes signed number multiplication. It is required that when the operation is unsigned multiplication the denotement the elongated bit both multiplication and multiplier should be elongated with 0, that is a 16=a17=b16=b17= 0.Is required that when the operation is signed multiplication the denotement elongated bit depends on whether the multiplication is negative or the multiplier is negative or both the operands are negative. For this when the multiplicand operand is negative and multiplier operand is positive operand is negative and multiplier operand is positive the denotement elongated bit should be engendered are s_u=1, a15= 1, b15= 0, a16= a17=0, and b16= b17=1.Table 3 shows the SUMBE multiplier operation.

Sign-unsigned	Type of operation
0	Unsigned multiplication
1	Signed multiplication

Fig:SUMBE operation

Shows the partial products engendered by partial product engenderer circuit which is shown in Fig. 3. There are 5-partial products which designation extension and negate bit Ni.all the 9-partial products are engendered in parallel.

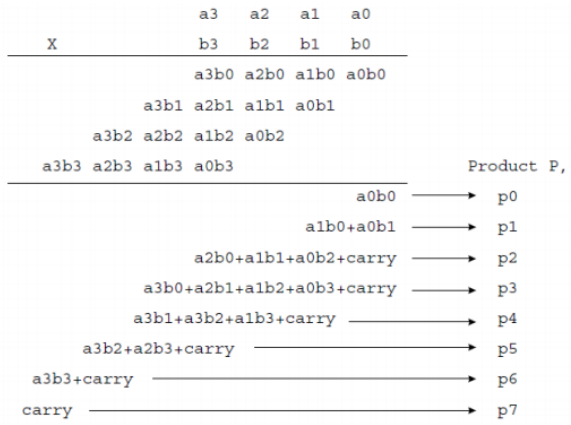

Fig: multiplier for signed-unsigned numbers using bugh vally

there are 9-partial products namely X1, X2, X3,X4, X5, X6, X7, X8and X9. These are 9-partial products are integrated by the carry preserve adders (CSA) and the final stage is carry look ahead (CLA) adder as shown in Fig.7.Each CSA adder takes three inputs and engender sum and carry in parallel. There are three CSAs, five partial products are integrated by the CSA tree and determinately when there are only two outputs left out then conclusively CLA adder is utilized to engender the final result. Assuming each gate delay an unit delay, including partial product engenderer circuit delay, then the total through the CSA and CLA is 3+4=7 unit delay. Thus with present profoundly and immensely colossal scale integration (VLSI) the total delay is estimated around 0.7 nanosecond and the multiplier operates at giga hertz frequency.

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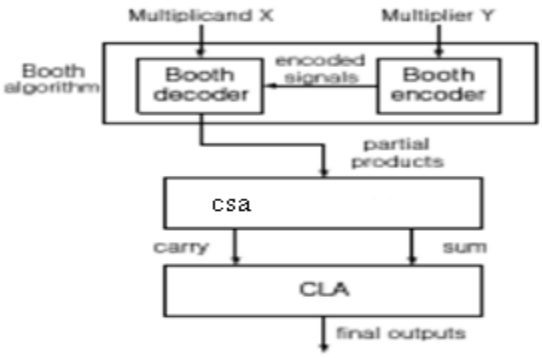


Fig: Architecture of the modified Booth multiplier

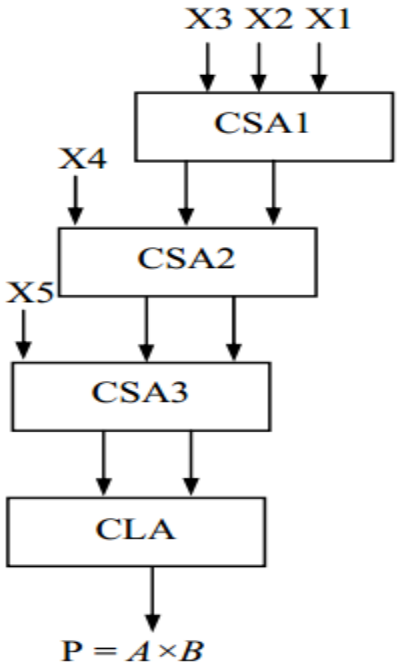
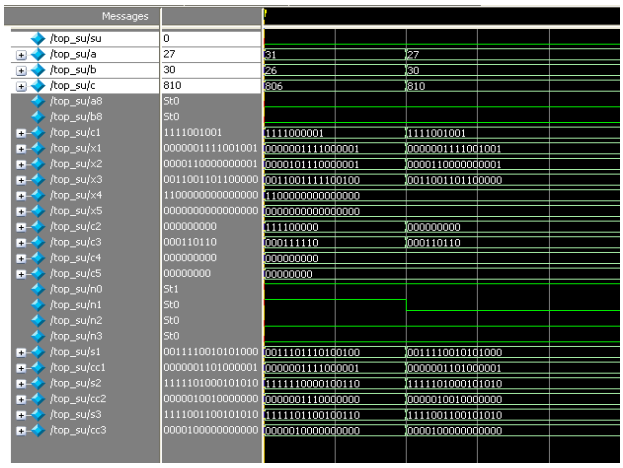


Fig: Partial product adder logic

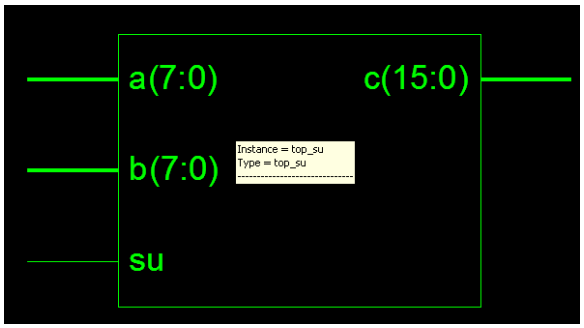
IV. SIMULATION RESULTS

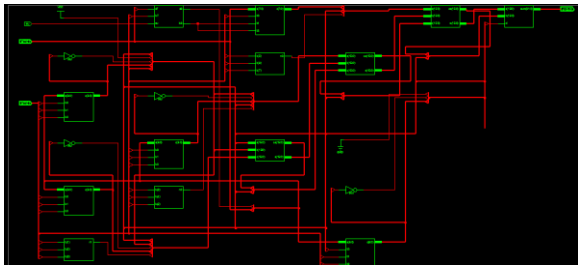
Verilog code is indited to engender the required hardware and to engender the partial product, for CSA adder, and CLA integrated.



SYNTHESIS REPORT:

Device Utilization Summary (estimated values)		
Logic Utilization	Used	Available
Number of Slices	91	4656
Number of 4 input LUTs	161	9312
Number of bonded IOBs	33	232





V. CONCLUSION

In all multiplication operation product is obtained by integrating partial products. Thus the

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final speed of the multiplier circuit depends on the speed of the adder circuit and the number of partial products engendered. If radix 8 Booth encodind technique is utilized then there are only 3 partial products and for that only one CSA and a CLA is required to engender the final product.

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