Application of Error Correction Code For Pipelined Filters with Efficient Addition Structure

Mr.B.Ganesamoorthy, P.Jeevitha

***Abstract*- Filters play a vital role in digital signal processing systems.In order to obtain the realiable operation, the filters are protected using the error correction codes.The pipelined filter structure can be used for obtaining the increase in the clock speed or the sample speed or to reduce the power consumption at the same speed in the design and also to retain the filter properties.This pipelining transformation leads to reduction in the critical path.To achieve the fault tolerance these filters are applied with the error correction code.The pipelined filter structure is modified at the adder section for efficient operation is to be proposed.The efficient operation in terms provides reduced processing time with lower power consumption.The proposed filter structure can be operated at the lower supply voltage to meet the clock period or the sample period constraints.These proposed technique is applied for the finite impulse response filters.**

Index terms- Soft errors,Error Correction Codes(ECC),filters.

I. INTRODUCTION

The Digital filter structures are studied using [1]. The FIR filter error correction is studied using [2].The filters are mainly used to reject the unwanted components inorder to provide the better quality signal at the output.These filters are playing a vital role in the signal processing and communication system image enhancement,noise and echo cancellation,etc.There are two main kinds of filters,they are analog and digital.In analog filters the output and the input are the analog signal.Eventhough these filters are fast and simple to realize,they are little in stable.So,nowadays the analog filters are replced with the digital filters because of performing the numerical calculations on the sampled signal value and also these filters eliminate the drawbacks of the analog filters.These digital filters are further classified into two types:1.FIR(Finite Impulse Response) filter,2.IIR(Infinite Impulse Response) filter [3].The FIR filter is preferred over the IIR filter because of efficient implementation with fewer finite precision error.and having better stability with linear phase.

The pipelined and non pipelined FIR and IIR filter is designed and implemented in FPGA's in order to analyse the delay and frequency of each design [4].The objective used is,enhancing the individual block speed in the digital system leads to the enhancement of the overall system speed The three different pipelined structure (i.e) direct form-1,fine grain and broadcast are used for designing the FIR filter.These can be synthesized using the Xilinx synthesis tool and can be implemented using the Spartan 3A FPGA family.These experiment generates the result that the fire grain structure is used for the effective area utilization,and the direct form-1 structure used for the higher speed operation [5].The digital filters are more versatile and as the ability to process the signal in various ways and it also as the ability to adapt the changes in the characteristics of the signal.

The individual block speed enhancement leads to the whole system speed enhancement [6].Pipelining is a technique called overlapping of multiple instructions during execution.By using this technique the optimized speed and the minimal hardware cost of the FIR filter design is being achieved.Also by using these technique the dalay at the filter is to be reduced on comparing with the non pipelined structure [7].The tapped line delay structure and the transposed filter structure has been studied and the filter is also implemented with the Distributed arithmetic and Symmetric convolution technique.These has been synthesized using the ModelSim XE simulator and implemented using the Spartan 3E FPGA family.

Different methods used for implementing the Finite Impulse Response filter that include Modified Booth encoding algorithm along with the spurious power suppression technique for getting the reduced area utilization and lower power operation.The better solution fo the realization of the filters is the multistage digital filter.By combining the decimation/interpolation operations related to the implementation of multi channel filter in the pipelining interleaving technique can give an efficient multistage multichannel digital filter.

In the brief,this paper gives the implementation of efficient pipelined filter also further achieving a fault tolerant realiable operation by implementing this filter with the redundant module.

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Mr.B.Ganesamoorthy*, Electronics and Communication Engineering, Adhiparasakthi Engineering College,, Melmaruvathur,Tamil Nadu,India,, Mobile No:9600321227.*

P.Jeevitha*, Electronics and Communication Engineering , Adhiparasakthi Engineering College, Melmaruvathur,Tamil Nadu,India,, Mobile No:9047359623.*

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II. EXISTING FILTER STRUCTURE

The existing pipeline filter structure is shown in the Fig.1.This filter structure is designed for four input and four filter coefficients.The four filters are considered to be x1,x2,x3 and x4 and the filter coefficients are found to be h0,h1,h2 and h3.The output generated will be y1,y2,y3 and y4.

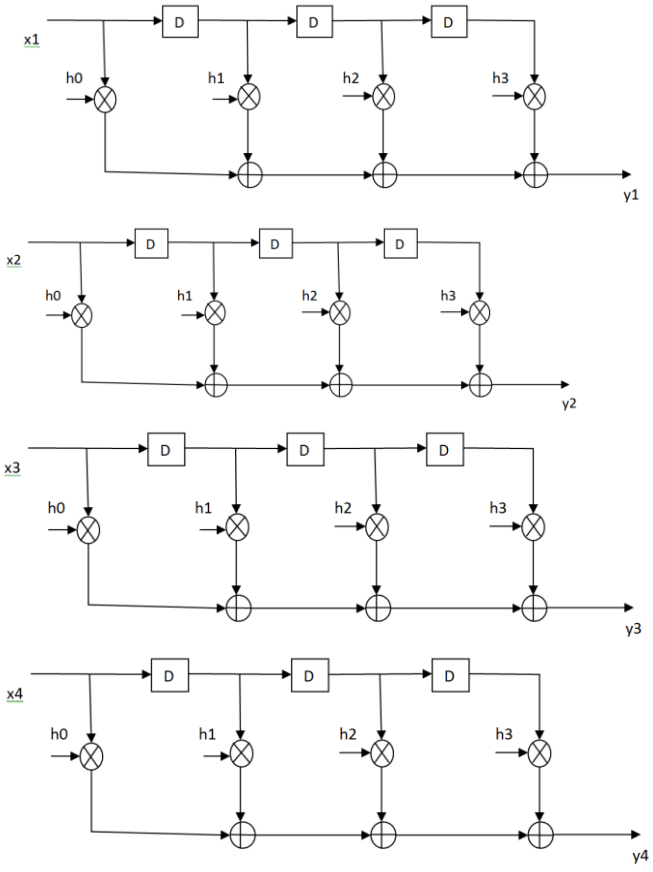

Fig.1 Four filter pipelined structure

A. *Original Module*

The original module should be represented in the Fig.1.In this module the applied input get convoluted by using its filter coefficients then it generates the convoluted output.The original module operates on the given below equation.

$$y[n] = \sum_{l=0}^{\infty} (x[n-l])\,h[l]$$

B. *Redundant Module*

The redundant module is the module used for achieving the realiable operation over the original module.The redundant module is said to be the parity module which is used to generate the parity bits.These parity bits are represented as z1,z2,z3.The module takes a block of k bits and generated the block of n bits and the parity is obtained as n-k bits.

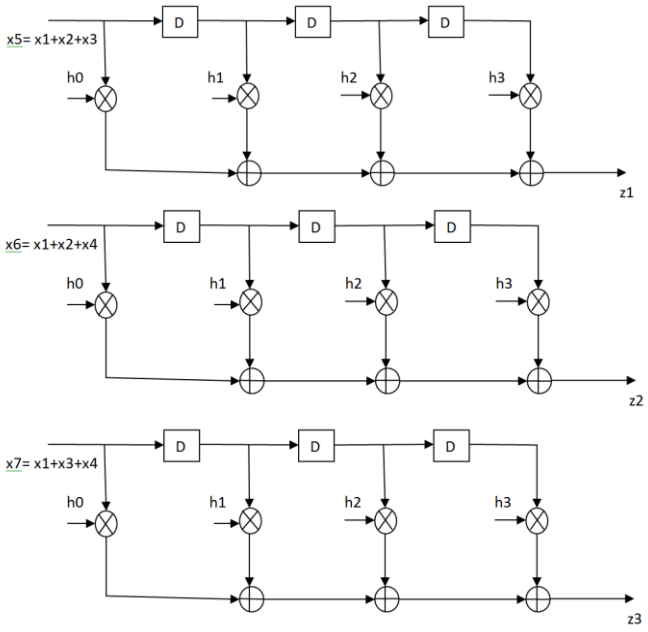

Fig.2 Redundant module

C. *Single error correction module*

The single error correction module is used to correct the single bit error in the generated or convoluted output at the original module. By applying the parity over the original module the error in the bit at the convoluted output is to be detected and corrected with the help of equation given below.

$$Z1[n] = \sum_{l=0}^{\infty}(x1[n-l] + x2[n-l] + x3[n-l])h[l]$$

$$Z2[n] = \sum_{l=0}^{\infty}(x1[n-l] + x2[n-l] + x4[n-l])h[l]$$

$$Z3[n] = \sum_{l=0}^{\infty}(x1[n-l] + x3[n-l] + x4[n-l])h[l]$$

The single error correction module is given in the below Fig.3.

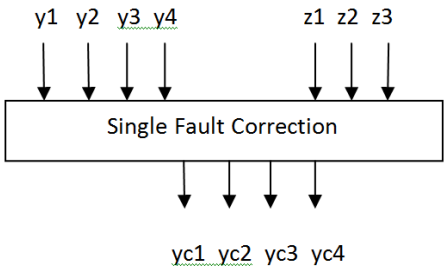

Fig.3.Single error correction module

III. PROPOSED FILTER STRUCTURE

The proposed filter structure has a difference in the adder structure implementation as compared with the existing pipeline structure. These efficient adder structure implementation in the pipelined filter is given in the Fig.4. below.

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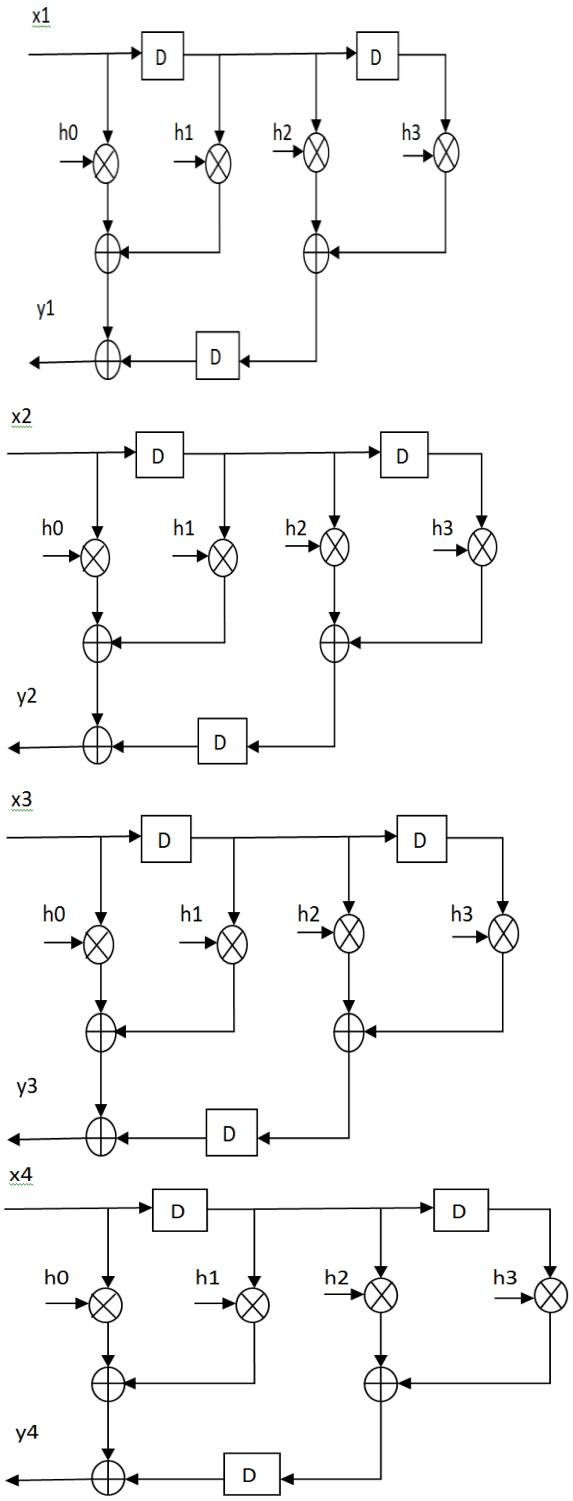

Fig.4.Proposed Efficient Adder Pipelined Structure

A. *Original Module*

The original module is represented in the Fig.5.In this module the applied input get convoluted by using the efficient adder structure.The original module is represented in same Fig.4.

B. *Redundant Module*

The redundant module is same as that of the existing systems redundant module used for achieving the reliable operation over the main module.These module is used for generating the parity bits also represented as z1,z2 and z3.The parity is calculated as n-k bits.Let as consider a simple example of Hamming code with k=4 and n=7,here the parity bits p1,p2 and p3 are computed based on the data bits d1,d2,d3 and d4 as follows:

$$p1 = d1 \pm d2 \pm d3$$
$$p2 = d1 \pm d2 \pm d4$$
$$p3 = d1 \pm d3 \pm d4$$

The redundant module for the proposed system is shown in the Fig.5.

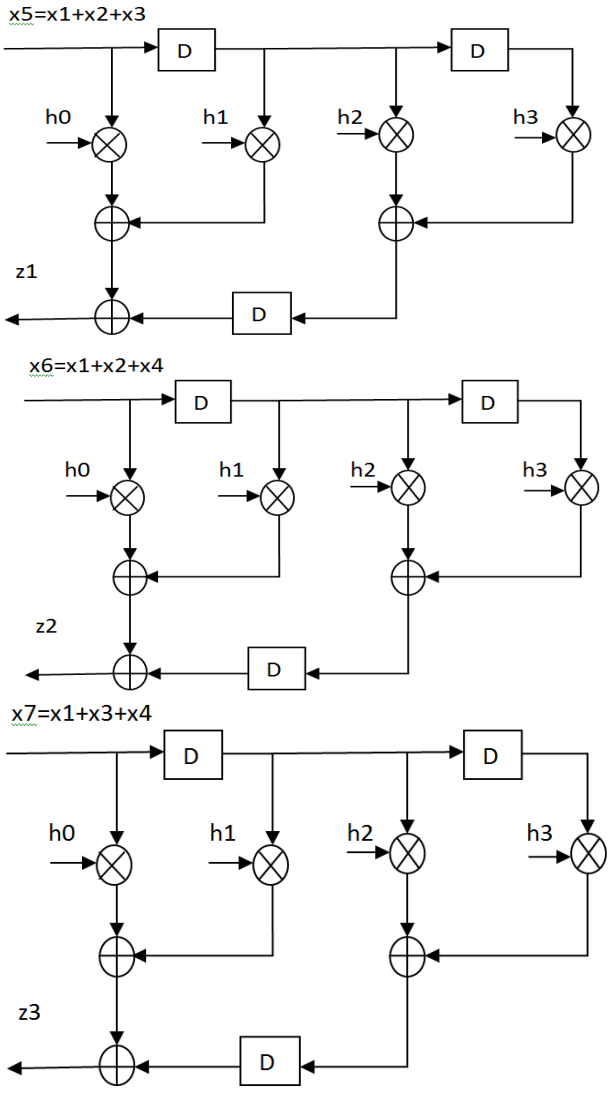

Fig.5. Proposed Redundant Module

C. *Single Error Correction Module*

The single error correction module is used to correct the single bit error in the generated convoluted output at the proposed area efficient adder structure.The single error correction module is shown in the Fig.6.

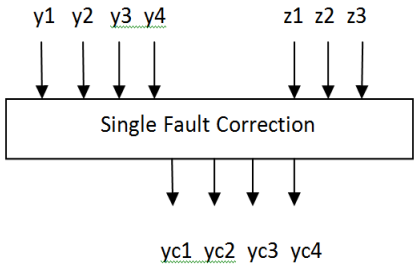

Fig.6 Proposed Single Error Correction Module

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IV. SIMULATION RESULTS

The Simulation results and the RTL schematic for the existing and proposed module are given below:

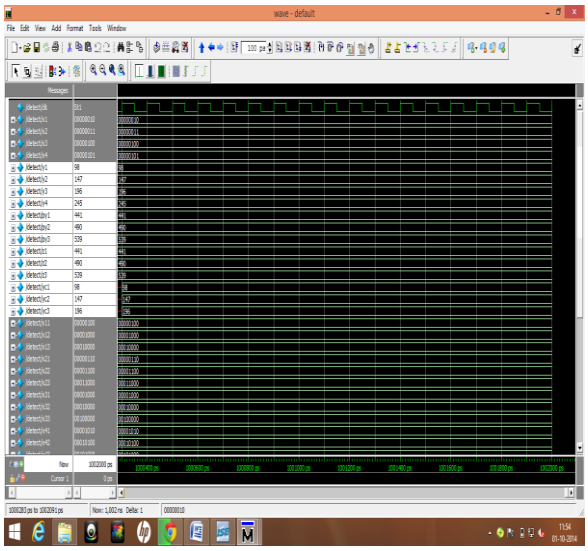
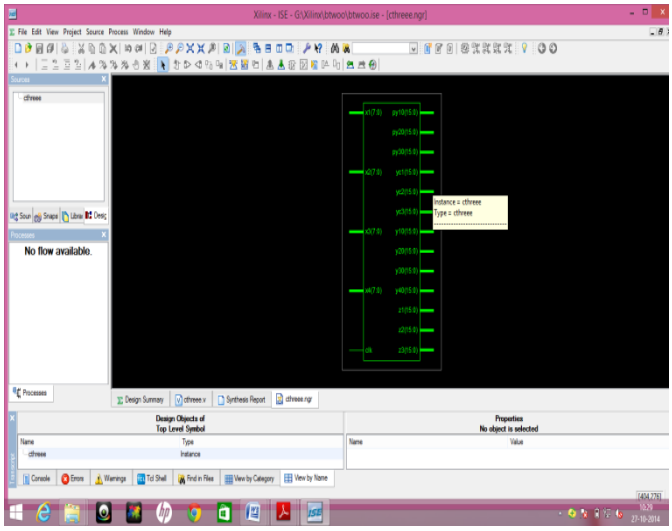
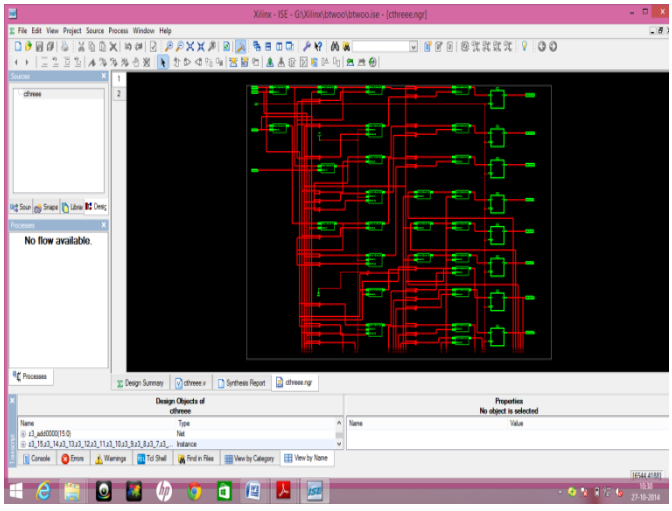


Fig.7. Simulation result for the Existing system





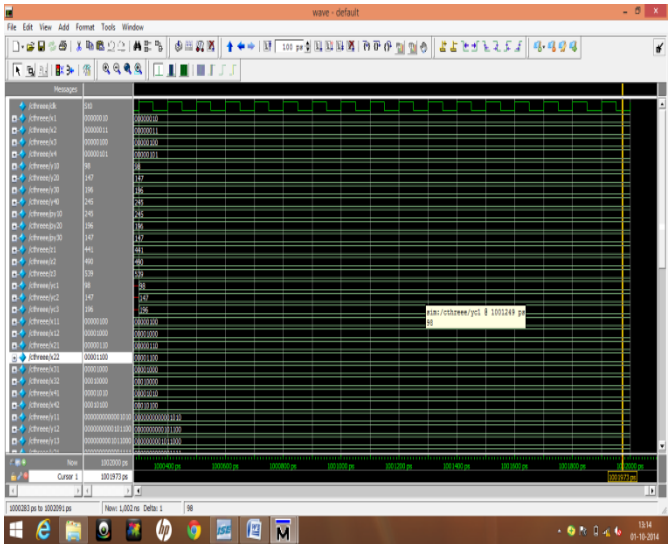


Fig.9.Simulation Result of proposed system

Table 1. Comparison table for Existing and Proposed Blocks

	Unprotected	Existing system	Proposed system
Slices	2093	2098	2061
Flipflops	1235	1248	1210
LUT's	5672	5688	5123
Gclks	12%	14%	5%
No.bonded IOB's	31%	28%	12%
Power(mW)	323	329	309
Time period	49.89ns	51.46ns	44.76ns

V. CONCLUSION

In this paper, the Filter is designed with efficient adder implementation for getting the reduced power.The modified adder structure generates the similar result as that of the existing module.The power consumption should be reduced from 315mW to 309mW.The resource utilization can be obtained by analyzing the slices,flipflops,used gate clk's,and IOB's.The single bit error correction is achieved by using the Hamming Error Correction Code in the proposed system.

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B. Ganesamoorthy received his B.E (Electronics andCommunication Engineering) from GovernmentCollege of Engineering Bargur in May 2004 and M.E (Applied Electronics) from College of Engineering, Guindy in May 2008. He is now with Adhiparasakthi Engineering College, Melmaruvathur as Assistant Professor.

P.Jeevitha received her B.E (Electronics and CommunicationEngineering) from Adhiparasakthi Engineering College,Melmaruvathur in April 2013 and pursuing M.E (VLSI Design) in Adhiparasakthi Engineering College.

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