AREA EFFICIENT ENCODING TECHNIQUE FOR REDUCING POWER IN DSRC

,K.UMADEVI[1], Mr.S.PRAKASH[2] ,Mr.K.MATHIVANAN[3]

PG scholar, Assistant professors,Dept.Of.ECE,
Adhiparasakthi Engineering College, Melmaruvathur.

Abstract----The Dedicated Short Range Communication is an emerging Technique. It is one way or two way short range to medium range wireless communication which is important in real time applications such as safety application commercial vehicle application emergency warning system for vehicle and intersection collision avoidance etc. The DSRC adopts the FM0/MANCHESTER code. The codes are used to achieve dc-balance and signal reliability. The similarity oriented logic simplification Technique (SOLS) is used here. This method is used to overcome the limitations and it also used to improve the hardware utilization rate. In these both coding have the number of the components. In this paper analyzed to reduce the number of components. Using the both code to reduce the power, delay, area in DSRC. The power consumption is 29392.843nW for Manchester and fm0 encoding, and area is 203μM². This paper implemented in cadence software.

Key words—DSRC,FM0,MANCHESTER,SOLS.

I. INTRODUCTION

The dedicated short range communication is a protocol for one or two way medium range communication. The DSRC can be briefly classified into two categories: automobile-to-automobile and automobile-to roadside. In automobile-to-automobile, the DSRC enables the message sending and broadcasting among automobile. The automobile-to-roadside focuses on the intelligent transportation service, such as electronic toll collection (ETC).The DSRC architecture having the transceiver. The transceiver having the baseband processing, RF front end and microprocessor. The microprocessor is used to transfer the instruction to the baseband processing and RF front end. the RF front end is used to transmit and receive the wireless signals using the antenna. The baseband processing is responsible for modulation, error correction, encoding and synchronization. The transmitted signal consists of the arbitrary binary sequence, it is very difficult to obtain the dc-balance.the fm0 and Manchester are provide the transmitted signal and then the dc-balance. The (SOLS) similarity oriented logic simplification having the two methods: area compact retiming and balance logic operation sharing. The area compact retiming used to reduce the transistor counts .the balance logic operation sharing is used to combine the fm0 and Manchester encoding.

II. PRINCIPLES OF FM0 CODE AND MANCHESTER CODE

A .Fm0 encoding

The FM0 having the following three rules.

1) If X is the logic-0,the fm0 code has the transition between the A and B.
2) If X is the logic-1,there is no transition is allowed between the A and B.
3) The transition is allocated in each FM0 code.

The wave form is given below the following diagram.the fm0 having the clock and then the x.the clock and then the cycle having the cycle in each transaction.

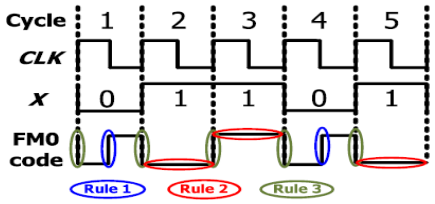

Fig.1.FM0 encoding

B. Manchester encoding

The Manchester encoding is realized with the XOR operation for using the CLOCK and X. The clock always has a transition within the one cycle.

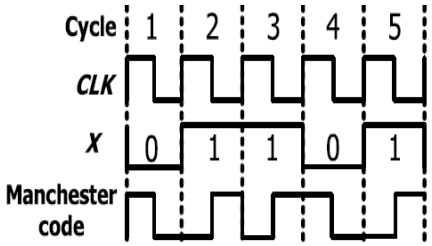

Fig.2. Manchester encoding

III. THE STATE CODE PRINCIPLE FOR FM0/MANCHESTER:

The Manchester encoding is an XOR operation only. The FM0 code starts with the FSM principle. The FSM of FM0 code classified into four states. The four states as shown in the below figure.

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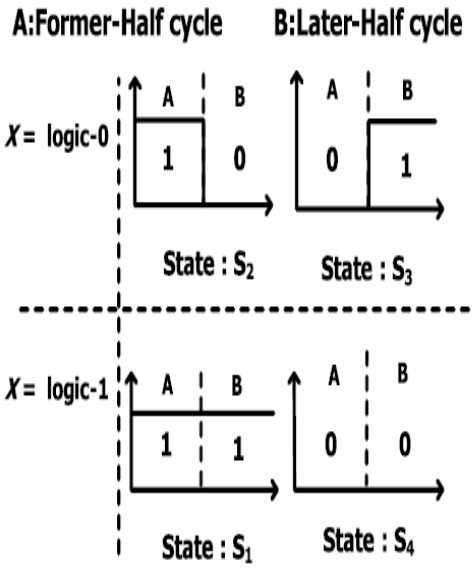

Fig.3.State diagram

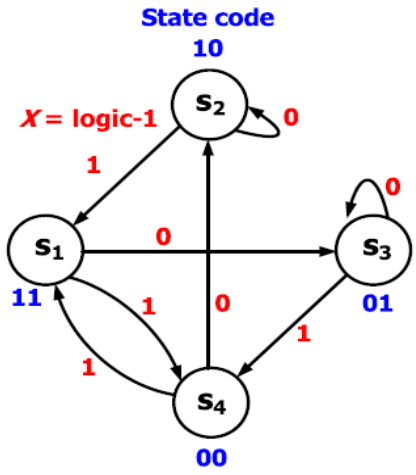

Fig.4.FSM of FM0

Suppose the initial state is S1, and its state code is 11 for A and B, respectively.

1) If the X is logic-0, the state-transition must follow both rules for FM01 and 3. The only one next-state that can satisfy both rules for the X of logic-0 is S3. If the X is logic-1, the state-transition must follow both rules for FM0 2 and 3. The only one next-state that can satisfy both rules for the X of logic-1 is S4. Thus, the state-transition of each state can be completely constructed. The FSM of FM0 can also conduct the transition table of each state A(t) and B(t) represent the discrete-time state code of current-state at time instant t. Their previous-states are denoted as the A(t − 1)and the B(t − 1), respectively. With this transition table, the Boolean functions of A(t) and B(t) are given as

$$A(t) = B(t-1)$$

$$B(t) = X \oplus B(t-1)$$

With both A(t) and B(t), the Boolean function of FM0 code is denoted as

CLK A(t) +~ CLK B(t)

TABLE-1

Previous state		Current state			
A(t-1)	B(t-1)	A(t)		B(t)	
		X=0	X=1	X=0	X=1
1	1	0	0	1	0
1	0	1	1	0	1
0	1	1	0	1	1
0	0	1	1	0	1

IV. HARDWARE ARCHITECTURE OF FM0/MANCHESTER CODE.

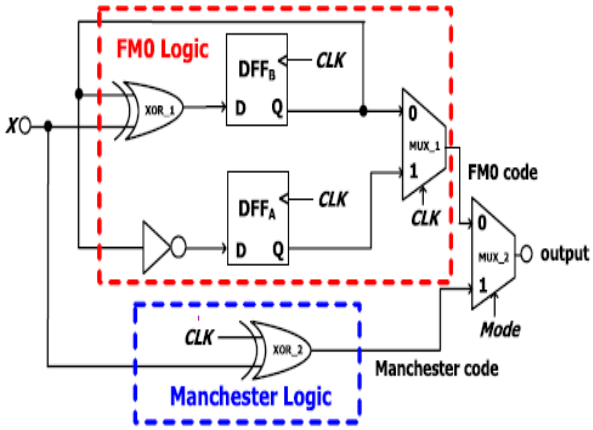

Fig.5.Hardware architecture

This is the hardware architecture of the fm0/Manchester code. the top part is denoted the fm0 code and then the bottom part is denoted as the Manchester code. in fm0 code the DFFA and DFFB are used to store the state code of the fm0 code and also mux_1 and not gate is used in the fm0 code. when the mode=0 is for the fm0 code. the Manchester code is developed only using the XOR gate and when the mode=1 is for the Manchester code. the hardware utilization rate is defined as the following.

$$HUR = \frac{Active\ components}{total\ components} \times 100$$

The active components means the components are work in the both fm0 and Manchester code. The total components means the number of the components are present in the hole circuit. the HUR rate is given below the following section.

TABLE-II

Coding	Active components(transistor count)/ total components (transistor count)	HUR
FM0	6(86)/7(98)	85.71%
MANCHESTER	2(26)/7(98)	28.57%
AVERAGE	4(56)/7(98)	57.14%

For both the encoding methods the total components is 7.for the fm0 code the total component is 7 and then the active component is 6.in Manchester code the total component is 7 the active component is 2.in both coding having 98

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transistors are used without SOLS. The fm0 having 86 transistor, and then the Manchester having the 26 transistor. the average for both coding is 56 transistors .In proposed work reduce the total components from 7 to 6 and reduce the transistor counts. In this paper two multiplexer is used in proposed work reduce two multiplexer from one multiplexer, when reduce the multiplexer the total components are reduced the area and then the power consumption also reduced.

V. FMO AND MANCHESTER ENCODER USING SOLS TECHNIQUE:

The SOLS technique is classified into two parts area compact retiming and balance logic operation sharing

A. *area compact retiming*

For fm0 the state code of the each state is stored into DFFA and DFFB .the transition of the state code is only depends on the previous state of B(t-1) instead of the both A(t-1) and B(t-1)

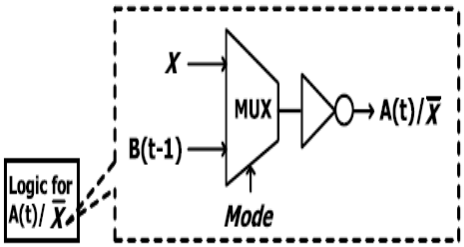

Fig.6.Area compact retiming

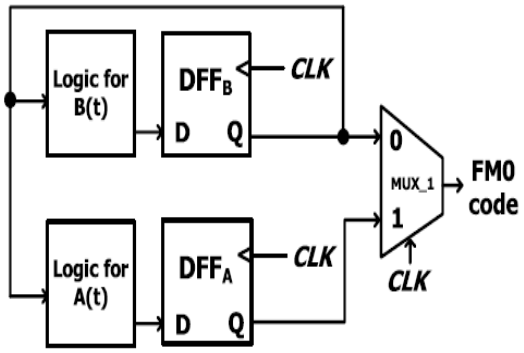

Fig.7.FM0 encoding without area compact retiming.

The previous state is denoted as the A(t-1) and then the B(t-1).and then the current state is denoted as the A(t) and then the B(t)

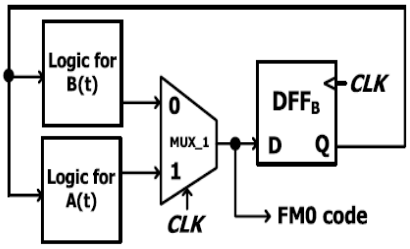

Fig.8.FM0 encoding with area compact retiming.

Thus, the FM0 encoding just requires a single 1-bitflip-flop to store the previous value B(t−1).If the DFFA is directly removed, a non synchronization between A(t) and B(t)causes the logic fault of FM0 code. To avoid this logic-fault, the DFFB is relocated right after the MUX−1, where the DFFB is assumed be positive-edge triggered flip flop. At each cycle, the FM0 code, comprising A and B, is derived from the logic of A(t) and the logic of B(t), respectively. The FM0 code is alternatively switched between A(t) and B(t) through the MUX−1 by the control signal of the CLK. In the Q of DFFB is directly updated from the logic of B(t)with 1-cycle latency. when the CLK is logic-0, the B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. the timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. the B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. the timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. The transistor count of the FM0 encoding architecture without area-compact retiming is 72,and that with area-compact retiming is 50. The area-compact retiming technique reduces 22 transistors.

B.*Bbalance logic operation sharing*

The Manchester encoding is derived using the XOR operation. the equation of the XOR gate is given below.

$$X \oplus CLK = X\ CLK + \sim X\ CLK$$

the concept of balance logic-operation sharing is to integrate the X into A(t) and X into B(t).the fm0 and Manchester logics have a common point of the multiplexer like logic with the selection of the CLK. the diagram for the balance logic operation sharing given the following.

The A(t) can be derived from an inverter of B(t − 1), and X is obtained by an inverter of X. The logic for A(t)/X can share the same inverter, and then a multiplexer is placed before the inverter to switch he operands of B(t − 1) and X. The Mode indicates eitherFM0 or Manchester encoding is adopted. The similar concept can be also applied to the logic for B(t)/X

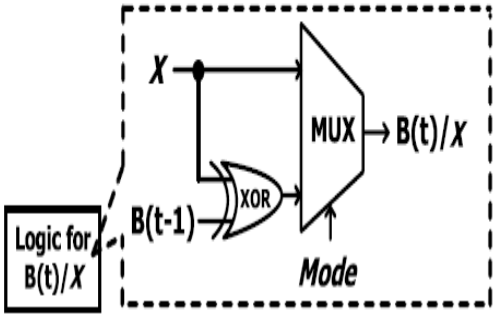

Fig.9.Balance logic operation sharing

Nevertheless, this architecture exhibits a drawback that the XOR is only dedicated for FM0 encoding, and is not shared with Manchester encoding. Therefore, the HUR of this architecture is certainly limited. The X can be also interpreted as the X ⊕0, and thereby the XOR operation can be shared with Manchester and FM0 encodings, where the

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TABLE-III

	2003	**2009**	**2008**	**2009**	**2013**
Coding methods	Manchester	Manchester	Manchester	FM0	Manchester
realization	0.35umμm CMOS	90nm CMOS	Xilinx FPGA Spartan 2	Xilinx FPGA Spartan 2	Xilinx FPGA Spartan 2
Supply voltage	3.3 V	1.2 V	N/A	N/A	N/A
Technique	Gated inverter	CMOS switch	FSM based design	FSM based design	Joint MODEM codec
HUR	N/A	N/A	N/A	N/A	N/A
Operation frequency	1GHZ[1.94GHZ]	5GHZ[2.5GHZ	256.54MHZ	192.64MHZ	612MHZ
Power consumption	N/A	N/A	N/A	N/A	34MW
area	N/A	N/A	N/A	N/A	N/A
Transistor count	54	26	N/A	N/A	N/A
FPGA resource usage	N/A	N/A	Slice:1 Filp flop:2 LUTS:2 Bonded IOBS:3	Slice:5 Filp flop:4 LUTS:10 Bonded IOBS:4	Slice:1 Filp flop:0 LUTS:1 Bonded IOBS:3

multiplexer irresponsible to switch the operands of B(t−1) and logic-0. This architecture shares the XOR for both B(t) and X, and there by increases the HUR. When the FM0 code is adopted, the CLR is disabled, and the B(t −1) can be derived from DFFB .Hence, the multiplexer can be totally saved, and its function can be completely integrated into the relocated DFF. The logic for A(t)/X includes the MUX−2 and an inverter. Instead ,the logic for B(t)/X just incorporates a XOR gate. In the logic for A(t)/X, the computation time of MUX−2is almost identical to that of XOR in the logic for B(t)/X. However, the logic for A(t)/X further incorporates an inverter in the series of MUX−2. This unbalance computation time between A(t)/X and B(t)/X results in the glitch to MUX−1,possibly causing the logic-fault on coding. To alleviate this unbalance computation time, the architecture of the balance computation time between A(t)/X and B(t)/X The XOR in the logic for B(t)/X is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for A(t)/X. This shared inverter is relocated backward to the output of MUX−1. Thus, the logic computation time between A(t)/X and B(t)/X is more balance to each other. The adoption of FM0 or Manchester code depends on Mode and CLR. In addition, the CLR further has another individual function of a hardware initialization. If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization. To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design froma system controller. Whether FM0 or Manchester code is adopted, no logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed VLSI architecture is greatly improved

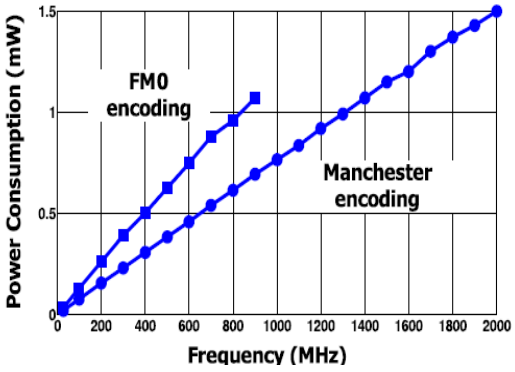

Fig.10.power for FM0 and Manchester

VI. CONCLUSION

The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FM0 and Manchester encodings is discussed in detail. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The area-compact retiming relocates the hardware resource to reduce the transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester encodings with the identical logic components. This paper is realized in 180nm technology with an outstanding device efficiency. The power consumption is 29392.843nW for Manchester encoding and FM0 encoding.

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VII. REFERENCE

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