VHDL Implementation of Alamouti Space Time Block Coded (STBC) MIMO encoder and decoder on FPGA

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***Abstract* — Realization of multi input and multi output (MIMO) systems is highly essential for Wimax networks. In wireless communications the transmitted signal must traverse a potentially difficult environment with scattering, reflection, refraction and so on and may then be further corrupted by thermal noise. In the receiver STBC redundancy results in a higher chance of being able to use one or more of the received copies to correctly decode the received signal. The space time coding combines all the copies of the received signal in an optimal way to extract as much information from each of them as possible. In this project a computationally efficient algorithm for space time block decoding will be implemented for FPGA based applications. The VHDL will be used for realization of the decoding algorithm and other communication blocks. The decoding algorithm will be computationally efficient extension of the maximum likelihood algorithm. The new algorithm results in more than 50% reduction in the computational complexity. The STBC encoder will also be realized which generates the required appropriate codes for decoder to validate the complete design.**

***Index Terms* —** *FPGA Spartan3E, MIMO, ML Decoder, STBC Encoder, VHDL.*

I. INTRODUCTION

In radio, multiple-input and multiple-output, or MIMO is the use of multiple antennas at both the transmitter and receiver to improve communication performance. It is one of several forms of smart antenna technology. Note that the terms input and output refer to the radio channel carrying the signal, not to the devices having antennas. MIMO technology has attracted attention in wireless communications, because it offers significant increases in data throughput and link range without additional bandwidth or transmit power. It achieves this by higher spectral efficiency (more bits per second per hertz of bandwidth) and link reliability or diversity (reduced fading) [1]-[3].

MIMO can be sub-divided into three main categories,

1. Precoding
2. Spatial multiplexing or SM, and
3. Diversity coding.

Spatial multiplexing requires multiple-input and multiple-output (MIMO) antenna configuration. In spatial multiplexing, a high rate signal is split into multiple lower rate streams and each stream is transmitted from a different transmit antenna in the same frequency channel. If these signals arrive at the receiver antenna array with sufficiently different spatial signatures, the receiver can separate these streams into parallel channels. Spatial multiplexing is a very powerful technique for increasing channel capacity at higher signal-to-noise ratios. The maximum number of spatial streams is limited by the lesser in the number of antennas at the transmitter or receiver. Spatial multiplexing can be used with or without transmit channel knowledge. Spatial multiplexing can also be used for simultaneous transmission to multiple receivers, known as space-division multiple access. By scheduling receivers with different spatial signatures, good reliability can be assured.

It is a technique used in wireless communications to transmit multiple copies of a data stream across a number of antennas and to exploit the various received versions of the data to improve the reliability of data-transfer. The fact that transmitted data must traverse a potentially difficult environment with scattering, reflection, refraction and so on and, as well as, be corrupted by thermal noise in the receiver means that some of the received copies of the data will be "better" than others. This redundancy results in a higher chance of being able to use one or more of the received copies of the data to correctly decode the received signal. In fact, STBC combines all the copies of the received signals in an optimal way to extract as much information from each of them as possible.

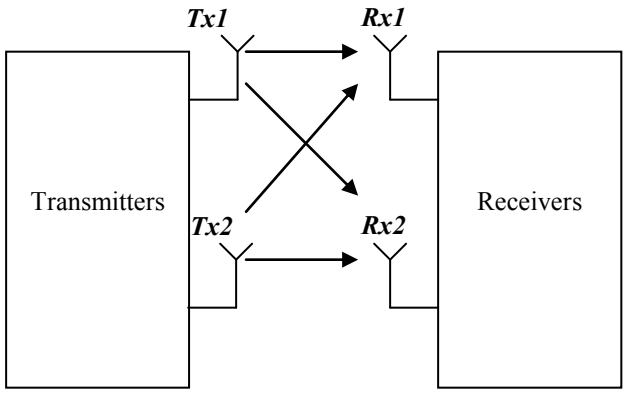

Fig 1. 2x2 MIMO basic system model

The MIMO refer to Multi-Input-Multi-Output (MIMO) antenna system. In this case we are using 2x2 MIMO system. One possible way to improve the reliability of wireless communications is to employ diversity. Diversity is the technique of transmitting the same information across multiple channels to achieve higher reliability. MIMO systems are able to achieve impressive improvements in reliability and capacity by exploiting the diversity offered by the multiple channels between the transmit and receive antennas. Fig 1. shows 2×2 MIMO system, there is the potential for both transmit and receive diversity.

II. BRIEF EXPLANATION

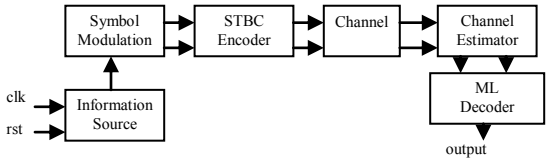

Fig 2.Block Diagram of the proposed design

In the proposed design, STBC transmission blocks are also designed to validate the complete STBC Implementation. Thus, the design consists of STBC Transmitter blocks and Receiver blocks as shown in Fig 2. Transmitter consists of Symbol modulator and Encoder blocks; Receiver consists of Channel Estimator and Maximum Likelihood Decoder as the main blocks.

In a classical one-transmitter system, symbols S_0 , S_1 , S_2 , ... are transmitted at time intervals t, t+T, t+2T, ... respectively. In a two transmitter Alamouti encoder scheme however, the symbols S_0 and S_1 are transmitted simultaneously from two transmit antennas Tx_1 and Tx_2 respectively, at time interval t. At time interval t+ T, Tx_1 transmits symbol $-S_1^*$ and Tx2 transmits symbol S_0^*.

The transmitter based on Alamouti encoder contains sequential logic and thus requires some control logic and a clock signal. At any symbol period two input bits are modulated by two BPSK modulators [4]. This outputs the real and imaginary components and these are inserted to the Alamouti encoder which encodes the symbols. The only operation that the Alamouti encoder performs on modulated symbols is the negation of either the real or imaginary part of a symbol . System clock is used to ensure that all signals are latched at the correct instant of time. It is designed to operate at the same clock speed as the data rate of the system, so one clock cycle is assumed to be one symbol period.

The combiner complexity and ML detector complexity depends on type of modulation. Binary phase shift keyed (BPSK) symbols are the simplest to detect. Detection of non equal energy modulation scheme requires channel estimates in the ML detector and has higher complexity. The present work considers BPSK implementation only [8]-[9].

III. PROPOSED DESIGN

At a given symbol period, two signals are simultaneously transmitted from the two antennas. The signal transmitted from antenna zero is denoted by S_0 and from antenna one by S_1 . During the next symbol period signal ($-S_1^*$) is transmitted from antenna zero, and signal S_0^* is transmitted from antenna one. where * represents the complex conjugate.The remaining symboles are transmitted from Tx_1 and Tx_2 in same manner as given in the Table 1.

Table 1.Symbols transmission in different time slots

	Time intervals			
	t	***t+2T***	***t+3T***	***t+4T***
Tx_1	S_0	$-S_1^*$	S_2	$-S_3^*$
Tx_2	S_1	S_0^*	S_3	S_2^*

At the input of the channel estimator, the received signals are given by

$$r_{00} = r(t) = h_0 s_0 + h_1 s_1 \quad (1)$$
$$r_{10} = r(t) = h_2 s_0 + h_3 s_1 \quad (2)$$
$$r_{01} = r(t+T) = -h_0 s_1^* + h_1 s_0^* \quad (3)$$
$$r_{11} = r(t+T) = -h_2 s_1^* + h_3 s_0^* \quad (4)$$

At the receiver section, a real-time FPGA based channel estimator produces the estimates h_0 and h_1 and this information is fed to the combiner to yield two combined output signals $\sim S_0$ and $\sim S_1$. The signals $\sim S_0$ and $\sim S_1$ are sent to the maximum likelihood (ML) detector so that ML estimates $\sim S_0$ and $\sim S_1$ can be made of S_0 and S_1 [5]-[7].

Implementation of a MIMO 2 transmitter and 2 receiver Alamouti system, requires the estimation of 4 channels (h_0, h_1, h_2 and h_3). In this situation, the output of combiner yields 2 outputs

$$\sim S_0 = h_0^* r_{00} + h_1 r_{01}^* + h_2^* r_{10} + h_3 r_{11}^* \quad (5)$$
$$\sim S_1 = h_1^* r_{00} - h_2 r_{11}^* + h_3^* r_{10} - h_3 r_{01}^* \quad (6)$$

where h_0 and h_1, h_2 and h_3 are channel estimates from the first and second receivers respectively. In the case of a 2 × 2 Alamouti implementation using PSK signals, the ML decoder remains unchanged except for the combiner. As seen from (4), the combiner output $\sim S_0$ is actually the sum of $\sim S_0$ from receiver 0 and $\sim S_0$ from receiver 1. Likewise, $\sim S_1$ is actually the sum of $\sim S_1$ from receiver 0 and $\sim S_1$ from receiver 1. Thus a 2 × 2 Alamouti implementation can be easily implemented by summing together the appropriate combiner outputs from 2 receivers before feeding one ML detector.

ML Decoder decides final output based on the maximum likelihood detection. ML Decoder receives approximated symbols ($\sim S_0$ and $\sim S_1$) data from combiners and gives the final data (S_0 and S_1).

The complete design is implemented using a top down hierarchical schematic entry approach on the Xilinx Integrated System Enviroment (ISE) Foundation design tool. VHDL code can also be integrated as a block with other schematic components if desired. We have also made extensive use of various Xilinx Core Generator intellectual property(IP) modules incorporated within the ISE Foundation toolset to shorten design cycle time.

IV. RESULTS AND DISCUSSION

RTL schematic for the complete logic is given in the Fig 3.

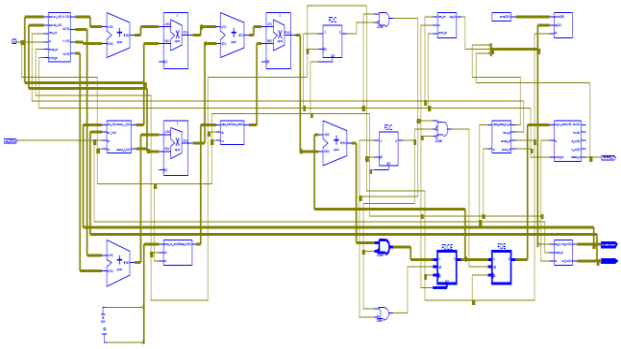

Fig 3.RTL schematic of the complete design

Simulation results of the proposed design are given in the Fig 4 below. The first waveform is the main clock used in the complete logic. The second waveform shows input data bits come from input data generator module. The next two waveforms are antenna0 and antenna1 outputs transmitted through channel. The fifth and sixth waves are inputs received at the receiver. Seventh and eighth waveforms are equalized outputs at the receiver side. The ninth waveform is the final detected output from the Maximum Likelihood Decoder.

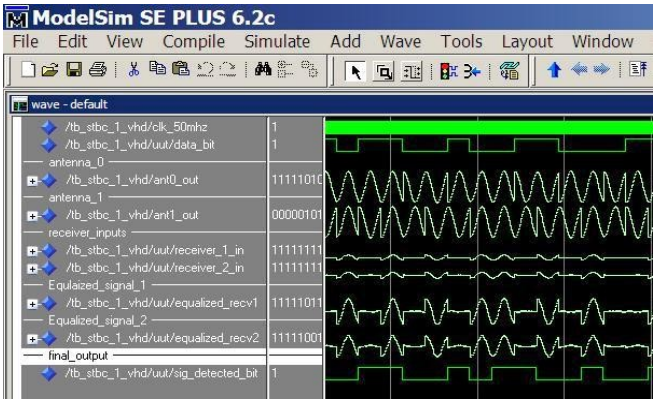

Fig 4.Simulation results of the top level design

STBC Encoder at the transmitter part will encode the data for antenna_0 and antenna_1.The results are shown in below Fig 5.

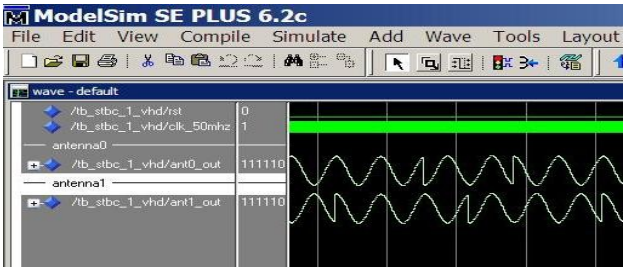

Fig 5.STBC Encoder outputs for two antennas

ML Decoder at the receiver part will decode the reliable data from data collected through receiving antennas.

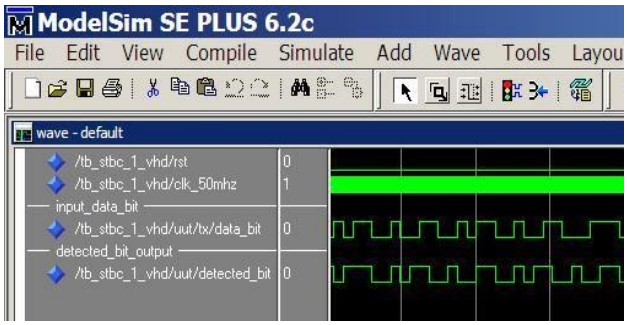

Fig 6.ML Decoder output results

Chipscope software is used to verify the hardware signals running in FPGA after programming.

The final Chipscope results are:

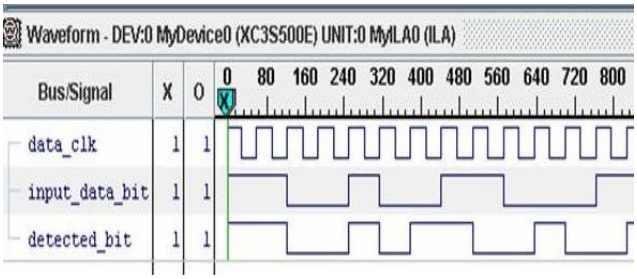

Fig 7.Chipscope results for final design

The hardware used is Spartan 3E FPGA. Device utilization for the complete logic is given in the Table 2.

Table 2.Device Utilization for Spartan 3E FPGA

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Slice Registers	2130	4656	45%
4 input LUT's	1630	9312	17%
Slice FF's	3612	9312	38%
IOB's	23	232	9%

Timing Report of the complete logic (Speed Grade: -5) is given below:

Minimum period: 24.222ns
Maximum Frequency: 41.286MHz
Minimum input arrival time before clock: 3.812ns
Maximum output required time after clock: 9.087ns
Maximum combinational path delay: 2.655ns

V. CONCLUSIONS

In this project Alamouti STBC transmission is shown to be in upper bound for transmitting data through communication channel with respect to combating fading and transmission loss. The STBC encoding allows us to get Space wise (by multi transmitting antennas) and Time wise (corresponding to different transmitting times) encoding of blocks of data to be transmitted, by which reliability of data transmission is provided. At the receiver part, ML Decoder gives the reliable data by collecting channel estimated parameters and received signals. In MIMO with STBC when selecting the number of transmit/receive antennas, several practical considerations must be taken into account as under strict delay constraints, achieving high diversity gains (i.e. high reliability) becomes critical in order to minimize the need for retransmissions. Since transmit/receive diversity gains experience diminishing returns as their numbers increase, complexity considerations dictate the use of small antenna arrays (typically no more than 4 antennas at each end).

VI. REFERENCES

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