

Leakage Diminution of Adder through Novel Ultra Power Gating Technique

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Abstract: Technology scaling helps us to exhibit more functionality per area or we can say package density, low switching power and higher speed as well as it also increases the Leakage power tremendously. Leakage power dissipation in the IC increases exponentially with technology continuously scaling down. Although Multi threshold Power gating schemes is very useful to reduce the Leakage current in the circuit by using high threshold sleep transistor. There exists an extensive body of research that aims at obtaining lifetime as well as leakage reduction of circuit for the cost of the area. In this research paper we proposed power gating technique Ultra Low Power (ULP) Diode with body biasing, is handling to solve the problem of leakage with the variation of body biasing.

Keywords ; ULP(Ultra low power gating technique), Leakage Reduction, MTCMOS technique, Low Power

I. INTRODUCTION

Benefits of CMOS technology scaling in the nanometer region comes with consequences of increasing MOS transistor leakage current. Leakage current affects not only the standby leakage current and active power of a CMOS system but also circuit reliability since leakage current is strongly related to process variations. A drastic increase in transistor leakage current is the primary disadvantage of technology scaling. There are several different techniques that can be used to handle the leakage from various angles. Power gating is one of the very popular technique to reduce leakage current. Power gating scheme uses large transistors, called sleep transistors, in series with the pull up and pull down stacks to cut off the power supply rail from the circuit when the circuit is in standby mode. With technology scaling the power density of ICs is also increasing due to leakage. This also motivates a circuit designer to develop new techniques to deal with the problem. To solve the leakage problem, power gating is widely implemented to suppress the standby leakage current.

Power gating is a very simple technique : a circuit is cut off from its power supply in sleep mode by means of a current switch These include retaining data by isolating outputs and the use of retention flip-flops, the design and sizing of current switches, rush current, and ground bounce during the wake-up process, and questions of physical design, with their impact on area and wire length, as well as power network analysis. Power gating has to be considered during the early stage of design, including architectural design.

In this work we calculate the numerical simulation through the ULP gating technique . our calculation is to compare the numerical analysis of leakage current at several possible value of bogy biasing with fixed supply voltage.

II. POWER GATING TECHNIQUE

Power gating refers to cutting off, or gating a circuit from its power supply rails (V_{dd} and/or V_{ss}) during standby mode. Power gating is a commonly used low-power design technique that is very effective in reducing power of a circuit during standby mode. Power gating exploits the multi threshold voltage technology by using high-speed low threshold voltage devices for the logic cells to achieve high performance during active mode, and high threshold voltage sleep devices to suppress the leakage currents during standby mode.

The most natural way to reduce the leakage power dissipation of a VLSI circuit in the standby mode is to turn off its supply voltage. This can be done by using one PMOS transistor and one NMOS transistor in series with the transistors of each logic block to create a virtual ground and a virtual power supply as depicted in Figure 1.

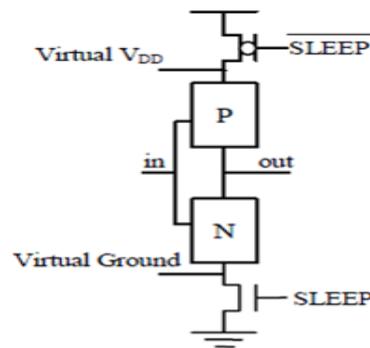


Figure 1 Power Gating Technique

In the active state, the sleep transistor is on therefore the circuit functions as usual. In the standby state, the transistor is off, which disconnects the gate from the ground. Note that to lower the standby leakage, the threshold voltage of the sleep transistor must be higher. Otherwise, the sleep transistor will have a high leakage current, which will reduce the effectiveness of power gating.

III. ULTRA LOW POWER DIODE BASED TECHNIQUE

Here high threshold transistor are N1,N2,P2 and high threshold transistor N2 and P2 are used as ultra low power diode, which reduces leakage more effectively. The ultra low power diode improves speed of the circuit when forward body bias voltage is applied on PMOS P2 transistor in active mode and leakage reduced by using reverse body biasing on P2 transistor. The ULP diode reduces the leakage current strongly in compare to simple diode connected technique and the current driving capacity of it is similar to simple diode connected technique. The basic design of the ultra low power diode is shown in Figure 2.

In CMOS by connecting the drain to gate can be used as standard diode. When diode is reverse bias, it appears that source is directly connected to gate. The reverse leakage current is directly related to CMOS drain current at zero gate to source voltage. This increases exponentially for lower threshold voltage. This leakage current can be reduced by using more heavily doped transistor with higher threshold voltage but it reduces the current driving capability in forward biasing mode. So ultra low power diode is a very effective way to reduce leakage current more effectively. When diode is reverse bias both P2 and N2 operates with negative V_{gs} voltage which leads to strong reduction of leakage current in comparison to standard diode. When diode reverse bias voltage increase the current increase due to increase in V_{ds} . The current reaches to peak value and then strongly decreases with V_{gs} of transistor becoming more and more negative.

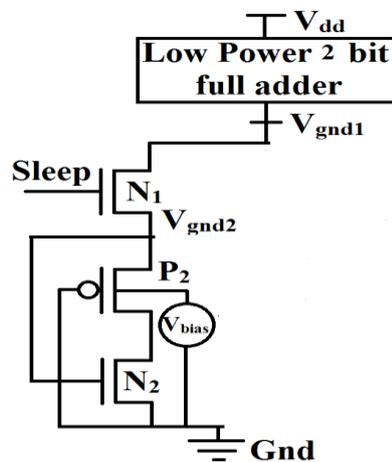


Figure 2 Ultra low power diode based MTCMOS technique with body biasing

By using reverse body bias the threshold voltage of the transistor increases so leakage current reduces effectively to a considerable amount.

IV SIMULATION RESULT

The simulation result of Table 1, represents the comparison between ULP gating technique and non gated techniques, when applying the reverse body biasing on the PMOS power gated transistor in diode based and ULP power gating techniques, the leakage current reduces more effectively.

Table 1 Simulation Result of non gated vs ULP Power gating technique

V_{dd} (V)	Avg. Leakage Current (nano amp.)		Comparative leakage reduction (in %)
	ULP gating Technique	without gating technique	
1.4v	0.213	6.07	96.49%
1.2v	0.231	3.89	94.06%
1v	0.227	2.52	91.15%

The wave form of leakage current shown in figure 3

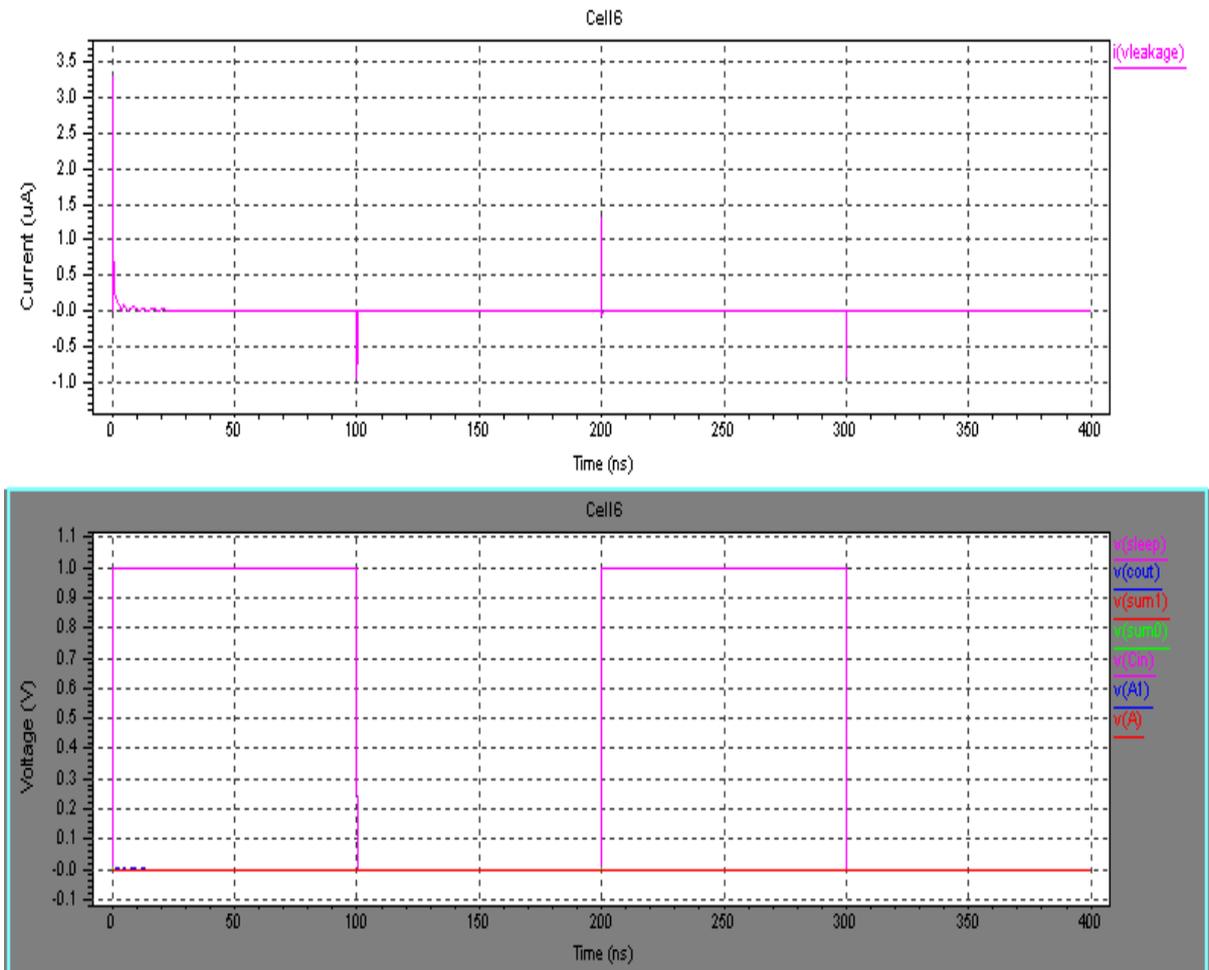


Figure 3 Wave form of leakage current analysis of multi adder (ULP Diode based gating technique)

V CONCLUSION

Leakage current the ULP diode based multimode MTCMOS technique shows the best result over conventional technique by reducing the leakage current by max. 96.47% when V_{dd} is 1.4 v. Study concluded that MTCMOS technique reduces standby leakage current. That also brought to picture that temperature increase did not affect the magnitude of delay significantly but standby leakage current increases at considerable amount as temperature.

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