Analysis of 8T SRAM with Read and Write Assist Schemes (UDVS) In 45nm CMOS Technology

Srikanth Lade[1], Pradeep Kumar Urity[2]

***Abstract*: UDVS techniques are presented in this paper to minimize the power consumption. Designing memories with dynamic voltage scaling (DVS) capability is important since significant active as well as leakage powers can be reduced by voltage scaling. Ultra dynamic voltage scaling is to scale the supply voltage by using assists circuits for different modes of the cell operation. Write assist circuits are designed to improve the write margin of the SRAM cell. In this paper three write assist circuits and two read assists circuits have been designed. First one is Capacitive W-AC approach to reduce the level of cell supply voltage accordingly when word line is enabled so as to make power reduction. Second scheme is Transient Negative Bit-line Voltage write assist scheme performs write operation without using any on-chip or off-chip voltage sources. Read assist circuits are designed for basic cell of SRAM to read the data from the cell without altering the cell data with low power consumption and high data transfer speed. Reconfigurable assist circuits provide the necessary adaptability for circuits to adjust themselves to the requirements of the voltage range that they are operating in. In this paper finally implemented 8T SRAM cell with efficient data transfer with high speed with less power consumption in 45nm with UDVS Technique in which supply voltage could be changed for different modes of operation of SRAM Cell.**

***Keywords* - UDVS, Tran-NBL, Capacitive W-AC**

I. INTRODUCTION

Static Random Access Memory (SRAM) comes under classification of volatile memory. In recent years high speed and low-power circuit design gaining more importance in research area. Since tremendous development in VLSI technologies, the designing of high speed and low power devices such as portable electronic gadgets is most working field in industry.

So energy saving is a key point in designing the electronic circuits. So Ultra Dynamic Voltage Scaling (UDVS) technique is an approach to reduce energy consumption by adjusting the system supply voltage over a wide range depending on the performance of operation requirement. UDVS is required for systems with time-varying constraints like output voltage or frequency. In modern ICs, caches are occupying more area in designing on-chip memories. So, on chip memories consequently cause more energy consumption. For the U-DVS techniques mentioned above, it is required to have the on chip memories are capable of operating on a wide voltage range. An SRAM designed for operation in sub-threshold presented in this paper.

This paper first discusses voltage scaling and design issues, operation of basic SRAM cell and write assists schemes.

II. Operation of SRAM cell

Modes of the cell are

2.1 Write mode.(supply should less or bit-line should negative)
2.2 Read mode.(cell supply voltage should high)
2.3 Standby mode.(stability should high)

2.1 Write mode

Writing the data in to the cell leads to latching in the cell. This latching occurs based on threshold levels of both inverters connected in back to back so as to store the data. For easy write operations there are so many write assist schemes to have low power consumption.

2.1.1 Write Driver Circuit

In order to read the write driver circuit drives the appropriate data values onto the bit line true and compliment lines. Since the primary objective data from an SRAM, the Data must write into memory first. The four vertical devices in series are often referred to as a gated inverter. When write enable is asserted high is to drive a "0", the NFETs and PFETs may be similarly sized, rather than the typical two to one ratio. Write circuitry and its waveforms are shown in "Fig1"and "Fig2" respectively.

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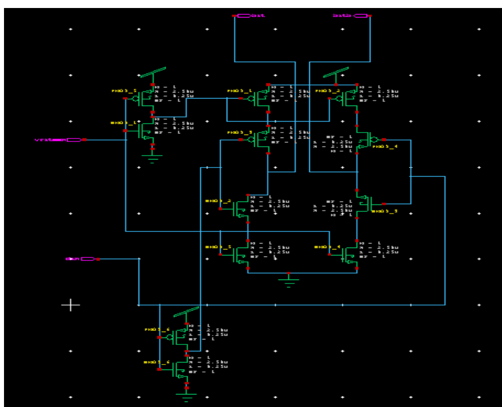

Fig. 1 Write driver circuit

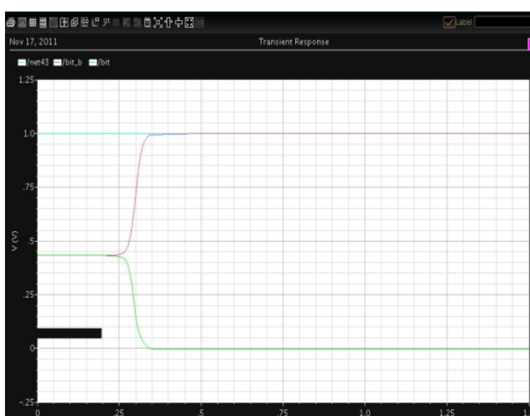

Fig. 2 Waveform of Writedriver circuit

2.1.2 Write assist schemes

Control of process parameter becomes extremely difficult by Scaling supply voltage and sizing of transistors. So every time scaling the supply voltage manually is not benefit to achieve low power requirement but write circuit writes the data into SRAM cell when strength of the cell stored data is less than that of write data. For that cell supply voltage should less than that of write circuitry supply voltage. Write assist circuits can solve this problem. In this paper three write assist schemes have been used to make write data to be written in to the cell.

2.1.2.1 Capacitive W-AC (capacitive write assist scheme)
2.1.2.2 Transient-NBL (transient-negative bit line scheme)
2.1.2.3 NBL scheme on the source of the write circuit

2.1.2.1 Capacitive W-AC (Capacitive Write Assist Scheme)

In this scheme data can be written with high WM by changing the strength of the cell. Cell supply is scaled by using column write assist circuit so as to reduce the cell stability. Lowering the SRAM cell voltage supply reduces the current to the pull-up PMOS device. As result, this assists the SRAM's write operation. In this approach the bit-cell supply is lowered below the word line level by capacitive charge sharing scheme.

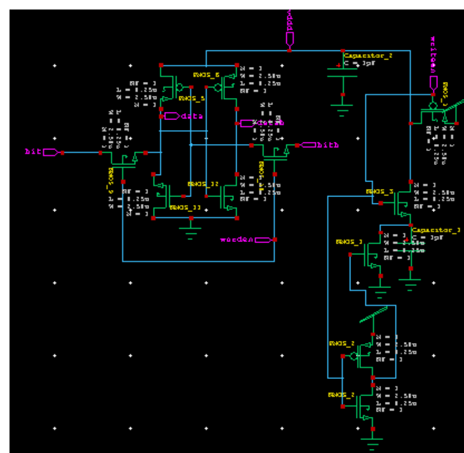

Fig. 3 capacitive W-AC circuit

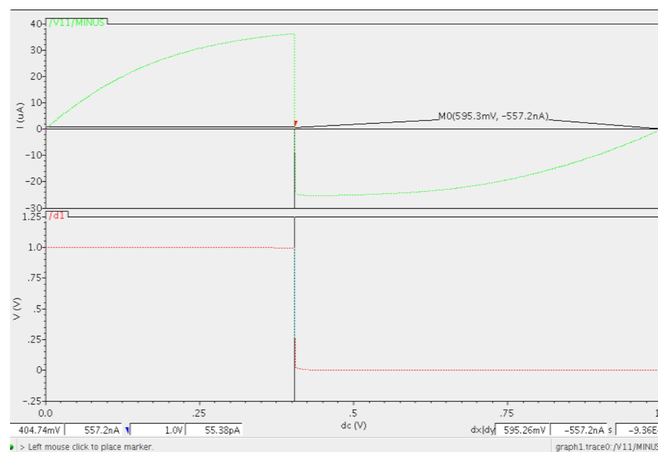

Fig. 4 Waveforms of Capacitive W-AC circuit

Here by DC analysis is done to get N-Curves shown in "Fig 4" when word line is high. Capacitive WA scheme is used to scale supply to reduce cell stability.

2.1.2.2 Transient-NBL (transient-negative bit line scheme) write circuitry

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This is the second write assist scheme to make very easy write operation. Main aim of scheme is undershooting bit line to provide negative source voltage to access transistor so as to provide high channel width to write the data early means WM can be improved.

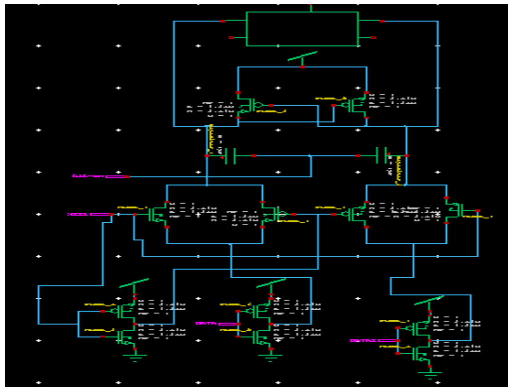

Fig .5 Transient-NBL write circuit

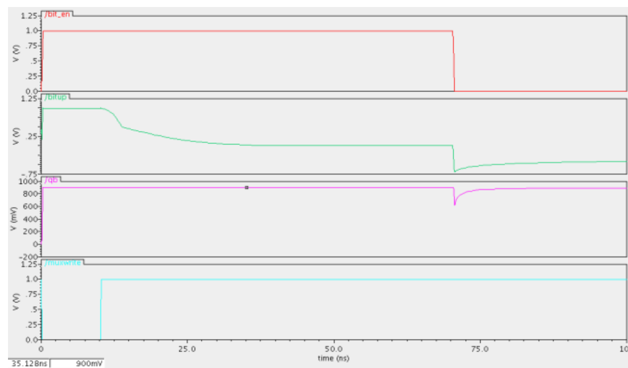

Fig. 6 For Cell supply voltage is 900mV

From "Fig 6" data can be driven into the cell is 1 when NBL driver circuitry make bit line is negative. In this transient negative bit line scheme write operation is performed by increasing the strength of SRAM pass transistor. When supply voltage of the cell is 900mV so that strength of the stored data is more than write data. So for 0 is written when Bit-en low and cell is not able to latch. So cell strength has been reduced to latch the state of the cell.

2.1.2.3 NBL scheme on the source of the write circuit

In this scheme write of data is performed by negative the bit line as before but difference of this scheme is applied the negative bit-line voltage on source of the driver circuitry instead of using coupling operation inside the driver circuitry.

Fig. 7 Source coupled NBL write circuit

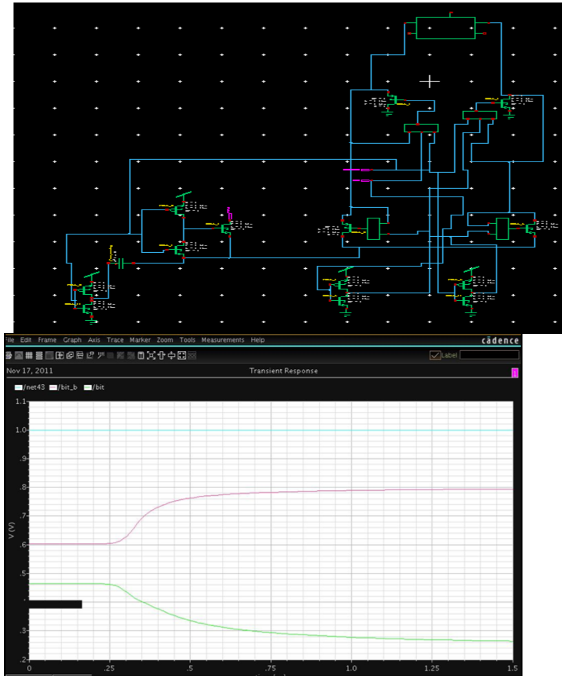

Fig. 8 waveform of source coupled NBL write circuit

From above "Fig 8" data can be driven into cell is 1using NBL driver circuitry.

2.2 Read Assist Schemes

To enhance both stability and performance of SRAM cell, it is important that the Bit line capacitive loading should be as low as possible. In this section we analyze a new read-assist scheme for cell that will nullify the drawbacks of local sense amplifier. The proposed schemes improves the performance of sensing circuitry by amplifying the BL voltage drop and while reducing the BL voltage swing which results in significant power reduction. Reduction in cell VDD with respect to the original scheme causes reduction in leakage power dissipation. These problems can be overcome by following Read assists schemes.

2. 2.1 Proposed Read Assist scheme for 6-T SRAM Cell

Here while performing write operation to cell write driver circuitry is needed along with to perform read operation following read equipment is needed

a. Sense amplifiers
b. Isolation circuitry
c. Pre-charge circuitry
d. SRAM Cell

Operation: while performing read operation first isolation circuitry going to isolate sense amplifier then pre-charge circuitry pre-charge the bit-line so

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as to produce potential error to sense data using sense amplifier.

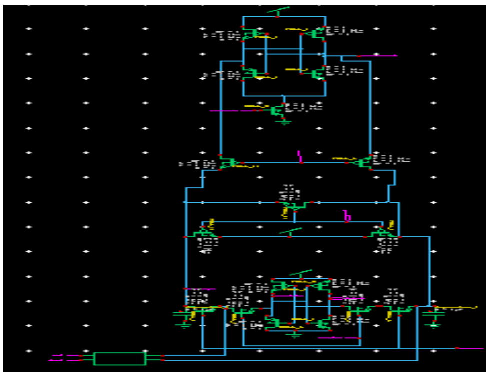

Fig. 9 Read assists Scheme with 6-T

2.2.2 8-T cell with all peripheral circuitry to write and read totally

Here UDVS Technique is used to make read and write operation on cell with less power consumption. UDVS (Ultra Dynamic Voltage Scaling) Technique is used by which cell stability can be adjusted according to the cell operation so that power dissipation can be very low.

Here N,P Sense amplifiers are used to improve speed of operation by reducing sensing delay. So Speed and power consumption requirement for any system can be achieved using this read assist scheme.

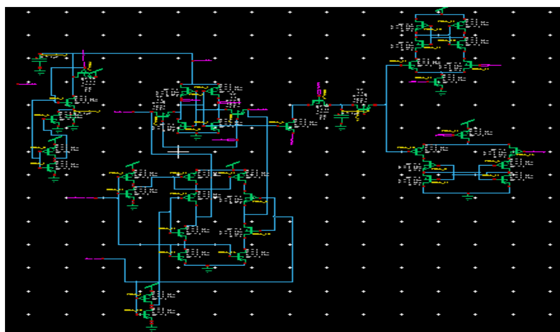

Fig. 10 Read assist Scheme with 8-T

Fig.11 waveforms of Read assist Sccheme

Here Data which is stored in SRAM cell can be sensed using P,N Sense amplifiers after pre-charge operation is performed which is shown in "Fig 11".

2.3 Standby Mode

Here write enable line should be zero. So two transistors in 6T SRAM cell are in off condition. Current is generally flowing between supplies to ground. We designed circuit to reduce leakage current and is designed in 45nm technology with sub-threshold voltage of 0.7V. Until and unless threshold voltage is 0.7V transistor is not switched ON.

III. Layouts

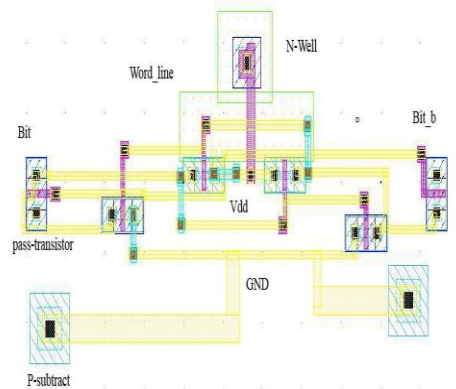

Fig. 12 Layout of 6T SRAM cell

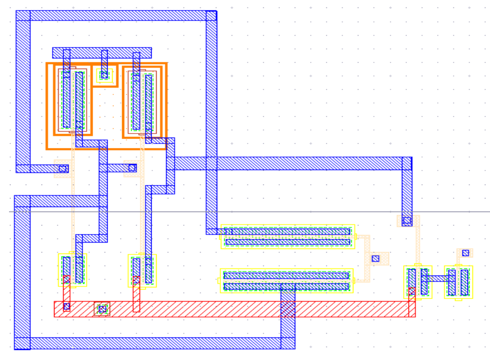

Fig 13. layout of 8T SRAM cell

IV. Results

4.1 Power Calculations for 6-T SRAM Cell

The delay and power calculations are done on this schematic 6-T SRAM cell

4.1.1 Calculation of delay

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Write to bit b =52.33ps
Write to bit = 26.33ps

I. Calculation of power

Condition	Power in watts
Initial	37.84×10^{-15}
Write -“1”logic	123.5×10^{-15}
Read-“1” logic	32.3×10^{-15}
Write-“0” logic	118.4×10^{-15}
Read-“0”logic	32.8×10^{-15}

From above “Table 1” it is clear that power consumed by SRAM cell in write operation is more when compared to read operation.

4.2 Delay and leakage currents for 8-T SRAM cell are calculated. Cell is sized according to better write and read margins.

4.2.1 Delay calculations

Write in to bit-line=42.02ps.
Write into bit-line-bar=35.4ps.

4.2.2 Calculation of currents

I read=60.2 u A
I leakage=57.4 pA.

Here leakage power of the cell= $I_{leakage}$ x supply voltage (in standby mode)
=3.21 x 1
=3.21 uW.

II. Calculation of power

Conditions	Power (watts×10^{-15})
Write Logic-1	102.2
Write Logic-0	92.3
Read Logic-1	52.3
Read Logic-0	42.9

From above “Table2” we can conclude that power consumed by SRAM cell for write operation is more than read operation. So I use write assist schemes to reduce the power consumption because we are designing low power SRAM so power consumption should less.

III. Calculation of power dissipation

Name of the write assist scheme	Write margin(WM)	
	Write trip voltage	write trip current
Capacitive W-AC	0.69V	5.8uA
Transient-NBL	0.62V	3.1uA

4.2.5 Write margin calculations

Write margin defines how fast the data is going to write and read margin is defined to know how fast the data is reading from the cell.

IV. Write margin

Supply voltage of the cell	Power dissipation(pW)
1 V	50.4
0.5 V	52.9

These values are calculated by using N-curves of the cell drawn by varying one node voltage from 0 to supply voltage and by doing DC analysis.

V. CONCLUSION

In this paper, the 4T transistor back to back connected two inverter along with two access transistors cell a is designed with proper sizing accordingly to the best write, read margins and best system noise margins. Power consumed by write driver circuit to write the data is more with compared with power consumed by read sense amplifier. By using UDVS technique and different write assist circuitry how fast data is going to write logic values in to the cell is calculated by using WM and power consumed also has been reduced. Comparison is done between different schemes with parameter WM. Read operation is performed by different read assist circuits to improve power management. 8T cell is designed with high stability and high SNM with Data retention voltage around 0.6V.

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