Implementation of Linear Frequency Modulation signal generation using Multi DDS Technology on FPGA

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Abstract—Direct Digital Synthesizer (DDS) is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Radar Wave form generation is a prime challenge in digital radar Transmitter, with the demand on the performance and functionality of digital radar transmitter increases highly, it is particularly necessary to develop high-efficient up-conversion technology for generation of Linear Frequency Modulated signal using Multi-DDS Technology. Radar is an object detection system which uses radio waves to determine the range, altitude, direction, or speed of objects. Digital Up-conversion is the core technology in digital radar transmitter. To achieve high sampling rate, we have to use high clock frequency hence a high hardware clock is required. In this paper we are using the Multi-DDS (10 DDS) technology which is based on parallel processing, a large bandwidth signal can be produced at conditions of a lower hardware clock. This output signal is used to generate the Radar signal with high sampling rate (200 MHz). Similarly Multi-DDS technology gives a high-efficient solution. With this by using lower hardware clock high sampling rate can be achieved. As this paper presents the results based on a system (i.e. Virtex5 FPGA) whose clock frequency is 200MHz.

Index Terms—Digital up-conversion; high-efficient; parallel processing; Linear Frequency Modulation; Multi-DDS Technology.

I. INTRODUCTION

Depending on its flexibility, small size and low development costs, digital radar transmitter is widely used in the field of radar signal processing. But with the Traditional digital up conversion process is used to achieve high sampling rate, we have to use high clock frequency hence high hardware clock is required. With this Multi-DDS (10 DDS) technology a lower hardware clock and high sampling rate can be achieved. As this paper presents the results based on a system (i.e. Virtex5 FPGA) whose clock frequency is 200MHz.

The above figure shows generic DDS which is a combination of n DDS modules. According to this paper for getting 200MHz sampling rate 10 DDS are suffice. With this we are generating the radar signal and finally got the radar signal with high sampling rate.

II. SINGLE DDS UNIT

A digitally-controlled method of generating multiple frequencies from a reference frequency source has evolved called Direct Digital Synthesis (DDS). The NCO main purpose is to generate the carrier signals (cosine). The main advantage is ROM based techniques will be used for area optimization.
A numerically controlled oscillator (NCO) is a digital signal generator which creates a synchronous, discrete-time, discrete valued representation of a waveform. NCOs are often used in conjunction with a Digital-to-analog converter (DAC) at the output to create a direct digital synthesizer (DDS). Applications of DDS include: signal generation, local oscillators in communication systems, function generators, mixers, modulators, sound synthesizers and as part of a digital phase-locked loop.

A basic Direct Digital Synthesizer consists of a frequency reference, a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC).

The reference provides a stable time base for the system and determines the frequency accuracy of the DDS. It provides the clock to the NCO which produces at its output a discrete-time, quantized version of the desired output waveform (often a sinusoid) whose period is controlled by the digital word contained in the Frequency Control Register. The sampled, digital waveform is converted to an analog waveform by the DAC. The output reconstruction filter rejects the spectral replicas produced by the zero-order hold inherent in the analog conversion process.

Phases to amplitude converter (PAC)

This uses the phase accumulator output word usually as an index waveform look-up table (LUT) to provide a corresponding amplitude sample. Sometimes interpolation is used with the look-up table to provide better accuracy and reduced phase error noise. A binary accumulator consists of an N-bit binary adder and a register. Each clock cycle produces a N-bit output consisting of the previous output obtained from the register summed with the frequency control word (FCW) which is constant for a given output frequency. The adder is designed to overflow when the sum of the absolute value of its operands exceeds its capacity (2^n - 1). The overflow bits is discarded so the output width is always equal to its input word width. The PAC can be simple read only memory containing 2M contiguous sample of the desired output waveform.

III. Multi DDS Technology

Direct Digital Frequency Synthesis (DDFS or simply DDS), also known as Numerically Controlled Oscillator (NCO). Direct Digital Synthesizer (DDS) is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Applications of DDS include: signal generation, local oscillators in communication systems, function generators, mixers, modulators, sound synthesizers and as part of a digital phase-locked loop. A basic Direct Digital Synthesizer consists of a frequency reference, a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC). The reference provides a stable time base for the system and determines the frequency accuracy of the DDS. It provides the clock to the NCO which produces at its output a discrete-time, quantized version of the desired output waveform whose period is controlled by the digital word contained in the Frequency Control Register. The sampled,
digital waveform is converted to an analog waveform by the DAC. The output reconstruction filter rejects the spectral replicas produced by the zero-order hold inherent in the analog conversion process. Many possibilities for frequency generation are open to the designer, ranging from phase-locked-loop (PLL) based techniques for very high-frequency synthesis, to dynamic programming of digital-to-analog converter (DAC) outputs to generate arbitrary waveforms at lower frequencies. But the DDS technique is rapidly gaining acceptance for solving frequency (or waveform) generation requirements in both communications and industrial applications because single-chip IC devices can generate programmable analog output waveforms simply and with high resolution and accuracy.

IV. CORE ARCHITECTURE OVERVIEW

The core consists of two main parts, a Phase Generator and SIN/COS LUT, which can be used independently or together with an optional dither generator to create a DDS capability. A time-division multi-channel capability is supported, with independently configurable phase increment and offset parameters. Below Figure provides a block diagram of the DDS Compiler core.

Figure 4. DDS Compiler IP core

Phase Generator:

The Phase Generator consists of an accumulator followed by an optional adder to provide addition of phase offset. When the core is customized the phase increment and offset can be independently configured to be either fixed, programmable or supplied by the PINC_IN and POFF_IN input ports respectively. When set to programmable, registers are implemented with a bus interface, consisting of ADDR, REG_SELECT, WE, and DATA signals. The address input, ADDR, specifies the channel for which DATA is to be written when multi-channel, with REG_SELECT specifying whether DATA is phase increment or offset. When set to fix the DDS output frequency is set when the core is customized and cannot be adjusted once the core is embedded in a design.

SIN/COS LUT:

When configured as a SIN/COS LUT, the Phase Generator is not implemented, and the phase is input via the PHASE_IN port, and transformed into the sine and cosine outputs using a look-up table. Efficient memory usage is achieved using half-wave and quarter wave storage schemes. The presence of both outputs and their negation are configurable when the core is customized. Precision can be increased using optional Taylor Series Correction. This exploits Xtreme DSP slices on FPGA families that support them to achieve high SFDR with high speed operation.

V. LINEAR FREQUENCY MODULATION

An LFM signal is a kind of signal in which the frequency of the transmitted signal is varied over a pulse duration of $\tau_p$. This variation of the frequency from low to high or vice versa is known as “chirping”. Changing the frequency from low to high is called “up-chirp” or upsweep. Similarly, changing the frequency from high to low is called called “down-chirp”. The technique of applying a different chirp rate for each pulse is known as “chirp diversity”.

VI. IMPLEMENTATION

Linear frequency Modulated signal is generated using Multi DDS technology which is achieved by using single DDS IP core architected in parallel processing. Design is implemented using VHDL structural style of modelling on Xilinx Virtex 5 ML506 evaluation platform. FPGA utilization summary and Timing parameters are listed in below figure. The RTL schematics of the design top module is shown in figure.

VII. RESULTS

The device utilization summary is shown in below table.

Figure 5. Device utilization summary

Figure 6. Top level Module of Multi DDS

<table>
<thead>
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<th>Device Utilization Summary</th>
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<th>Variable</th>
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<tr>
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<td>50%</td>
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<tr>
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<td>99%</td>
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VIII. CONCLUSION

In this paper we have presented the implementation for generation of Linear Frequency Modulated signal at IF level using Multi-DDS Technology. This design was carried out on Xilinx Virtex-5 FPGA having an on board clock of 200MHz by using this clock we have generated the IF signal at 2GHz using very less resource utilization. The design results are cross verified using MATLAB generated code.

REFERENCES