Implementation of Linear Frequency Modulation signal generation using Multi DDS Technology on FPGA

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***Abstract*—Direct Digital Synthesizer (DDS) is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Radar Wave form generation is a prime challenge in digital radar Transmitter, with the demand on the performance and functionality of digital radar transmitter increases highly, it is particularly necessary to develop high-efficient up-conversion technology for generation of Linear Frequency Modulated signal using Multi-DDS Technology.Radar is an object detection system which uses radio waves to determine the range, altitude, direction, or speed of objects. Digital Up-conversion is the core technology in digital radar transmitter. To achieve high sampling rate, we have to use high clock frequency hence a high hardware clock is required. In this paper we are using the Multi-DDS (10 DDS) technology which is based on parallel processing, a large bandwidth signal can be produced at conditions of a lower hardware clock. This output signal is used to generate the Radar signal with high sampling rate (200 MHz). Similarly Multi-DDS technology gives a high-efficient solution. With this by using lower hardware clock high sampling rate can be achieved. As this paper presents the results based on a system (i.e. Virtex5 FPGA) whose clock frequency is 200MHz.**

***Index Terms*—Digital up-conversion; high-efficient; parallel processing;Linear Frequency Modulation;Multi-DDS Technology.**

I. Introduction

Depending on its flexibility, small size and low development costs,digital radar tranmitter is widely used in the field of radar signal processing.But with the Traditional digital up conversion process is used to achieve high sampling rate, we have to use high clock frequency hence high hardware clock is required. With this Multi-DDS (10 DDS) technology a lower hardware clock and high sampling rate can be achieved. As this paper presents the results based on a system (i.e Virtex5-FPGA) whose clock frequency is 200MHz.By assuming that 1DDS will give 200MHz clock Frequency. In this paper we are using a multi-DDS technique by assuming (10 DDS) that 10 DDS are working parallel to generate 2GHz Clock .sampling Rate increases from 200MHz to 2GHz in order to meet the requirement of Radar applications. RADAR (Acronym for Radio Detection and Ranging) is an object-detection system that uses radio waves to determine the range, altitude, direction, or speed of objects. A radar system has a transmitter that emits radio waves called radar signals in predetermined directions. When these come into contact with an object they are usually reflected or scattered in many directions.The radar signals that are reflected back towards the transmitter are the desirable ones that make radar work.

Radar receivers are usually, but not always in the same location as the transmitter. Although the reflected radar signals captured by the receiving antenna are usually very weak, they can be strengthened by electronic amplifiers. More sophisticated methods of signal processing are also used in order to recover useful radar signals.

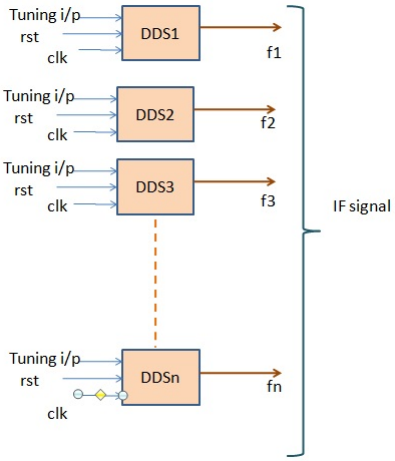

Figure 1. Block diagram of Multi DDS

The above figure shows generic DDS which is a combination of n DDS modules. According to this paper for getting 200MHz sampling rate 10 DDS are suffice. With this we are generating the radar signal and finally got the radar signal with high sampling rate.

II. Single DDS unit

A digitally-controlled method of generating multiple frequencies from a reference frequency source has evolved called Direct Digital Synthesis (DDS). The NCO main purpose is to generation the carrier signals (cosine).The main advantage is ROM based techniques will be used for area optimization.

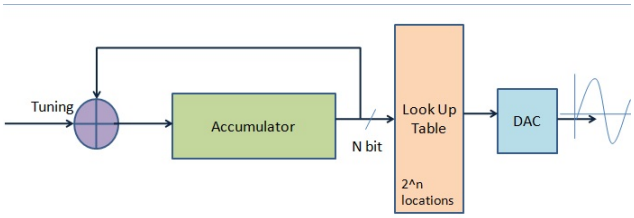

Figure 2. Single DDS architecture

A numerically controlled oscillator (NCO) is a digital signal generator which creates a synchronous, discretetime, discrete valued representation of a waveform. NCOs are often used in conjuction with a Digital-toanalog converter (DAC)at the output to create a direct digital synthesizer(DDS).Applications of DDS include: signal generation, local oscillators in communication systems, function generators, mixers, modulators, sound synthesizers and as part of a digital phase-locked loop. A basic Direct Digital Synthesizer consists of a frequency reference, a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC).

The reference provides a stable time base for the system and determines the frequency accuracy of the DDS. It provides the clock to the NCO which produces at its output a discrete-time, quantized version of the desired output waveform (often a sinusoid) whose period is controlled by the digital word contained in the Frequency Control Register. The sampled, digital waveform is converted to an analog waveform by the DAC. The output reconstruction filter rejects the spectral replicas produced by the zero-order hold inherent in the analog conversion process.

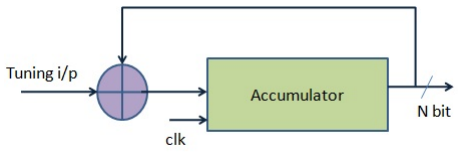

Figure 3. Phase Accumulator

Which adds to the value held at its output a frequency control value at each clock sample. The phase accumulator consists of phase increment register, adder and phase register. The phase increment register stores the instantaneous phase increment values resulting from frequency modulation control block. Look up Tables are programmed to consider 255 as highest phase value and phase increment by one results next cycle of waveform.

All the blocks are connected with common clock and reset signals. The delta phase value decides the phase increment for each clock pulse. Hence decides the resulting signal frequency. The Frequency modulating instantaneous value is added to the delta phase value which causes instantaneous change in frequency. Due to the digital nature of the modulator only at each clock tick the modulating signal value shall affect the resulting frequency. If the modulating signal is analog then an Analog to Digital converter must be used to digitize the modulating signal which can be used in NCO. The phase accumulator produces accumulated phase value for each clock pulse. In case if the DDS is used for phase modulation then instantaneous phase modulating signal value is added to the phase output of phase accumulator.

The Parallel in Parallel Out shift register cells are required in phase accumulator block to hold frequency and phase values. Synchronization is required between the phase increment register and phase register. This is achieved by connecting a common clock signal.Generic is used in VHDL implementation which allows to instantiate the PIPO component any bit size.

The heart of the system is the phase accumulator whose content is updated once for each clock cycle. Each time the phase accumulator is updated, the digital number M stored in the delta phase register is added to the number in the phase accumulator register. The truncated output of the phase accumulator serves as the address to a sine (or cosine) lookup table. Each lookup table contains the corresponding digital amplitude information for one complete cycle of a sine wave. The lookup table therefore maps the phase information from the phase accumulator into a digital amplitude word, which in turn drives the DAC.

Phase to amplitude converter (PAC)

This uses the phase accumulator output word usually as an index waveform look-up table (LUT) to provide a corresponding amplitude sample. Sometimes interpolation is used with the look-up table to provide better accuracy and reduced phase error noise. A binary accumulator consists of an N-bit binary adder and a register. Each clock cycle produces a N-bit output consisting of the previous output obtained from the register summed with the frequency control word(FCW) which is constant for a given output frequency. The adder is designed to overflow when the sum of the absolute value of its operands exceeds its capacity(2n-1).The overflow bits is discarded so the output word width is always equal to its input word width .The PAC can be simple read only memory containing 2M contiguous sample of the desired output waveform.

III. Multi DDS Technology

Direct Digital Frequency Synthesis (DDFS or simply DDS), also known as Numerically Controlled Oscillator (NCO). Direct Digital Synthesizer (DDS) is a type of frequency synthesizer used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Applications of DDS include: signal generation, local oscillators in communication systems, function generators, mixers, modulators, sound synthesizers and as part of a digital phase-locked loop.A basic Direct Digital Synthesizer consists of a frequency reference, a numerically controlled oscillator (NCO) and a digital-to-analog converter (DAC).The reference provides a stable time base for the system and determines the frequency accuracy of the DDS. It provides the clock to the NCO which produces at its output a discrete-time, quantized version of the desired output waveform whose period is controlled by the digital word contained in the Frequency Control Register. The sampled,

digital waveform is converted to an analog waveform by the DAC. The output reconstruction filter rejects the spectral replicas produced by the zero-order hold inherent in the analog conversion process. Many possibilities for frequency generation are open to the designer, ranging from phase-locked-loop (PLL) based techniques for very high-frequency synthesis, to dynamic programming of digital-to-analog converter (DAC) outputs to generate arbitrary waveforms at lower frequencies. But the DDS technique is rapidly gaining acceptance for solving frequency (or waveform) generation requirements in both communications and industrial applications because single-chip IC devices can generate programmable analog output waveforms simply and with high resolution and accuracy.

IV. Core Architecture Overview

The core consists of two main parts, a Phase Generator and SIN/COS LUT, which can be used independently or together with an optional dither generator to create a DDS capability. A time-division multi-channel capability is supported, with independently configurable phase increment and offset parameters. Below Figure provides a block diagram of the DDS Compiler core.

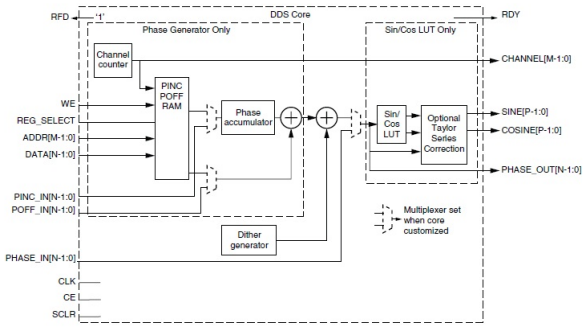

Figure 4. DDS Compiler IP core

Phase Generator:

The Phase Generator consists of an accumulator followed by an optional adder to provide addition of phase offset. When the core is customized the phase increment and offset can be independently configured to be either fixed, programmable or supplied by the PINC_IN and POFF_IN input ports respectively. When set to programmable, registers are implemented with a bus interface, consisting of ADDR, REG_SELECT, WE, and DATA signals. The address input, ADDR, specifies the channel for which DATA is to be written when multi-channel, with REG_SELECT specifying whether DATA is phase increment or offset. When set to fix the DDS output frequency is set when the core is customized and cannot be adjusted once the core is embedded in a design.

SIN/COS LUT:

When configured as a SIN/COS LUT, the Phase Generator is not implemented, and the phase is input via the PHASE_IN port, and transformed into the sine and cosine outputs using a look-up table. Efficient memory usage is achieved using half wave and quarter wave storage schemes. The presence of both outputs and their negation are configurable when the core is customized. Precision can be increased using optional Taylor Series Correction. This exploits Xtreme DSP slices on FPGA families that support them to achieve high SFDR with high speed operation.

V. Linear Frequency Modulation

An LFM signal is a kind of signal in which the frequency of the transmitted signal is varied over a pulse duration of τ_p. This variation of the frequency from low to high or vice a versa is known as “chirping”. Changing the frequency from low to high is called “up-chirp” or upsweep . Similarly, changing the frequency from high to low is called called “down-chirp”. The technique of applying a different chirp rate for each pulse is known as “chirp diversity”.

VI. Implementation

Linear frequency Modulated signal is generated using Multi DDS technology which is achived by using single DDS IP core architectured in parrallel processing. Design is implemented using VHDL structural style of modelling on Xilinx Virtex 5 ML506 evaluation platform. FPGA utilization summary and Timing parametrs are listed in below figure. The RTL schematics of the design top module is shown in figure.

VII. Results

The device utilization summary is shown in below table

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	1879	32640	5%
Number of Slice LUTs	1436	32640	4%
Number of fully used LUT-FF pairs	937	2378	39%
Number of bonded IOBs	14	480	2%
Number of Block RAM/FIFO	10	132	7%
Number of BUFG/BUFGCTRLs	3	32	9%

Figure 5. Device utilaztion summary

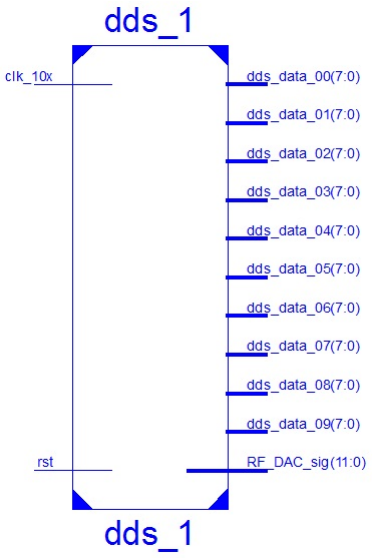

Figure 6. Top level Module of Multi DDS

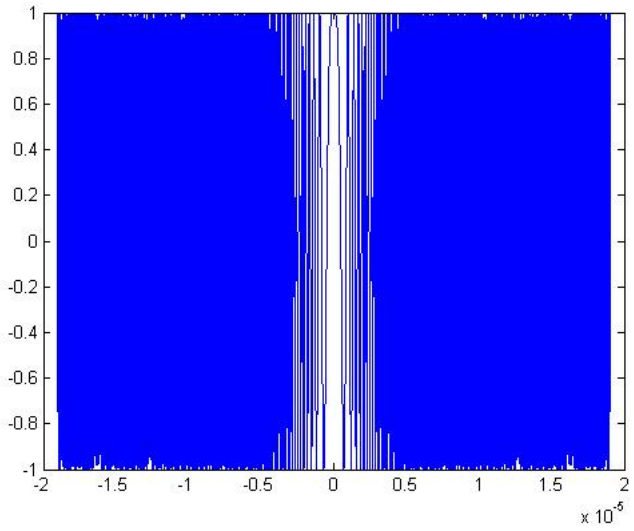

Figure 7. LFM signal

VIII. Conclusion

In this paper we have presented the implementation for generation of Linear Frequency Modulated signal at IF level using Multi-DDS Technology. This design was carried out on Xilinx Viretx5 FPGA having an on board clock of 200MHz by using this clock we have generated the IF signal at 2GHz using very less resource utilization. The design results are cross verified using MATLAB generated code.

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