COST EFFICIENT SERIES CONNECTION OF SUBMULTILEVEL INVERTERS

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Abstract:

In this paper, initially a new topology for sub multilevel inverter is proposed and then series connection of the sub multilevel inverters is proposed as a generalized multilevel inverter for cost efficient basis. The proposed multilevel inverter uses reduced number of switching devices. Special attention has been paid to obtain optimal structures regarding different criteria such as number of switches, standing voltage on the switches, number of dc voltage sources, etc. The proposed multilevel inverter has been analyzed in symmetric conditions.

I. INTRODUCTION

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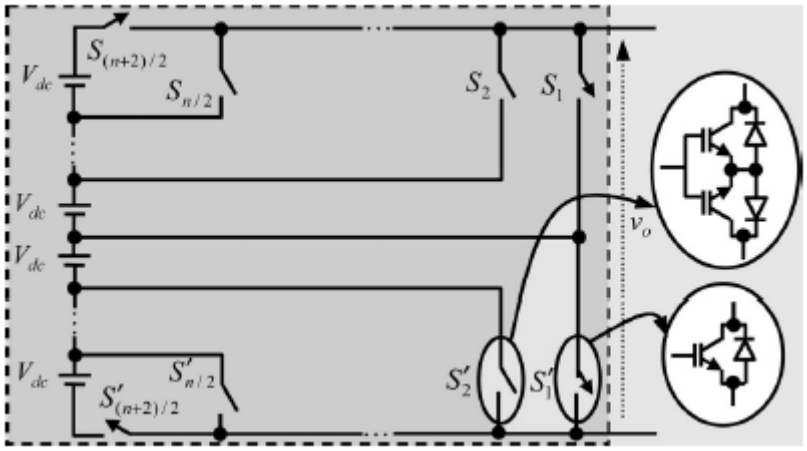

Fig. 1. Proposed generalized submultilevel inverter.

The power loss of the proposed topology is calculated. Afterward, the proposed multilevel inverter is compared with other multilevel inverter topologies considering the number

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of switches. A design example is then given which is used for simulation and experimental studies

TABLE I
OUTPUT VOLTAGES FOR STATES OF SWITCHES

State	Switches states									v_o
	S_1	S_1'	S_2	S_2'	...	$S'_{n/2}$	$S_{n/2}$	$S_{(n+2)/2}$	$S'_{(n+2)/2}$	
1	1	1	0	0	...	0	0	0	0	0
2	0	1	1	0	...	0	0	0	0	V_{dc}
3	0	0	1	1	...	0	0	0	0	$2V_{dc}$
⋮	⋮	⋮	⋮	⋮	...	⋮	⋮	⋮	⋮	⋮
$n-1$	0	0	0	0	...	1	1	0	0	$(n-2)V_{dc}$
n	0	0	0	0	...	0	1	0	1	$(n-1)V_{dc}$
n - 1	0	0	0	0	...	0	0	1	1	nV_{dc}

Considering Fig. 1, for each value of the output voltage of submultilevel inverter, two switches must be turned ON, one from the upper switches and the other from the lower switches. For example, to get output voltage of *V*dc, the switches *S'*1 and *S*2 are turned ON. In order to obtain the output voltage of (*n*−1) *Vdc*, the switches *Sn*/2 and *S'* (*n*+2)/2 should be turned ON.

Considering Fig. 1, the following equations can be written:

$$N_{\text{switch,sub}} = \begin{cases} 2, & \text{for } n = 1 \\ (n+2), & \text{for } n \geq 2 \end{cases} \quad (1)$$

$$N_{\text{driver,sub}} = N_{\text{switch,sub}} \quad (2)$$

$$N_{\text{IGBT,sub}} = 2n \quad (3)$$

$$N_{\text{source,sub}} = n \quad (4)$$

where, *N*switch,sub, *N*driver,sub, *N*IGBT,sub, and *N*source,sub are the number of switches, number of switches drivers in one sub-multilevel inverter, number of IGBTs in one sub-multilevel inverter, and number of dc sources in one sub-multilevel inverter, respectively.

For the proposed typical sub-multilevel inverter (see Fig. 1), the standing voltage on the switches is calculated. A switch experiences different off-state voltages in different switching combinations. Among these off-state voltages, the highest voltage is considered to be the standing voltage of the switch. This can be a criterion for voltage rating of the switch. For example, in Fig. 1, the switch *S*1 experiences the maximum off-state voltage when the switch

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$S(n+2)/2$ is turned ON that is equal to $(n/2)V$dc. For the switch $S2$, the standing voltage is $(n/2 - 1)V$dc. For the switches S_1 and S_2 , the standing voltage is equal to $(n/2)V$dc and $(n/2 - 1)V$dc, respectively. This calculation can be done for any switch in the sub-multilevel inverter. The standing voltage for the sub-multilevel inverter is sum of all standing voltage on the switches in their off state [12]. For a sub-multilevel inverter including n dc voltage sources, the standing voltage on the switches depends on n and whether it is odd or even. For different n, the standing voltage on the switches of ith sub-multilevel inverter (Vstand,i) can be obtained by (5), shown at the bottom of the next page.

Proposed Generalized Multilevel Inverter

The proposed sub-multilevel inverters can be connected in series to achieve the desired voltage and number of voltage levels. Fig. 2 shows m sub multilevel inverters in series. Each sub-multilevel inverter has n dc voltage source. The dc voltage sources in each sub-multilevel inverter are equal.

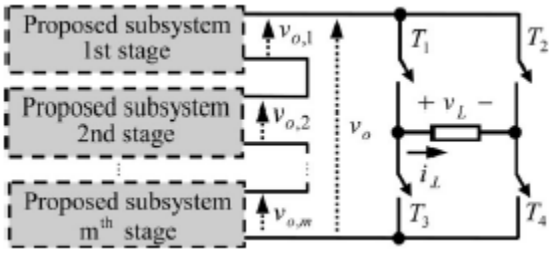

Fig. 2. Proposed general multilevel inverter using series connection of m proposed sub-multilevel inverters, each one has n dc voltage sources.

The output voltage of the sub-multilevel inverters (and series connection of them) is always positive or zero. To operate as an inverter, it is necessary to change the voltage polarity in every half cycle. For this purpose, an H-bridge inverter is added to the output of the series connected sub-multilevel inverters.

It is important to note that the switches of the H-bridge must withstand higher voltage. This should be considered in the design of the inverter. However, these switches are turned ON and OFF once during a fundamental cycle. So, these switches would be high-voltage low-frequency switches.

Considering that the multilevel inverter shown in Fig. 2 includes m sub-multilevel inverter (using (1)–(4) and considering the H-bridge part), the following equations can be written:

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$$N_{\text{switch}} = \begin{cases} 2m+4, & \text{for } n = 1 \\ m \cdot (n+2) + 4, & \text{for } n \geq 2 \end{cases} \quad (6)$$

(7)

$$N_{\text{driver}} = N_{\text{switch}}$$

$$N_{\text{IGBT}} = 2mn + 4 \quad (8)$$

$$N_{\text{source}} = mn \quad (9)$$

where *N*switch, *N*driver , *N*IGBT, and *N*source are the number of switches, number of switches drivers (which is equal to number of switches), number of IGBTs, and total number of dc sources, respectively.

Considering (6) and (8), in general, the number of IGBTs is not equal to the number of switches in the proposed multilevel inverter; hence, some of the switches are bidirectional (which is considered as one switch) and consist of two IGBTs. The proposed topology can be extended to three-phase systems using three single-phase units.

1) ***Proposed symmetric Multilevel Inverter:***

For the symmetric topology, the value of the dc voltage sources is different from a sub-multilevel inverter to another. In other words, if the dc sources of the first sub-multilevel inverter is $V_{\text{dc},1}$, the dc sources of the second sub-multilevel inverter is $V_{\text{dc},2}$. To get maximum number of level for the output voltage, there must be no redundancy. This is achieved when the value of the dc voltage sources in sub-multilevel inverters have the following relation:

$$V_{\text{dc},2} = (n+1) \cdot V_{\text{dc},1}$$

$$V_{\text{dc},3} = (n+1)V_{\text{dc},1} + nV_{\text{dc},2} = (n+1)V_{\text{dc},1} + n(n+1)V_{\text{dc},1}$$

$$= (n+1)(n+1)V_{\text{dc},1} = (n+1)^2 V_{\text{dc},1} \quad (16)$$

Therefore, in general, the following relation should be valid for the dc sources of the sub-multilevel inverters:

$$V_{\text{dc},i} = (n+1)^{i-1} \cdot V_{\text{dc},1}, \qquad i = 1, 2, 3, \ldots, m \quad (17)$$

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Where Vdc,i is the value of the dc sources in the ith sub-multilevel inverter. The maximum value of the output voltage (sum of all dc voltage sources) for the proposed asymmetric topology can be obtained as follows:

$$V_{o,\max} = n\sum_{i=1}^{m} V_{\mathrm{dc},i}. \tag{18}$$

Using (17) and (18), the maximum value of the output voltage can be written as

$$V_{o,\max} = [(n+1)^m - 1]V_{\mathrm{dc},1}. \tag{19}$$

With the aforementioned arrangement of the dc voltage sources, the number of voltage levels will be equal to

$$N_{\mathrm{level}} = 2(n+1)^m - 1. \tag{20}$$

For the asymmetric topology, the total standing voltage of the switches (Vstand,total) is sum of standing voltages on the switches of the sub-multilevel inverters ($\sum_{i=1}^{m} V\mathrm{stand}, i$) and also the standing voltage on the switches of the H-bridge part (4Vo,max). Therefore, it can be written as follows

$$V_{\mathrm{stand,total}} = \sum_{i=1}^{m} V_{\mathrm{stand},i} + 4V_{o,\max}. \tag{21}$$

Using (5), (17), (19), and (21), the total standing voltage of the switches can be written as follows:

$$V_{\mathrm{stand,total}} = \left[\frac{(n+1)^m - 1}{n}\right] \cdot V_{\mathrm{stand},1} + 4[(n+1)^m - 1] \cdot V_{\mathrm{dc},1}. \tag{22}$$

Using (20) and (22), the total standing voltage in terms of number of output voltage level and n can be expressed as follows:

$$V_{\mathrm{stand,total}} = \left(\frac{N_{\mathrm{level}} - 1}{2}\right) \cdot \left(\frac{V_{\mathrm{stand},1}}{n} + 4V_{\mathrm{dc},1}\right) \tag{23}$$

C. Optimal Structures

In this section, the aim is to determine the optimal structures considering different aspects. For the proposed multilevel inverter, there are two design parameters. The first parameter is the number of dc sources in each sub-multilevel inverter n and the other is the

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1) Optimal Structures of the symmetric Topology: The first optimal structure is to determine n to obtain the maximum voltage level for a constant number of switches (or driver circuits). Using (6) and (20), the number of voltage levels in terms of number of switches is as follows:

$$N_{\text{level}} = \begin{cases} 2(2)^{\frac{N_{\text{switch}}-4}{2}} - 1, & \text{for } n = 1 \\ 2(n+1)^{\frac{N_{\text{switch}}-4}{(n+2)}} - 1, & \text{for } n \geq 2 \end{cases}$$
$$= \begin{cases} 2(2^{\frac{1}{2}})^{N_{\text{switch}}-4} - 1, & \text{for } n = 1 \\ 2\left[(n+1)^{\frac{1}{(n+2)}}\right]^{(N_{\text{switch}}-4)} - 1, & \text{for } n \geq 2. \end{cases} \quad (27)$$

In (27), the number of switches is considered as a constant. Therefore, the number of voltage levels is maximized for such an n that maximizes the following term:

$$D = \begin{cases} 2^{\frac{1}{2}}, & \text{for } n = 1 \\ (n+1)^{\frac{1}{(n+2)}}, & \text{for } n \geq 2. \end{cases} \quad (28)$$

Fig. 4 shows the variation of D versus n. As the figure indicates, $n = 1$ gives the optimal structure from the viewpoint of number of switches.

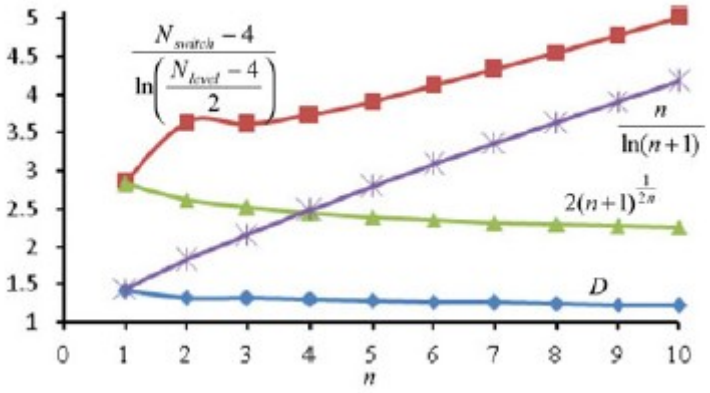

Fig. 4. Variation of D, (29), $2(n + 1)1/2n$, and $n/\ln(n + 1)$ versus n.

Similarly, another optimal structure can be obtained for minimizing the number of switches for a constant number of voltage levels.

The variation of (29) versus n is also depicted in Fig. 4. It is clear that $n = 1$ gives again the optimal structure. Considering (7), the number of gate drivers is equal to the number of switches. Therefore, $n = 1$ also gives the optimal structure from the viewpoint of minimum gate drivers. In the previous analysis, the number of switches was considered as a criterion for determining the

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optimal structures. As mentioned before, the number of switches is not equal to the number of IGBTs. If the number of IGBTs is used as a criterion, the results will be the same. Considering (8) and (20), the number of voltage levels as a function of n for a constant number of IGBTs is as follows:

$$N_{\text{level}} = 2(n+1)^{\frac{N_{\text{IGBT}}-4}{2n}} - 1 = 2\left[(n+1)^{\frac{1}{2n}}\right]^{(N_{\text{IGBT}}-4)} - 1. \quad (30)$$

Taking into account that the number of IGBTs has been considered to be constant, in (30), the number of voltage levels will be maximum if the term $2(n + 1)1/2n$ is maximum. Fig. 4 also shows the variation of $2(n + 1)1/2n$ versus n. As this figure shows, the number of levels decreases as n increases.

Therefore, the maximum number of voltage level for a constant number of IGBTs is obtained when n is equal to 1. The same result can be obtained for the minimum number of IGBTs for a constant number of voltage levels.

The number of the dc voltage sources Nsource is the other variable which is used to obtain optimal topology. The aim is to minimize the number of required dc voltage sources for a specific number of voltage levels. Using (9) and (20), Nsource can be written as follows in terms of the number of output voltage levels and the number of dc voltage sources in each submultilevel inverter:

$$N_{\text{source}} = \frac{n}{\ln(n+1)} \cdot \ln\left(\frac{N_{\text{level}}+1}{2}\right). \quad (31)$$

The aforementioned equation gets its minimum value when the term $n/\ln(n + 1)$ is minimum. Variation of this term versus n is also shown in Fig. 4. It is clear that the minimum value is achieved when $n = 1$.

To obtain the optimal structure from viewpoint of standing voltage on the switches, using (23), the normalized total standing voltage is obtained as follows:

$$\text{Normalized } V_{\text{stand,total}} = \frac{V_{\text{stand,total}}}{(N_{\text{level}}-1)\cdot V_{\text{dc,1}}} - 2 = \frac{V_{\text{stand,1}}}{2nV_{\text{dc,1}}}. \quad (32)$$

This equation is same as (26). Therefore, for the asymmetric topology (like the symmetric topology), the optimal structure considering the total standing voltage on the switches

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is achieved for $n = 1$ and $n = 2$. It is important to note that the standing voltage on the switches is the same for these two values of n. This is clear from Fig. 1 for $n = 1$ and $n = 2$.

It can be concluded from the previous analysis that the optimal structure (for the asymmetric topology) from the viewpoint of the number of used switches, IGBTs, dc voltage sources, and the value of the standing voltage on the switches is obtained when n is 1.

OPERATION OF SYMMETRIC TOPOLOGY:

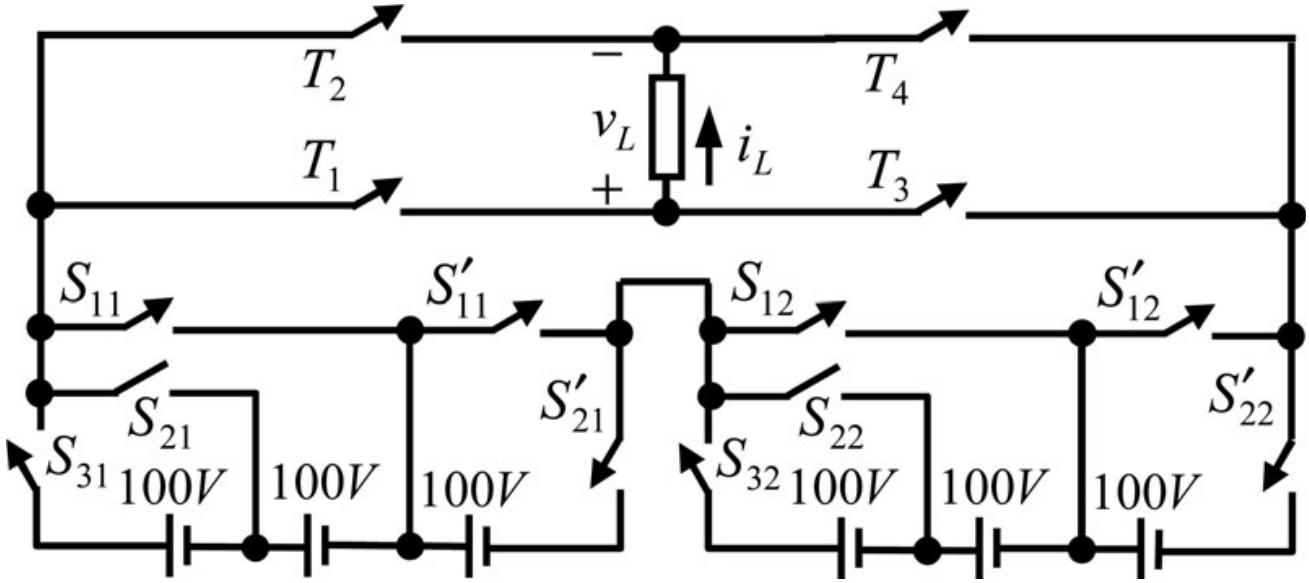

Fig. 13-level symmetric topology of submultilevel inverter

SIMULATION RESULTS:

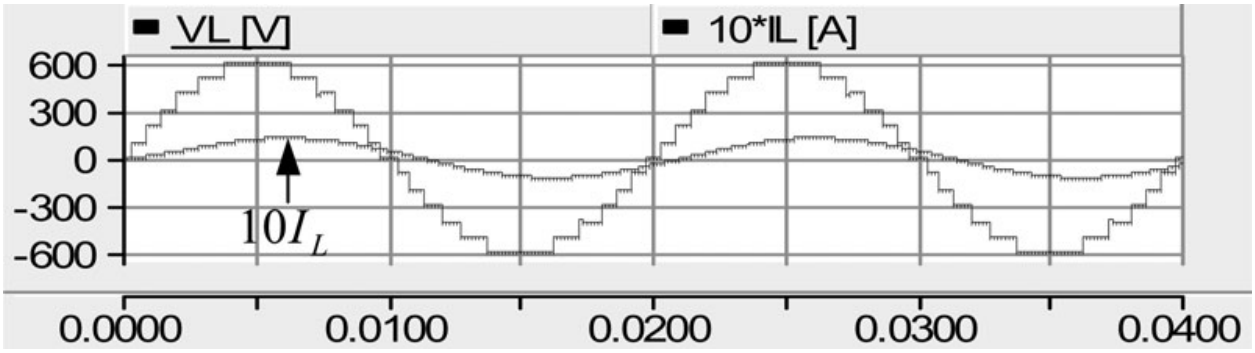

Fig. Simulation results for the 13-level symmetric topology

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VII. CONCLUSION

In this paper, initially, a submultilevel inverter has been proposed and then the cascaded submultilevel inverters have been considered as a generalized multilevel inverter in both symmetric and asymmetric conditions. The number of the dc voltage sources in each submultilevel inverter is equal. Therefore, the proposed multilevel inverter can be categorized in symmetric group. The optimal structures for the proposed multilevel inverter were obtained considering several factors such as the number of switching devices, number of dc voltage sources, number of output voltage levels, standing voltage on the switches etc. The comparison between the proposed topology and the topologies presented, the CHB topologies has been presented considering several factors. The simulation results of a 13-level symmetric topology based on the proposed multilevel inverter have been presented.

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