Power Factor Correction of BLDC Motor Drive Using Bridge Less Buck-Boost Converter

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Abstract— **In this paper, a power factor corrected (PFC) bridgeless (BL) buck-boost converter topology is proposed in order to fed a brushless direct current (BLDC) motor drive for low-power applications. A Novel bridgeless buck-boost converter configuration is proposed, which avoids the need of the diode bridge rectifier, reducing the conduction losses which incurred because of it. The dc link voltage of voltage source inverter (VSI) with single voltage sensor is varied to control the speed of BLDC motor. This makes the VSI to operate at fundamental frequency switching which utilizes the electronic commutation of BLDC motor and also achieves reduced switching losses. A PFC based bridgeless buck-boost converter is designed in such a way to operate in Discontinuous Inductor Current Mode (DCIM), so that it provides an inherent PFC at ac mains. In this paper bridgeless buck-boost converter topology equations are derived and the design of the bridgeless buck boost topology is given. In this paper, the drive performance is evaluated by varying the supply voltage and by wide range speed control. Due to this, at ac mains, the power quality is improved and the obtained power quality indices are within the range of International power quality standards like IEC 61000-3-2. Finally, in Matlab/Simulink environment, both the steady state and dynamic state performances of the proposed drive are simulated, which improved the power quality at ac mains.**

Index Terms—**Bridgeless (BL) buck–boost converter, brushless direct current (BLDC) motor, discontinuous inductor current mode (DICM), power factor corrected (PFC), power quality.**

I. INTRODUCTION

Efficiency and cost would be the major concerns in the development of low-power motor drives targeting household applications such as for example fans, water pumps, blowers, mixers, etc. The utilization of the brushless direct current (BLDC) motor in these applications is becoming very common due to options that come with high efficiency, high flux density per unit volume, low maintenance requirements, and low electromagnetic-interference problems. These BLDC motors are not limited to household applications, but they're ideal for other applications such as for example medical equipment, transportation, HVAC, motion control, and many industrial tools.

A BLDC motor has three phase windings on the stator and permanent magnets on the rotor. The BLDC motor can be referred to as an electronically commutated motor because an electronic

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commutation based on rotor position can be used rather than mechanical commutation which includes disadvantages like sparking and wear and tear of brushes and commutator assembly. Power quality problems have become important issues to be looked at due to the recommended limits of harmonics in supply current by various international power quality standards like the International Electro technical Commission (IEC) 61000-3-2. For class-A equipment (< 600 W, 16 A per phase) which include household equipment, IEC 61000-3-2restricts the harmonic current of different order such that the full total harmonic distortion (THD) of the supply current must be below 19%. A BLDC motor when fed by way of a diode bridge rectifier (DBR) with a higher value of dc link capacitor draws peaky current which can cause a THD of supply current of the order of 65% and power factor as little as 0.8.Hence, a DBR followed by way of a power factor corrected (PFC) converter is utilized for improving the ability quality at ac mains. Many topologies of the single-stage PFC converter are reported in the literature which includes gained importance due to high efficiency as compared to two-stage PFC converters due to low component count and an individual switch for dc link voltage control and PFC operation. The decision of mode of operation of a PFC converter is just a critical issue since it directly affects the price and rating of the components used in the PFC converter. The continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are the 2 modes of operation by which a PFC converter is designed to operate. In CCM, the present in the inductor or the voltage over the intermediate capacitor remains continuous, but it needs the sensing of two voltages (dc link voltage and supply voltage) and input side current for PFC operation, that is not cost-effective. On another hand, DCM requires someone voltage sensor for dc link voltage control, and inherent PFC is achieved at the ac mains, but at the cost of higher stresses on the PFC converter switch; hence, DCM is preferred for low-power applications.

The conventional PFC scheme of the BLDC motor drive utilizes a pulse width-modulated voltage source inverter (PWM-VSI) for speed control with a consistent dc link voltage. This offers higher switching losses in VSI while the switching losses increase as a square function of switching frequency. While the speed of the BLDC motor is directly proportional to the applied dc link voltage, hence, the speed control is accomplished by the variable dc link voltage of VSI. This enables the fundamental frequency switching of VSI (i.e., electronic commutation) and offers reduced switching losses. Singh and Singh have proposed a buck–boost converter feeding a BLDC motor on the cornerstone of the idea of constant dc link voltage and PWM-VSI for speed control which includes high switching losses. A single-ended primary-inductance converter (SEPIC)-based BLDC motor drive has been proposed by Gopalarathnam and Toliyat but has higher losses in VSI as a result of PWM switching and an elevated level of current and voltage sensors which restricts its applicability in low-cost application. Singh and Singh have proposed a Cuk converter-fed BLDC motor drive with the idea of variable dc link voltage. This reduces the switching losses in VSI as a result of fundamental switching frequency operation for the electronic commutation of the BLDC motor and to the variation of the speed by controlling the voltage at the dc bus of VSI. A CCM operation of the Cuk converter has been utilized which requires three

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sensors and isn't encouraged for cheap and low power rating.

For further improvement in efficiency, bridgeless (BL) converters are employed which permit the elimination of DBR in the front end. A buck–boost converter configuration is most effective among various BL converter topologies for applications requiring a wide selection of dc link voltage control (i.e., bucking and boosting mode). Jang and Jovanovi´c and Huber *et al.* have presented BL buck and boost converters, respectively. These may provide the voltage buck or voltage boost which limits the operating selection of dc link voltage control. Wei *et al.* have proposed a BL buck–boost converter but use three switches which will be not a cost-effective solution. A fresh group of BL SEPIC and Cuk converters has been reported in the literature but takes a large quantity of components and has losses connected with it. This paper presents a BL buck–boost converter-fed BLDC motor drive with variable dc link voltage of VSI for improved power quality at ac mains with reduced components.

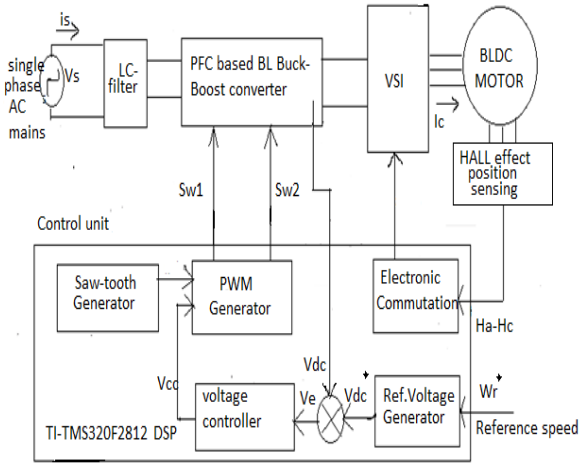

Fig. 1. Proposed BLDC motor drive with front-end BL buck–boost converter

II. PROPOSED PFC BL BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE

Fig. 1 shows the proposed BL buck–boost converter-based VSI-fed BLDC motor drive. The parameters of the BL buck–boost converter are made such that it operates in discontinuous inductor current mode (DICM) to attain an inherent power factor correction at ac mains. The speed control of BLDC motor is accomplished by the dc link voltage control of VSI using a BL buck–boost converter. This reduces the switching losses in VSI because of the low frequency operation of VSI for the electronic commutation of the BLDC motor. The performance of the proposed drive is evaluated for a wide selection of speed control with improved power quality at ac mains. Moreover, the effect of supply voltage variation at universal ac mains can be studied to demonstrate the performance of the drive in practical supply conditions. Voltage and current stresses on the PFC converter switch will also be evaluated for determining the switch rating and heat sink design. Finally, a hardware implementation of the proposed BLDC motor drive is carried out to demonstrate the feasibility of the proposed drive over a wide selection of speed control with improved power quality at ac mains. A short comparison of numerous configurations reported in the literature is tabulated in Table I. The comparison is carried on the basis of the total amount of components (switch—*S*w, diode—D, inductor—L, and capacitor—C) and total amount of components conducting during each half cycle of supply voltage. The BL buck and boost converter configurations are not suitable for the necessary application because of the requirement of high voltage conversion ratio. The proposed configuration of the BL buck–boost converter has the minimum amount of components and least amount of conduction devices during each half cycle of supply

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voltage which governs the decision of the BL buck–boost converter with this application.

III. OPERATING PRINCIPLE OF PFC BL BUCK–BOOST CONVERTER

The operation of the PFC BL buck–boost converter is classified into two parts which include the operation throughout the positive and negative half cycles of supply voltage and during the entire switching cycle.

A. Operation During Positive and Negative Half Cycles of Supply Voltage

In the proposed scheme of the BL buck–boost converter, switches *Sw*1 and *Sw*2 operate for the positive and negative half cycles of the supply voltage, respectively. Throughout the positive half cycle of the supply voltage, switch *Sw*1, inductor *Li*1, and diodes *D*1 and *Dp* are operated to transfer energy to dc link capacitor *Cd* as shown in Fig. 2(a)–(c). Similarly, for the negative half cycle of the supply voltage, switch *Sw*2, inductor *Li*2, and diodes *D*2 and *Dn* conduct as shown in Fig. 3(a)–(c).In the DICM operation of the BL buck–boost converter, the current in inductor *Li* becomes discontinuous for a particular duration in a switching period. Fig. 2(d) shows the waveforms of different parameters throughout the positive and negative half cycles of supply voltage.

B. Operation During Complete Switching Cycle

Three modes of operation throughout a complete switching cycle are discussed for the positive half cycle of supply voltage as shown hereinafter

Mode I:In this mode, switch *Sw*1 conducts to charge the inductor *Li*1; hence, an inductor current *i*Li1 increases in this mode as shown in Fig. 2(a). Diode *D p* completes the input side circuitry, whereas the dc link capacitor *Cd* is discharged by the VSI-fed BLDC motor as shown in Fig. 3(d).

Mode II:As shown in Fig. 2(b), in this mode of operation, switch *Sw*1 is turned off, and the stored energy in inductor *Li*1 is utilized in dc link capacitor *C d* before the inductor is wholly discharged. The existing in inductor *Li*1 reduces and reaches zero as shown in Fig. 3(d).

Mode III:In this mode, inductor *Li*1 enters discontinuous conduction, i.e., no energy is left in the inductor; hence, current *i*Li1 becomes zero for the remaining switching period. As shown in Fig. 2(c), none of the switch or diode is conducting in this mode, and dc link capacitor *C d* supplies energy to the load; hence, voltage *V* dc across dc link capacitor *C d* starts decreasing. The operation is repeated when switch *Sw*1 is fired up again after a complete switching cycle.

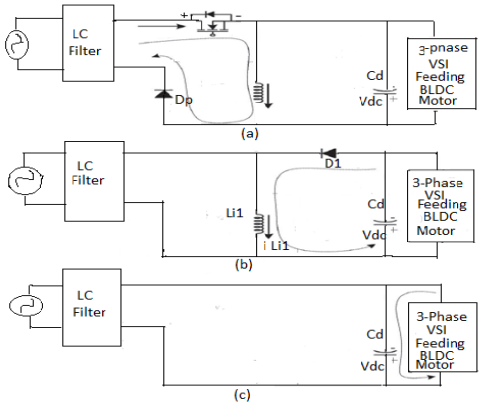

Fig. 2. Operation of the proposed converter in numerous modes (a)–(c) for a positive half cycle of supply voltage and (d) the associated waveforms. (a) Mode I. (b) Mode II. (c) Mode III.

Similarly, for the negative half cycle of the supply voltage, switch *Sw*2, inductor *Li*2, and diodes *Dn* and *D*2 operate for voltage control and PFC operation.

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IV. DESIGN OF PFC BL BUCK–BOOST CONVERTER

A PFC BL buck–boost converter was created to operate in DICM such that the current in inductors *Li*1 and *Li*2 becomes discontinuous in a switching period. For a BLDC of power rating 251 W (complete specifications of the BLDC motor aregiven in the Appendix), a power converter of 350 W (*Po*) is designed. For a supply voltage by having an rms value of 220 V, the average voltage appearing at the input side is given as

The relation governing the voltage conversion ratio for a buck–boost converter is given as

$$V_{dc} = \frac{V_{dc}}{V_{dc} + V_{dc}}$$

The proposed converter is designed for dc link voltage control from 50 V (*V* dc min) to 200 V (*V* dc max) with a nominal value (*V* dc des) of 100 V; hence, the minimum and the most duty ratio (*d* min and *d* max) corresponding to *V* dc min and *V* dc max are calculated as 0.2016 and 0.5025, respectively.

*A. Design of Input Inductors (Li*1 *and Li*2*)*

The value of inductance *L*ic1, to work in critical conduction mode in the buck–boost converter, is given as

$$L_{ic1} = \frac{R(1-D)^2}{2f_S}$$

where *R* is the equivalent load resistance, *d* is the duty ratio, and *f s* is the switching frequency.

Now, the value of *L*ic1 is calculated at the worst duty ratio of *d* min such that the converter operates in DICM even at really low duty ratio. At minimum duty ratio, i.e., the BLDC motor operating at 50 V (*V* dc min), the ability (*P* min) is given as 90 W (i.e., for constant torque, force power is proportional to speed).

B. Design of DC Link Capacitor (*C d*)

The design of the dc link capacitor is governed by the total amount of the second-order harmonic (lowest) current flowing in the capacitor and is derived as follows. For the PFC operation, the supply current (*is*) is in phase with the supply voltage (*v s*). Hence, the input power *P*in is given as

$$C_d = \frac{I_d}{2\omega\Delta V_{dc}}$$

Hence, the nearest possible value of dc link capacitor *C d* is selected as 2200 μ F.

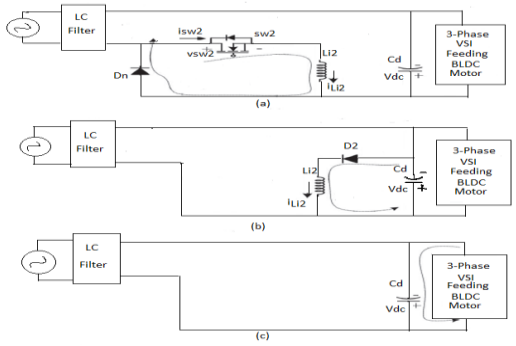

Fig. 3. Operation of the proposed converter in different modes (a)–(c) for a negative half cycle of supply voltage and (d) the associated waveforms. (a)Mode I. (b)Mode II. (c)Mode III.

The relation governing the voltage conversion ratio for a buck–boost converter is given as

$$d = \frac{V_{dc}}{V_{dc} + V_{in}}$$

The proposed converter is made for dc link voltage control from 50 V (*V* dc min) to 200 V (*V* dc max) with a nominal value (*V* dc des) of 100 V; hence, the minimum and the utmost duty ratio (*d* min and *d* max) corresponding to *V* dc min and *V* dc max are calculated as 0.2016 and 0.5025, respectively

*A. Design of Input Inductors (Li*1 *and Li*2*)*

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The value of inductance *L*ic1, to use in critical conduction mode in the buck–boost converter, is given as

$$L_{ic1} = \frac{R(1-d)^2}{2f_s}$$

where *R* is very same load resistance, *d* is the duty ratio, and *fs* is the switching frequency.

B. Design of DC Link Capacitor (*Cd*)

The design of the dc link capacitor is governed by the total amount of the second-order harmonic (lowest) current flowing in the capacitor and is derived as follows. For the PFC operation, the supply current (*is*) is in phase with the supply voltage (*Vs*). Hence, the input power *P*in is given as

$$P_{in} = \sqrt{2}\, V_s \sin(wt) * \sqrt{2}\, I_s \sin(wt)$$

For a maximum value of voltage ripple at the dc link capacitor, Sin(*ωt*) is taken as 1.

$$C_d = \frac{I_d}{2\omega \Delta V_{dc}}$$

Hence, the nearest possible value of dc link capacitor *Cd* is selected as 2200 μF.

C. Design of Input Filter (Lf and Cf)

A second-order low-pass *LC* filter can be used at the input side to absorb the larger order harmonics such it is not reflected in the supply current. The utmost value of filter capacitance is given as

$$C_{max} = \frac{I_{peak}}{\omega_L V_{peak}} \tan(\theta)$$

where *I* peak, *V* peak, *ωL*, and *θ* represent the peak value of supply current, peak value of supply voltage, line frequency in radians per second, and displacement angle between the supply voltage and supply current, respectively. Hence, a benefit of *Cf* is taken as 330 nF. Now, the value of inductor *Lf* is calculated as follows. The value of the filter inductor is created by considering the origin impedance (*Ls*) of 4%–5% of the bottom impedance.

Hence, the excess value of inductance required is given as

$$L_f = L_{Req} + L_s$$

V. CONTROL OF PFC BL BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE

The control of the PFC BL buck–boost converter-fed BLDC motor drive is classified into two parts as follows.

A. Control of Front-End PFC Converter: Voltage Follower Approach

The control of the front-end PFC converter generates the PWM pulses for the PFC converter switches (*Sw*1 and *Sw*2) for dc link voltage control with PFC operation at ac mains. An individual voltage control loop (voltage follower approach) is utilized for the PFC BL buck–boost converter operating in DICM. A reference dc link voltage ($V*$dc) is generated as

$$V_{dc}^* = k_v \omega^*$$

where *kv* and *ω*∗would be the motor's voltage constant and the reference speed, respectively.

VI. SIMULATED PERFORMANCE OF PROPOSED BLDC MOTOR DRIVE

In MATLAB/Simulink environment, using the Sim-Power-System tool box, proposed BLDC motor drive performance is simulated. The proposed drive performance is evaluated based on the performance of the BLDC motor and BL buck–boost converter and also from the power quality indices achieved at ac mains. For the proper functioning of the BLDC motor, the parameters of the BLDC motor such as

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speed (N), electromagnetic torque (*Te*), and stator current (*ia*) are analyzed. The PFC BL buck–boost converter parameters such as supply voltage (*Vs*), supply current (*is*), dc link voltage (*V*dc), inductor's currents (*i*Li1, *i*Li2), switch voltages (*V*sw1, *V*sw2) and switch currents (*i*sw1, *i*sw2) are evaluated.

Steady-State Performance

To confirm DICM operation of the BL buck–boost converter, the discontinuous inductor currents (*i*Li1 and *i*Li2) are achieved. The proposed BLDC motor drive performance at speed control by varying dc link voltage from 50 to 200 V is tabulated in Table III. The supply current harmonic spectra at rated and light load conditions, i.e., dc link voltages of 200 and 50 V, are shown in Fig. 7(a) and (b), respectively, which shows that the supply current THD obtained is within the IEC 61000-3-2 limits.

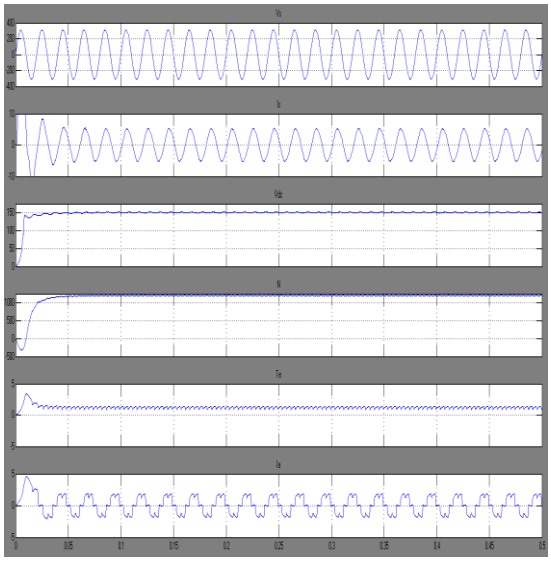
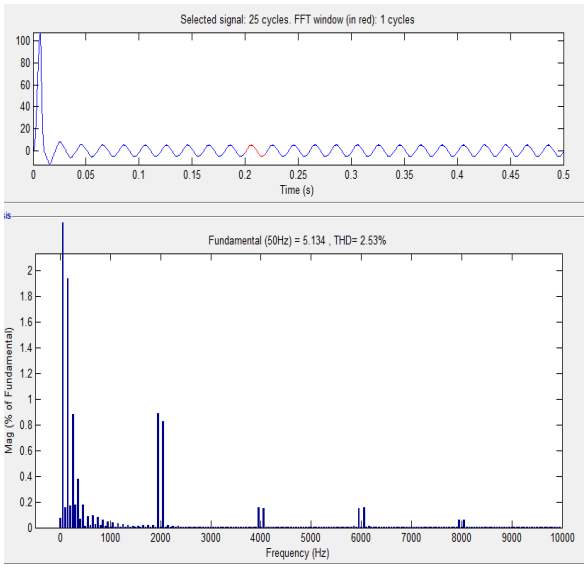


Fig. Steady-state performance of the proposed BLDC motor drive at rated conditions.



Vs	DPF	TH of Is(%)	PF	Is	CF
100	0.9933	1.65	0.99315	3.5855	1.414
120	0.9951	2.07	0.9948	2.926	1.414
140	0.9971	2.45	0.9968	2.438	1.414
160	09990	2.75	0.9987	2.124	1.414
180	0.9997	3.05	0.9993	1.874	1.414
240	0.989	4.28	0.998	1.399	1.414
260	0.9984	4.068	0.9973	1.2855	1.414

Fig. 7. Harmonic spectra of supply current at rated supply voltage and rated loading on BLDC motor for a dc link voltage of 240 V

Dynamic Performance of Proposed BLDC Motor Drive

The dynamic behavior of the proposed drive system during a starting at 50 V, step change in dc link voltage from 100 to 150 V, and supply voltage change from 270 to 170 V is shown in Fig. 8.

Performance Under Supply Voltage Variation

In practical supply conditions, the behavior of the proposed BLDC motor drive is demonstrated and also for supply voltages 90 to 270 V, the performance

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is evaluated. Table IV shows different power quality indices with variation in supply voltage. The supply current THD obtained is within the limits of IEC 61000-3-2. Fig. 9(a) and (b) shows the supply current harmonic spectra at ac mains at rated conditions of dc link voltage and load on the BLDC motor with supply voltage as 90 V and 270 V, respectively. For both the cases THD of supply current is within the limits which show an improved power quality operation at ac mains.

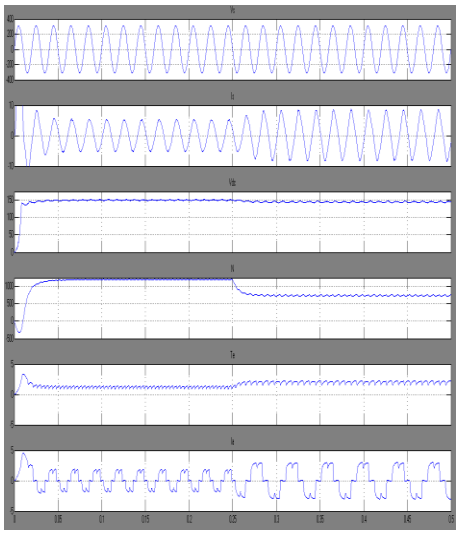


Fig. 8. Dynamic performance of proposed BLDC motor drive during (a) starting

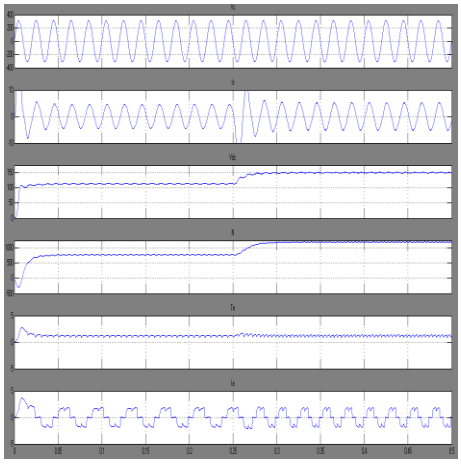


Fig. 8. Dynamic performance of proposed BLDC motor drive during (b) speed control

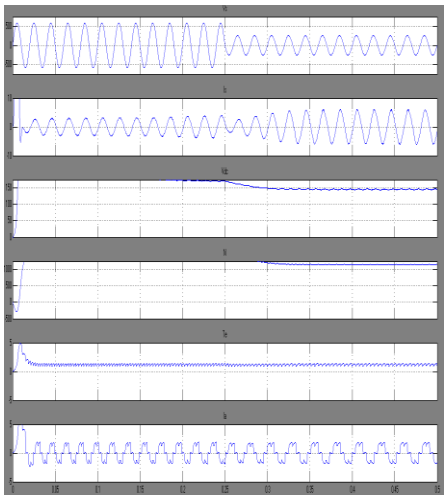
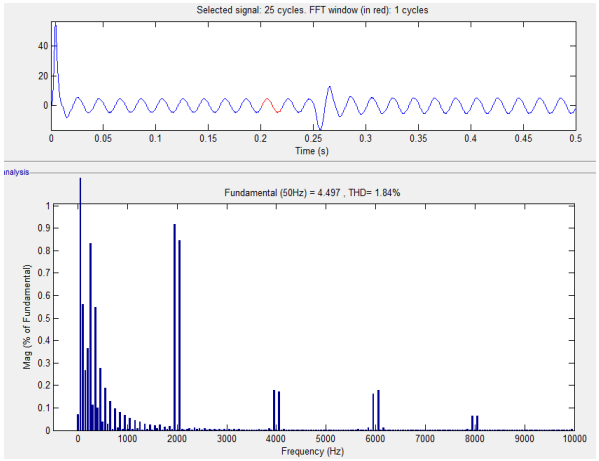


Fig. 8. Dynamic performance of proposed BLDC motor drive during (c) supply voltage variation at rated conditions.



Vdc	N	DPF	THD of Is	PF	Is
55	420	0.9855	6.73	0.983	0.4057
75	625	0.9917	5.62	0.991	0.5458
95	845	0.9946	5.1	0.993	0.6908
115	1055	0.9965	4.65	0.995	0.766

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135	1275	0.9978	4.43	0.9968	0.994
155	1480	0.9986	4.08	0.9979	1.148
165	1595	0.9989	3.93	0.9981	1.002

Fig. 9. Harmonic spectra of supply current at rated loading on BLDC motor with dc link voltage as 200 V and supply voltage as (a) 90 V and (b) 270

VII.CONCLUSION

A sincere effort is made to develop a novel PFC BL buck-boost converter for a BLDC motor drive using MATLAB Simulink. In this paper, the dc bus voltage is varied for speed control and VSI is operated at fundamental frequency to achieve electronically commutated BLDC motor to reduce switching losses in VSI. At ac mains, to achieve an inherent PFC, the BL buck-boost converter topology has been operated in Discontinuous Inductor Current Mode. The PMBLDCM speed has been identified to be proportional to the dc link voltage. Therefore, by controlling the dc link voltage, a smooth speed control has been achieved. The usage of the rate limiter in the reference dc link voltage has limited the motor current within the desired value at the time of transient conditions. In this proposed topology, a satisfactory performance for both speed control and supply voltage variation has been achieved. Moreover, the power quality indices are within the IEC 61000-3-2 limits. The proposed topology has achieved satisfactory performance which is useful for low power BLDC motor drive.

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