# DESIGN OF HIGH SPEED 128X 128 BIT VEDIC MULTIPLIER USING HIGH SPEED ADDER

Vengadapathiraj.M Rajendhiran.V Gururaj.M Vinoth Kannan.A Gomathi.R

**Abstract:In this paper describes about the design of 128-bit Vedic multiplier using ancient Vedic mathematics. Theproposed multiplier is designed to take two 128-bit inputs, and prescribed each 128-bit input into two 64-bit blocks this can be used to reduce the complexity of the design comparing to the other multiplication method used in digital signal processing and cryptographic algorithm Urdhva Tiryagbhyam method is used on these blocks and arranges the partial products in a way so they can be added using carry save adder and carry select adder and compared with ripple carry adder. The proposed architecture minimizes the combinational delay which makes more efficient than the ripple carry adder. Simulation is done in Xilinx 12.4 software using Verilog HDL.The Results show that proposed design is faster than other architectures of Vedic and non-Vedic multipliers. The combinational path delay for proposed system is 11.298ns which is more effective than RCA adder.**

**Keywords: Carry save adder, modified carry select adder carry select adder (CLA), Vedic Mathematics, and Urdhva Tiryagbhyam.**

## 1. INTRODUCTION

Multipliers play an essentialpart in today's digital signal processing and various other applications. With advances in technology, many scholars have tried and are trying to design multipliers which compromise either of the following design targets - high speed, low power consumption, symmetry of layout and hence less area or even combination of them in one multiplier thus making them suitable for numerous high speed, low power and compact VLSI execution.

There are number of multiplication algorithms proposed in literature which include array, booth, Wallacetree, modified booth and Vedic algorithms. It originate from the various proposed architectures in literature that Vedic multipliers are faster than non-Vedic multiplier architectures .Different architectures have been proposed in literature to improve the efficiency of multiplication using Vedic mathematics. These designs are based on unadventurous Vedic, Vedic using RCA, Vedic using addition tree structure and Vedic with CSA. Gupta proposed architecture for conservative Vedic multiplier. The problem of conservative Vedic architecture is that it works fine at 2 bit level but when we increase the order of multiplier, it becomes more complex. Pushpalata and Mehta proposed an enhanced architecture for Vedic multiplier.

In order to address the disadvantages with respect to speed of the above mentioned methods, explored a new approach to multiplier design based on ancient Vedic Mathematics. Vedic Mathematics is an ancient and eminent approach which acts as a foundation to solve several mathematical challenges encountered in the current day scenario. Vedic Mathematics existed in ancient India and was rediscovered by a popular mathematician, Sri Bharati Krishna Tirthaji [7]. He split Vedic mathematics into 16 simple sutras (formulae). These Sutras deal with Arithmetic, Algebra, and Geometry. Thesimplicity in the Vedic mathematics sutras paves way for its application in several prominent domains of engineering like Signal Processing, Control Engineering and VLSI [8]. In this paper a fast method forMultiplication based on ancient Indian Vedic mathematics is proposed which is quite different from the conventional method of multiplication like add and shift.

This paper describes the design of non-pipelined 128 bit Vedic multiplier. Section II describes ancient Vedic mathematics and the theory behind Urdhva-Triyagbhyam sutra. Section III describes the proposed design of non-pipelined Vedic multiplier. Section IVdescribes the results and comparisons of the proposed designs.



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Section V concludes the research work.

## II. VEDICMATHEMATICS

The word "Vedic" is derived from the word "Veda" which means the store-house of all knowledge. Vedic methods ideas can be directly applied to trigonometry, plain and spherical geometry, conics (both differential and essential), and applied mathematics of numerousvarieties. The charisma of Vedic mathematics lies in the fact that it reduces the cumbersome-looking calculations in conventional mathematics to a very modest one. This is so since the Vedic formulae are claimed to be based on the natural principles on which the human mind works.

Swami Bharati Krishna Tirtha(1884-1960), formerJagadguru Sankaracharya of Puri culled a set of 16 Sutras (aphorisms) and 13 Sub - Sutras (corollaries) from the Atharva Veda. He establishedapproaches and techniques for amplifying the principles contained in the aphorisms and their corollaries, and called it Vedic Mathematics [1].

### A. Urdhva-Triyagbhyam sutra

The multiplier is based on an algorithm Urdhva-Triyagbhyam of ancient Indian Vedic Mathematics. The Urdhva-Triyagbhyam sutra is basically vertically and crosswise. The Sanskrit words Urdhva stands for "vertical" and Triyagbhyam stands for "crosswise" [7]. These Sutras have been traditionally used for the multiplication of two numbers in the decimal number method. In this work, applying the similarconcepts to the binary number system. In this method the partial products are generated simultaneouslywhich itself reduces the delay makes this method fast. Consider two, three bit numbers A and B where A = a1a0 and B = b1b0 as shown in Figure 1. Firstly, the least significant bits are multiplied which gives the least significant bit of the product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added by, the product of LSB of multiplier thenfollowing higher bit of the multiplicand (crosswise). The sum gives second bit of the product and the carry is added in the output of next stage sum, which is obtained by processing the three bits with crosswise and vertical multiplication and addition to give the sum and carry. The sum is the conforming bit of the product and the carry is again added to the next stage multiplication and addition of two bits except the LSB. The similarprocessremains until the multiplication of the two MSBs to give the MSB of the product.

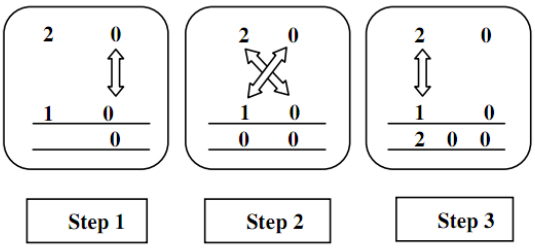


Figure1 Vertically and Crosswise Multiplication

## III. SUGGESTEDPROPOSALOFNONPIPELINED VEDIC MULTIPLIER

This paper describes design and construction of 128x128 Vedic multiplier is shown by using 2x2 Vedic multiplier is the building block. The approach applied for the design of 128x128 bit Urdhva-Triyagbhyam (UT) multiplier is to design a 2x2 bit Urdhva-Triyagbhyam multiplier as a basic building block in the preliminary stage of the work. This also gives chances for sectional design where smaller block can be used to design the bigger one and a hierarchy of design can be maintained. So the design complexity gets reduced for inputs of larger no of bits and modularity gets increased .This system gives auspicious result in terms of speed and power .This technique also provides a systematic structure .In the first stage of the project a 4 x 4 bit Urdhva-Triyagbhyam multiplier is designed using 2x2 bit Urdhva-Triyagbhyam multiplier as the central building block. Further 8x8 bitUrdhva-Triyagbhyam multiplier and 16x16 bit Urdhva-Triyagbhyam multiplier were designed, using 4x4 bit Urdhva-Triyagbhyam multiplier


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and 8x8 bit Urdhva-Triyagbhyam multiplier as the building blocks respectively. Next 32x32 bit Urdhva-Triyagbhyam multiplier and 64 x 64 bit Urdhva-Triyagbhyam multiplier were designed, using 16x16 bit Urdhva-Triyagbhyam multiplier and 32 x 32 bit Urdhva-Triyagbhyam multiplier as a basic building blocks respectively and finally 128x128 bit Vedic multiplier is done using 64x64 blocks as the basic building blocks for construction

**A. 4x4 bit Urdhva-Triyagbhyam Vedic multiplier**

Let A (multiplicand) and B (multiplier) are four bit numbers, A=a3a2a1a0 and B= b3b2b1b0.The output bits the multiplication result, y7y6y5y4y3y2y1y0. Partition the no. of bits in the inputs equally in two parts. Divide a and b into two parts, say “a3 a2” & “a1 a0” for A and “b3 b2” & “b1b0” for B. This is shown in the figure 2. We take two bits at a time and using fundamentals of Vedic multiplication and four 2x2 Vedic multipliers, the 4x4 bit Vedic multiplier can be obtained and it is shown in figure 4.

Consider the inputs a and b of 4 BIT each one. The lower two BITs of input a (a1-a0) are multiplied with the lower two BIT of b (b1-b0). This yields the 4 BIT result out of which lower 2 BITs are considered as the lower 2 BITs of the final result i.e. y[1:0] and the upper 2 BITs are considered as carry. The lower 2 BITs of a are multiplied with the upper 2 BITs of b, likewise the lower 2 BITs of bare multiplied with the upper 2 BITs of a and the result of this multiplication are added with the previous carry as shown in figure. Again this will produce altogether 4 BITs out of which lower 2 BITs are considered as the BITs of the final result i.e. y[3:2] and upper 3 BITs are the carry BITs which are added to the multiplication result of last step. The last step is to multiply the upper 2 BITs of both a and b and to add the previous carry. This will result in 4 BITs which are considered as the upper 4 BITs of the final result i.e. y [7:4].

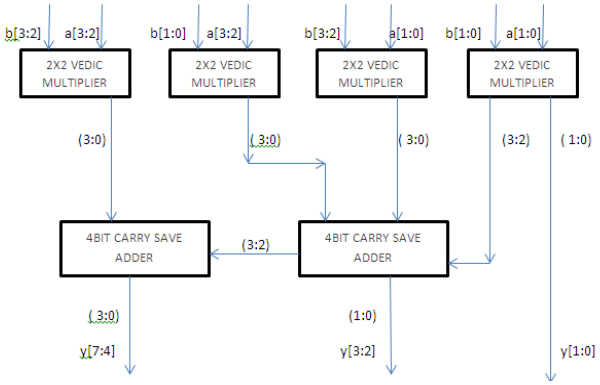


Figure.2 4x4 Vedic multiplication using csa

**B. 64x64 bit Urdhva-Triyagbhyam Vedic multiplier**

After the realization of 4x4 Vedic multiplier we will design 8x8 multiplier using the same methodapprovedabove. Further 16x16 bit Urdhva-Triyagbhyam multiplier and 32 x 32 bit Urdhva Tiryagbhyam multiplier stayed considered, using 8 x 8 bit Urdhva-Triyagbhyam multiplier and 16x16 bit Urdhva-Triyagbhyam multiplier as the building blocks correspondingly. Finally 64x64 bit multiplier is realized as shown in the figure 5. Here a and b are 64 bit input multiplicand and multiplier and y is the 128 bit multiplication resultant output.

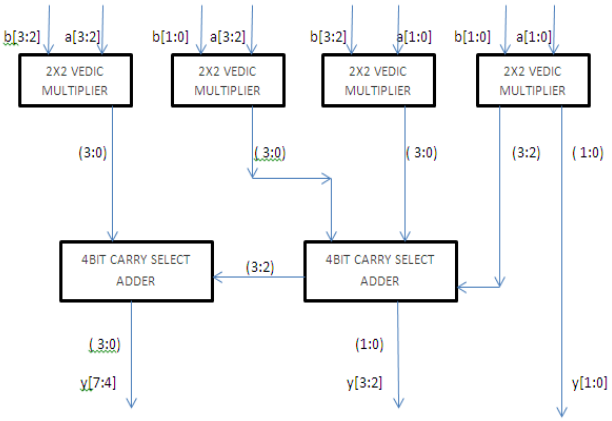




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Figure34x4 bit Vedic multiplication using csla

### C. 12x128 bit Urdhva-Triyagbhyam Vedic multiplier

After the realization of 4x4 Vedic multiplier we will design 8x8 multiplier using the same method approved above. Further 16x16 bit Urdhva-Triyagbhyam multiplier ,32 x 32 bit Urdhva-Triyagbhyam multiplier and 64x64 Urdhva-Triyagbhyam multiplierremained considered, using 8 x 8 bit Urdhva-Triyagbhyam multiplier and 16x16 bit Urdhva-Triyagbhyam multiplier as the building blocks correspondingly. Finally 128x128 bit multiplier is realized as shown in the figure 5. Here a and b are 64 bit input multiplicand and multiplier and y is the 128 bit multiplication resultant output.

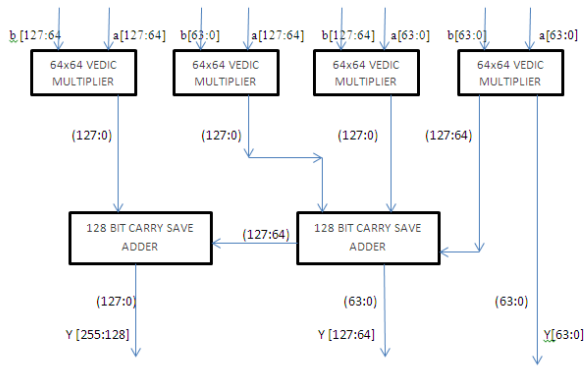


Figure4.1 proposed architecture of 128x128 bit Vedic multiplication using csa

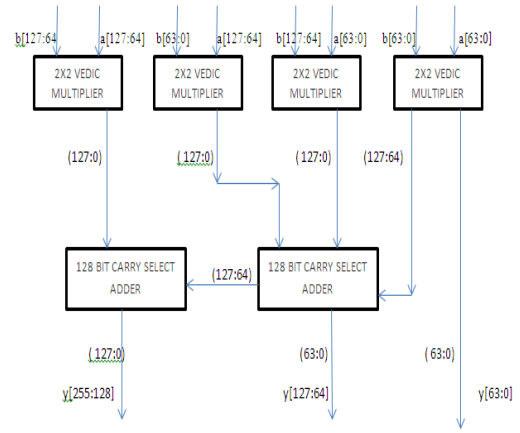


Figure4.2 proposed architecture of 128x128 bit Vedic multiplication using csla

## IV. IMPLEMENTATION RESULTS AND DISCUSSION

In these work, 4-bit, 8-bit, 16-bit, 32-bit, 64-bit and 128-bit Vedic multipliers(pipelined and non-pipelined) using "UrdhvaTiryagbhyam" Sutra is designed in Verilog. Logic synthesis and simulation was done using EDA (Electronic Design Automation) tool in Xilinx's 12.4. Simulation result of non-pipelined Vedic multipliers is shown in figure 5. The results showed that the proposed multiplier is are faster than the convolution method. The delay comparison of Vedic multiplier and non-vedic multiplier is shown in table below.

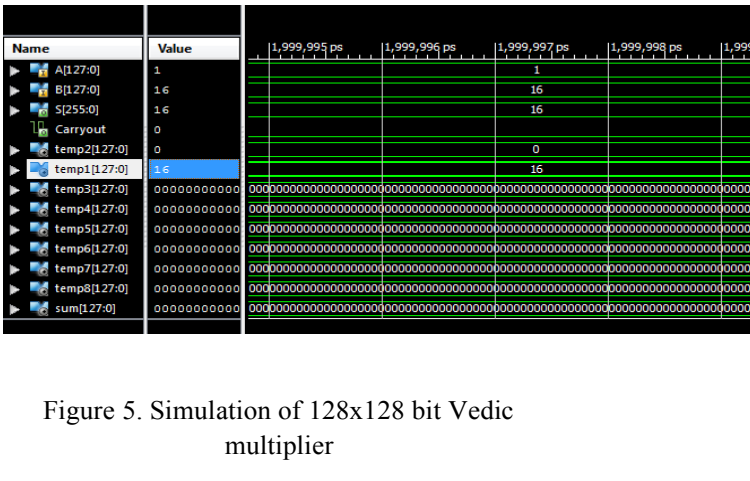


Figure 5. Simulation of 128x128 bit Vedic multiplier

The figuredisplays the simulation result of Vedic multiplier using carry save adder and carry select adder.

| Multiplier (bit) | Proposed Vedic multiplier using CSA | Proposed Vedic multiplier using CSLA | Non-pipelined Vedic multiplier using RCA | Modified booth multiplier |
|---|---|---|---|---|
| 8 bit | 5.287ns | 5.87ns | 10.685 ns | 15.256ns |
| 16 bit | 5.428ns | 5.98ns | 14.788 ns | 36.391ns |



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| | | | | |
|---|---|---|---|---|
| 32 bit | 5.9242 ns | 6.043ns | 19.442 ns | 74.432n s |
| 64 bit | 7.7272 ns | 8.01ns | 24.758 ns | 141.657 ns |
| 128 bit | 10.298 ns | 11.879 ns | 29.652 ns | 280.173 ns |

Table1. Comparison of combinational path delay between Vedic and non-vedic multiplier

## V. CONCLUSIONS

This proposed system an improved architecture for designing of a Vedic multiplier is reduced the Area. It consumes less power and also increases the speed of the system. In the previous architecture ripple carry adder used for adding partial products. In proposed designed architecture carry save adder and carry select adder becomes efficient in terms of combinational path delay. Furthermore the proposed design during the addition of partial products CSA,CSLA and modified CSLAis completelyused. The combinational path delay of suggested Vedic multiplier is10.298 ns and 11.879ns at 128-bit level. The table shows that the Vedic multiplier using carry save adder and carry select adder is faster than the other multipliers and also complexity gets reduced.

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