

Design of MUX using Deep Submicron Technology

K.Rajasri¹, M.Manikandan², D.Prabakaran³

Abstract— In this paper, a low leakage high speed domino circuit is proposed for MUX for register file in memory cell which has higher noise immunity and higher speed compared to other domino circuit. The technique which is utilized in this paper is based on current comparison domino which means the current of the pull-up network is compared with the reference current circuit. So delay and parasitic capacitance on the dynamic node is decreased. The reference current circuit is used to improve speed of the circuit. The leakage current is reduced by using footed transistor in diode configuration. Simulation result of the wide fan-in MUX designed using 22nm CMOS technology.

Index Terms— Domino logic, CCD domino circuit, leakage power, power consumption.

I. INTRODUCTION

Multiplexers, or MUX's, can be either digital circuits made from high speed logic gates used to switch digital or binary data or they can be analogue types using transistors, MOSFET's or relays to switch one of the voltage or current inputs through to a single output.

In electronics, a **multiplexer** (or **mux**) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth.

The rotary switch, also called a wafer switch as each layer of the switch is known as a wafer, is a mechanical device whose input is selected by rotating a shaft. In other words, the rotary switch is a manual switch that you can use to select individual data or signal lines simply by turning its inputs "ON" or "OFF". So how can we select each data input automatically using a digital device.

In digital electronics, multiplexers are also known as data selectors because they can "select" each input line, are constructed from individual Analogue Switches encased in a single IC package as opposed to the "mechanical" type

selectors such as normal conventional switches and relays.

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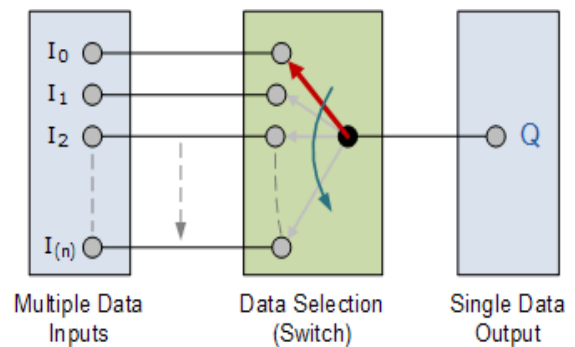


Fig.1 Basic Multiplexing Switching

They are used as one method of reducing the number of logic gates required in a circuit design or when a single data line or data bus is required to carry two or more different digital signals.

Generally, the selection of each input line in a multiplexer is controlled by an additional set of inputs called *control lines* and according to the binary condition of these control inputs, either "HIGH" or "LOW" the appropriate data input is connected directly to the output. Normally, a multiplexer has an even number of 2^N data input lines and a number of "control" inputs that correspond with the number of data inputs.

In this paper, we develop a new circuit for a MUX. The Current Comparison based Domino [CCD] technology is used. This domino circuit has high speed and consumes less power compared to other domino circuit. The performance CCD based MUX is compared to other domino circuit using 22nm Predictive Technology Model.

II. EXISTING SYSTEM

In the existing work the DFD(Diode Footed Domino) is designed. The DFD based MUX circuit is shown in Fig.2. In the evaluation phase, one of the RS signals goes high and allows the corresponding memory cell to evaluate the precharged bit line. Several dynamic bit lines can be combined to a single output by static NAND gates as shown in Fig.2. In this circuit, the excessive leakage of the evaluation network can cause logic failure during the read operation.

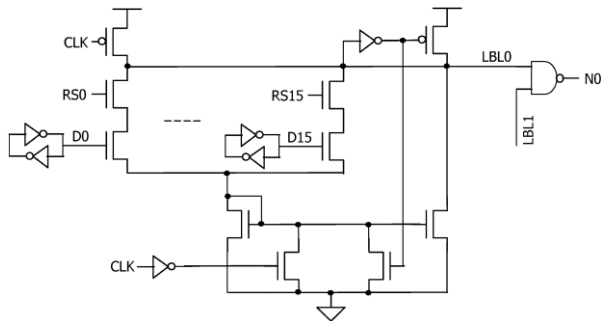


Fig.2 Diode-footed MUX in register file bit line.

In this technique, memory neither cells control the top transistors in the evaluation network through static NOR gates. The other inputs of the static NOR gates are connected to the intermediate nodes of the evaluation branches, which are charged high by the PMOS pull-up transistors controlled by the RS signals. Therefore, if RS is low, the gate-to-source voltage of the corresponding top NMOS transistor of the evaluation branch becomes (negative supply voltage), and thereby considerably reducing subthreshold leakage.

But this circuit has high leakage power and has high delay. To improve the noise immunity we proposed the CCD based MUX circuit. This circuit has superior performance compare to DFD circuit.

III. CIRCUIT DESIGN

High fan-in dynamic MUXs are commonly used in register files for implementation of bit-lines. In register files, because of the fairly small size of the memory, the bit-lines are implemented using wide domino MUX gates as shown in Fig.3. The row-select (RS) signals, provided by an address decoder, are applied to the top transistors in the evaluation network. The bottom transistors are connected to the memory cells.

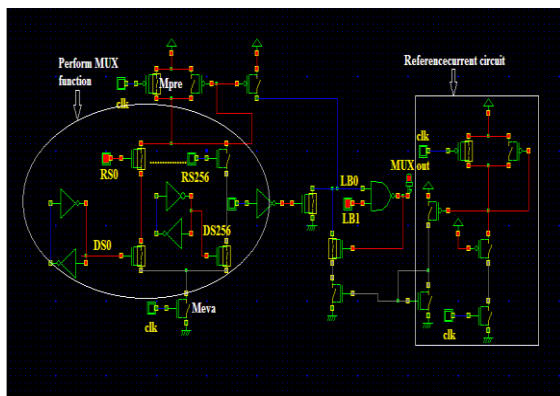


Fig.3 CCD based MUX in register file bit line.

A. Precharge Phase

Input signals and clock voltage are in high and low levels, respectively, [CLK = "0", CLKB = "1" and of the RS signal is high in Fig 3] in this phase. Therefore, the voltages of the dynamic node (Dyn) and node A have fallen to the low level by transistor Md and raise to the high level by transistor Ma, respectively. Hence, transistors Ma, Md, Me, and Mf are on and transistors M₁, M₂, and Mo are off. Also, the output voltage is raised to the high level by the output inverter. If

either of the RS signal not goes to the high, no data is selected in the memory cells. So we get output voltage as low level.

B. Evaluation Phase

In this phase, clock voltage is in the high level [CLK = "1", CLKB = "0" and RS= either "0" or "1" in Fig. 3] and input signals can be in the low level. Hence, transistors Ma and Md are off, transistor Mb, Mc, Mf, and Mo are on, and transistor Me can become on or off depending on input voltages. Thus, two states may occur. First, all of the input signals remain high. Second, at least one input falls to the low level. In the first state, a small amount of voltage is established across transistor Mb due to the leakage current. Although this leakage current is mirrored by transistor Mc, the keeper transistors of the second stage (Me and Mf) compensate this mirrored leakage current. It is clear that upsizing the transistor Mb and increasing the mirror ratio (M) increase the speed due to higher mirrored current at the expense of noise-immunity degradation. In the second state, when at least one conduction path exists, the pull-up current flow is raised and the voltage of node A is decreased to nonzero voltage, which is equal to gate-source voltage of the saturated transistor Mb.

This voltage is also equal to drain-source voltage of Mb and depends on size of Mb and its current. Increasing the pull-up current increases the mirrored current in transistor Mc, thus voltage of the dynamic node Dyn is charged to VDD, yielding discharging the voltage of the output node and turning off the main keeper transistor Me.

By this technique the contention current between the keeper transistor and the mirror transistor is mitigated. Timing diagram of 256-bit MUX based current comparison domino is shown below.

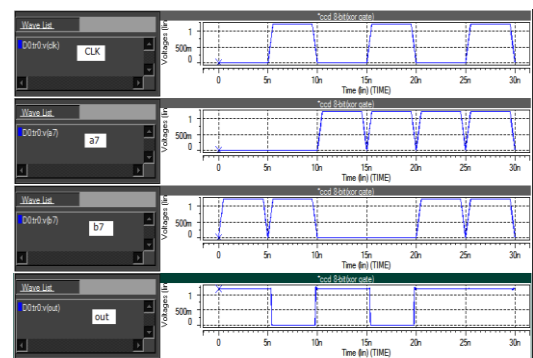


Fig.3 Timing Diagram

IV. SIMULATION RESULT

The simulations were performed using L=22nm technology along with the supply voltage V_{DD}=0.8V. In this paper a 64-bit wide fan-in gate for MUX is constructed using CCD based domino technique.. Since a single reference current structure can be shared among more than one domino logic circuits, the CCD technique is useful for constructing wide fan in circuits such as multiple bit adders, registers, multiplexers etc. This MUX circuit has much better noise margin, low

leakage current and low power consumption compared to other circuits designed using domino logic styles with traditional feedback keepers.

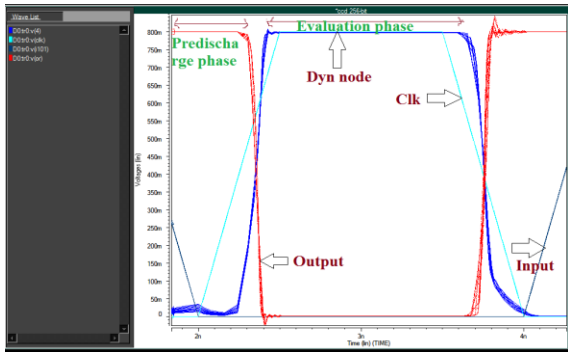


Fig.4 Simulation Result

The proposed technique has less delay(87ns) and require only 230uW power to perform operation. In Fig.5 delay of the proposed circuit is compared with other domino logic. The table 1 shows the CCD based MUX has less delay compared to other domino circuit.

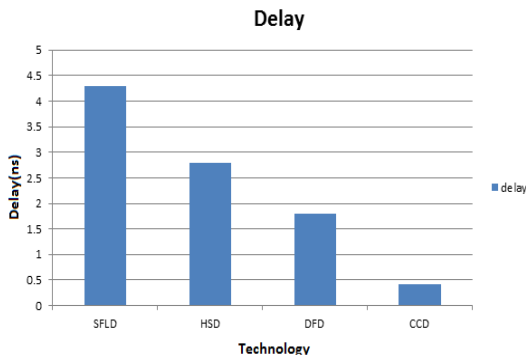


Fig.5 Delay Comparison

In Fig.6 power consumption of proposed circuit is compared with other domino logic circuit. The table 2 shows the CCD based MUX require less power to operate circuit. By using these comparison we can conclude that the proposed technique superior to other comparator circuit.

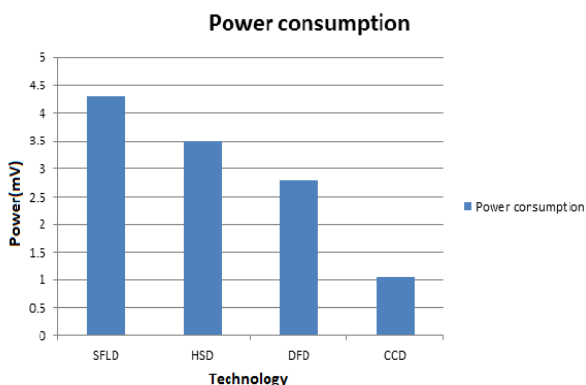


Fig.6 Power Consumption Comparison

Technique	Delay [ps]
SFLD	163.49
DFD	387.84
HSD	242.32
LCR	146.86
RSK	162.93
CCD	87.093

Table 1 Delay Comparison

Technique	Power Consumption[mW]
SFLD	10.568
HSD	5.053
LCR	8.746
RSK	6.47
DFD	7.577
CCD	1.997

Table 2. Power Consumption

V. CONCLUSION

As the technology scales down, the leakage current of the pull down evaluation network increases, especially in wide fan in dynamic gates. This will increase the power consumption and reduce the noise immunity. In this paper the performance of 256-bit MUX circuit designed using CCD domino circuit technique is analyzed in detail and its performance is compared with other MUX circuits. The 256-bit wide fan-in gate circuit is simulated using L=22nm technology along with supply voltage $V_{DD}=0.8V$. The experimental results shows that these wide fan in MUX gate circuits gives superior performance compared to wide fan-in gate circuits designed using conventional domino techniques.

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