Analysis and design of Transmission gate Ripple Carry Adder in Sub Threshold Region

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Abstract: Sub-threshold logic is the logic in which the power consumption is very low. This paper evaluates an 8bit ripple carry adder based on transmission gate in the sub-threshold region. The operating frequency of the ripple carry adder will be 15 MHz and the adder will be operate on the voltage varies from the 0.2vto 3.5v. In Transmission gate adder the circuit parameter like power, delay and power delay product after simulation is measured. The simulation is done with TANNER 14.1 tool in T-SPICE with 32nm technology in the voltage range varies from 2v to 3.5v and the operating frequency at 15 Mhz. The simulation result shows that the circuit will give good result at the operating voltage at 350mv.

Keywords: VLSI, CMOS circuit, Sub-threshold logic, TANNER Tool.

1. Introduction

Introduction: In modern processing **s**ystem adder play an important role. Main role of the adder is addition, subtraction, multiplication and division. Full adder is the basic block of the most of the circuits. For battery-operated portable applications such as cell phones, PDAs and laptop computers, as well as low-intensity applications such as distributed sensor networks, the need for power sensitive design has grown significantly. It has been shown that reducing the supply voltage is the most direct means of reducing dissipated power, and operating CMOS devices in the Sub-Threshold region is considered to be the most energy-efficient solution for low-performance applications [15]

For achievement of growing requirements for speed; the Adder is the basic block of Arithmetic Logic Units adders are the important blocks of signal processing for some modem architectures of high-speed Analog Digital Converters.[16] power consumption and signal delay are crucial to the design of high-performance very large scale integration (VLSI) circuits. A designer tries to save power, when designing a system**.** The growth of the electronics market has driven the VLSI industry towards

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very high integration density and system on chip designs. Moreover, with theexplosive growth the demand and popularity of portable electronics is driving designers to strive for smaller silicon area, higher speeds, longer battery life, and more reliability. The XOR-XNOR circuits are basic building blocks in various circuits' especially- Arithmetic circuits (adder and multipliers), Comparators, Parity checkers, Code converters etc. Basically There are three stages of development of the adders

- Firstly the mathematician solves the problem of implementation of the basic adder operation of the two bit via incarnate machine.
- Second focus will be on competition of the ad hoc procedures for generating faster sum of the two bits.
- Third focus in the area of optimization of the free variable i.e blocks width and driver size and otherwise determine structure.

2. Sub-threshold design

Design spectrum is a trade-off between power consumption and performance. The main aim of the design spectrum is low power rather than performance. So to search the solution of this problem the circuit is design in the sub-threshold region. In the sub-threshold region the supply voltage(V_{dd}) is less than the transistor threshold voltage(V_t). So in the sub-threshold region the voltage is very low. The motive of using the sub-threshold region is the ability to exploit the circuit leakage current as the operating drive current. In the sub-threshold region the the drain current I_d current is related to the supply voltage V_{dd} as shown in below equation

$$I_{ds}= I_o \ e^{\frac{Vgs-Vth}{V\text{tm}}} \ [1\text{-}e^{\frac{Vgs}{Vtm}}]$$

$$Io= \frac{W}{L} .\mu.C_{ox.}V^2{}_{tm}$$

$$V_{tm}=\frac{Kt}{q} \ (=26\text{mv at } 25^0 \text{ c})$$

By using this exponential relationship there is a reduction in power consumption is achieved but simultaneously increment in propagation delay is achieved. If a more power consumption reduction is achieved then delay increment can be neglected. This exponential equation is used in the following fields:

- Where power consumption is the prime factor rather than performance like wireless sensor node, RFID tags and medical equipment.
- Many burst mode application which require performance for the small interval of time.

3. Ripple Carry Full Adder circuits

Full adder circuit is the basic building block of the most of the circuits. Ripple carry adder is the adder in which the carry output of the previous state is directly connected with the carry input of the next state in a chain as shown below

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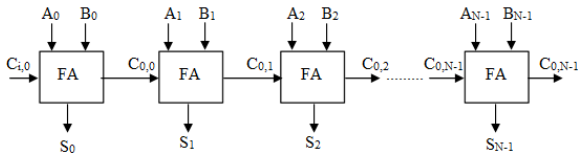

Fig. 1. N-bit Ripple Carry Full Adder

RCA is always preferred in terms of power and area when it appears to be fast enough for its intended purpose. RCA require the least amount of hardware of all adders, but they are the slowest[23].

3. Design of 8bit Ripple Carry Adder

3.1. 1bit CMOS full adder circuit

CMOS full adder circuit is the basic building block of all the circuits. All the design is compared with this circuit. The 1bit CMOS full adder is shown in figure 2. CMOS full adder circuit is consist of transistor. It has three input namely(A,B and C_{in}) and two output namely(Sum and Carry). The number of transistor used in the CMOS full adder is 28. The circuit is based on the CMOS logic and has equal rise and fall time.

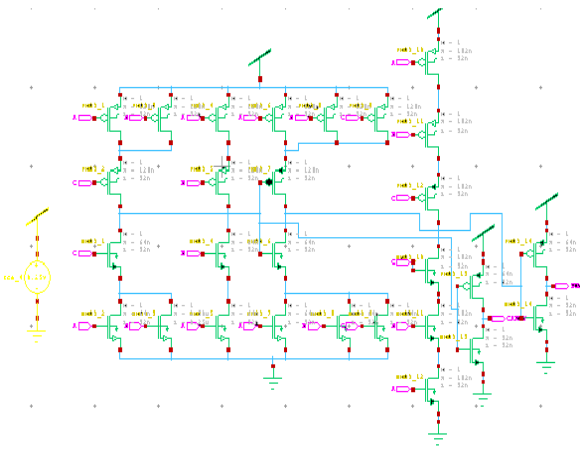

Fig.2. 1bit conventional CMOS RCA adder

The equations for Sum and Carry is shown

Sum= (A xor B) xor Cin

Carry=(A and B) + Cin(A xor B)

The CMOS circuit combines both PMOS (pull up) and NMOS (pull down) logic. Based on these equations the implementation of CMOS logic is done.

3.2 Transmission Function Full adder circuit

The Transmission function full adder circuit uses Ten Transistor in the circuit design.

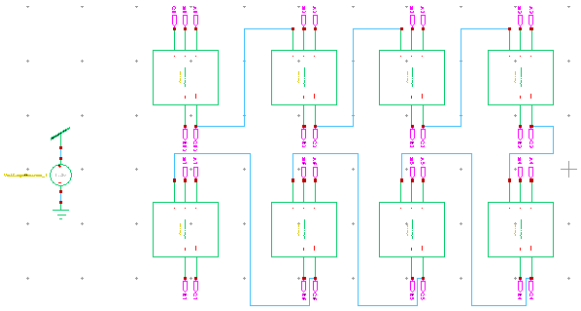

Fig.3. 8bit TFA Ripple Carry Adder

The 8bit TFA Ripple Carry Adder is shown in figure3

The TFA uses the following two equation

Sum= (A xor B) xor C_{in}

Carry=(A and B) + C_{in}(A xor B)

The area of TFA is less than conventional CMOS because uses of less number of Transistors. If

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area is less then the power consumption is also lower.

3.3 Transmission Gate Full adder circuit

Transmission gate full adder design uses 20 Transistors which are more than TFA but less than conventional CMOS. As accordingly area of TGA is less than conventional CMOS but slightly greater than TFA. The 8bit TGA Ripple carry adder is shown in figure4.

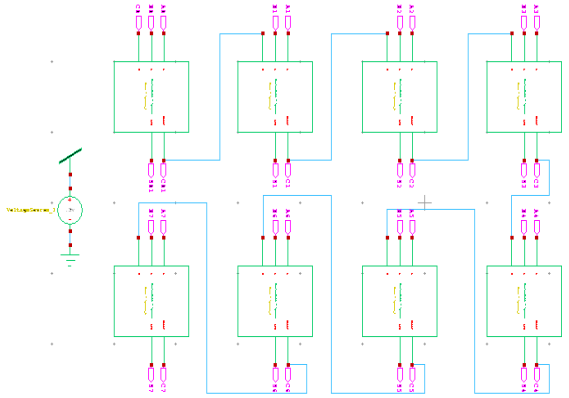

Fig.4. 8Bit TGA Ripple Carry Adder.

The Transmission gate adder has good power consumption and takes less area as compare to the conventional CMOS circuit.

4. Simulation Results of 8bit Ripple Carry Full Adder

8bit Ripple Carry Adder is designed by connecting 8different 1bit Ripple carry full adder one after another. Carry of the previous stage is connecting with the carry input of the next stage.

All the simulation is done with the help of the TANNER EDA 14.1 Tool in 32nm technology. The voltage will be vary from 2v to 3,5v and the operating frequency will be 15mhz.

Table1 Analysis of different 8bit RCA
Vdd=200mv, F=15mhz, Input= A7,B7,C6

Cell name	Power (pw)	Delay Sum (ns)	Delay Carry (ns)	PDP sum (aj)	PDP carry (aj)
CCMOS	0.1878	9.3188	0.8602	1.7500	0.1615
TFA	0.1985	2.2197	0.6951	0.4406	0.1379
TGA	0.2289	2.5332	0.7004	0.5798	0.1603

At the operating frequency 15mhz and the supply voltage V_{dd} 200mv the delay of TFA is much less than the CCMOS adder. the power delay product of the TFA is also less.

Table2. Analysis of different 8bit RCA
Vdd=250mv, F=15mhz, Input= A7,B7,C6

Cell name	Power (pw)	Delay Sum (ns)	Delay Carry (ns)	PDP sum (aj)	PDP Carry (aj)
CCMOS	0.2329	8.962	0.775	2.0872	0.1804
TFA	0.1908	1.797	0.689	0.3428	0.1314
TGA	0.2923	2.011	0.691	0.5878	0.2019

At the supply voltage 250mv and the operating frequency is 15mhz again the delay of the TFA is less as compare to the CCMOS and TGA. the power consumption is also lower of TGA. the delay and the power consumption of the CCMOS is higher in the voltage range 200mv and 250mv. The CCMOS RCA adder is the bench mark of all the three adders. All the calculations and the simulations are made with reference with this adder.

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Table3. Analysis of different 8bit RCA Vdd=300mv, F=15mhz, Input= A7,B7,C6

Cell name	Power (pw)	Delay Sum (ns)	Delay Carry (ns)	PDP sum (aj)	PDP carry (aj)
CCMOS	0.2752	5.228	0.729	1.4387	0.2006
TFA	0.2229	1.535	0.684	0.3421	0.1524
TGA	0.4039	1.678	0.686	0.6777	0.2770

At the supply voltage 300mv the delay of TFA is very low(1.535ns) as compare to the CCMOS(5.227ns). After that the delay of TGA is less in comparison of CCMOS but higher than the TFA.

Table4. Analysis of different 8bit RCA Vdd=350mv, F=15mhz, Input= A7,B7,C6

Cell name	Power (pw)	Delay Sum (ns)	Delay Carry (ns)	PDP sum (aj)	PDP carry (aj)
CCMOS	0.2329	3.3185	0.7056	0.7728	0.1643
TFA	0.2516	1.3373	0.6831	0.3364	0.1718
TGA	0.4039	1.4535	0.6840	0.5870	0.2762

At the supply voltage at 350mv the delay of TFA little larger than the TGA. but the delay of both adder(TFA and TGA) is much lower than CCMOS adder.

5. Conclusion

In this paper design of 8bit Ripple carry adder using Transmission gate is design and is simulated. The design os Adder is simulated in the TANNER EDA T-SPICE simulator in the 32nm technology. The delay, power and power delay product of the sum and carry is calculated. Simulation is done in the voltage range from 2mv to 3.5v and the operating frequency is 15mhz. The simulation result shows that the circuit give good result at the operating voltage 350mv.

6. Future Scope

The future scope of this paper can be on many points. Firstly the researcher can make 16bit ripple carry adder with the help of 8bit ripple carry adder. secondly the researcher can work on the delay of adder. Noise Margin is also a work of future reference. The power consumption and delay can be calculated with the help of some other techniques.

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