REDUCTION OF COMMON MODE VOLTAGE IN PWM RECTIFIER FED MOTOR DRIVES

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***Abstract*— Modern day switching devices such as IGBTs have fast switching nature leading to increase in Common Mode voltage and its adverse effects. Hence this paper mainly aims at reducing the magnitude of the Common Mode voltage. A Common-Mode (CM) filter based on different methods including LCL filter topology is proposed hereby. Firstly a CM filter makes use of the components of a line to line LCL filter, which is modified to address the CM voltage with minimal additional components. This leads to a compact filtering solution. Different variants of the filter topology are evaluated to establish the effectiveness of the proposed circuit. Secondly multi level inverter topology is examined to analyze the reduction in CM voltage as the number of levels increases. Further, addition of fourth leg to the bridge of a three phase inverter for the purpose of eliminating the CM voltage to ground is discussed. Hence CM voltage measurement on the motor side with the combination of PWM rectifier with LCL filter and fourth leg inverter topology is also presented. These results validate the effectiveness of the filter. Hence a solution for reducing the CM voltage which causes various several problems such as increase in shaft voltage and bearing current is discussed in this paper.**

Index Terms— Common mode voltage, LCL filter, Active front end rectifiers, parasitic capacitance, dv/dt filter, four leg inverter.

INTRODUCTION

Common Mode Voltage due to pulse width modulation in power converters introduces numerous problems in electrical system. Modern switching devices such as IGBT have fast turn-ON and turn-OFF time which results in high dv/dt being applied to the motor terminals. The high dv/dt switching pattern along with travelling wave effects of long cables applies stress on motor insulation, causing high ground currents which affects the motor bearings. The main cause for the occurrence of a shaft end to end voltage in an inverter-driven motor is the voltage-source PWM inverter employing the latest trench-gate insulated-gate bipolar transistors (IGBTs) which brings high-frequency common-mode and differential-mode voltages to the motor terminals.

These issues are exacerbated in PWM Active Front End (AFE) rectifier based motor drives when compared to one using a diode rectifier. Hence there are problems associated with IGBT technology based ASD with AFE rectifier using long cables. The common mode voltage due to such motor drive with AFE rectifier is a significant issue today. An integrated approach for filter design is discussed wherein the adverse effects of both AFE rectifier and the drive inverter are addressed on both common and differential mode basis[1,2]. The proposed topology addresses the problems of common mode voltage, common mode current and voltage doubling due to ASD. The design procedure for this proposed filter topology is discussed with simulation results that validate the effectiveness of the technology based Adjustable Speed Drives (ASD) using Active Front End (AFE) converter is widely used today[3]. Advantages of using IGBT based power converter are as following,

- High switching frequency.
- Smaller turn-ON and turn-OFF times, this reduces switching losses.
- Advance PWM techniques can be used for control.

Some of the applications require long cable between the motor and the power converter. In this case it has been observed that the voltage at the motor terminal doubles during switching transients as compared to voltage at inverter end. Also the high dv/dt at the inverter end due to faster turn-ON and turn-OFF times leads to problems [4, 5].

- Increased ground currents apart from voltage doubling at motor terminal.
- Bearing damage and insulation failure at load end.
- EMI/EMC concerns.

The DC bus energized using three phase diode bridge rectifiers injects lower order harmonics into grid. When this is not desirable along with the need for regenerative capabilities, AFE converter is a suitable alternative.

II. FILTER DESIGN OBJECTIVES

The design of ASD has to account the electrical noises introduced by modern PWM converters. This demands end to end solutions, wherein the electrical noises are minimized or eliminated with suitable filter topology as an integral part of the ASD system. The filter has to address

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both common mode and differential mode components. The design procedure needs to be independent of the load, but in most cases the load has to be considered to effectively mitigate the problem [6].

Further to address deleterious effects of CMV the presence of AFE converter has to be taken into account and retain the electrical noises generated within the system. This adds to the complexity of designing the filter. The filter design here address two aspects,

- Elimination of voltage doubling at motor terminal and minimizing CMC.
- To eliminate the CMV effects of AFE converter on the load and restrict the electrical switching noise within the ASD system.

III.MULTI LEVEL INVERTER TOPOLOGY

Multilevel voltage source inverters are a new generation of inverters. These are suitable for high power and high voltage applications due to reduced harmonic contents and low voltage stress across the load. Multilevel inverters have different voltage levels and switching states. They reduce the CMV which assists the generation of a high quality voltage and current.

The CMV for this purpose is measured as the voltage between the common-point in a three phase Y connected R-L load of the inverter and the electrical ground. Mathematically, this can be derived by considering the voltage at each phase of the inverter output with respect to the ground to be equal to the phase-to-a floating point voltage plus the floating point-ground voltage.

$$Vax=Van+Vnx$$

$$Vbx=Vbn+Vnx$$

$$Vcx=Vcn+Vnx$$

if the sum average of the three phase output voltage with respect to this assumed floating point under balanced operating condition is zero, then this floating point can be considered as the neutral point of the inventers' output. The voltage across the floating point neutral and ground can then be defined as the common-mode voltage Vn-x.

$$Vax+Vbx+Vcx=Van+Vbn+Vcn+3Vnx$$

$$Vnx= (Vax+Vbx+Vcx)/3$$

IV.FOUR LEG INVERTER TOPOLOGY

An alternative to expensive and large high impedance Common Mode filters is addition of fourth leg to the bridge of three phase inverter. This method helps to achieve an output neutral voltage which is equal to zero at all times thereby reducing the common mode potential produced my traditional modulation techniques. Hence LCL filter along with fourth leg inverter topology provides convincing solution for the reduction of CM voltage.

V.SIMULATION RESULTS

While simulating a multi level inverter to measure the common mode voltage, it is found that the common mode voltage is reduced to 81 volts. This accounts for 54% of the output voltage. With further increase in the number of levels the common mode voltage goes on decreasing. But in this method the increase in number of devices for each level is high when compared to the reduction in common mode voltage. Hence usage of LCL filter topology is found to be more effective in reducing the common mode voltage.

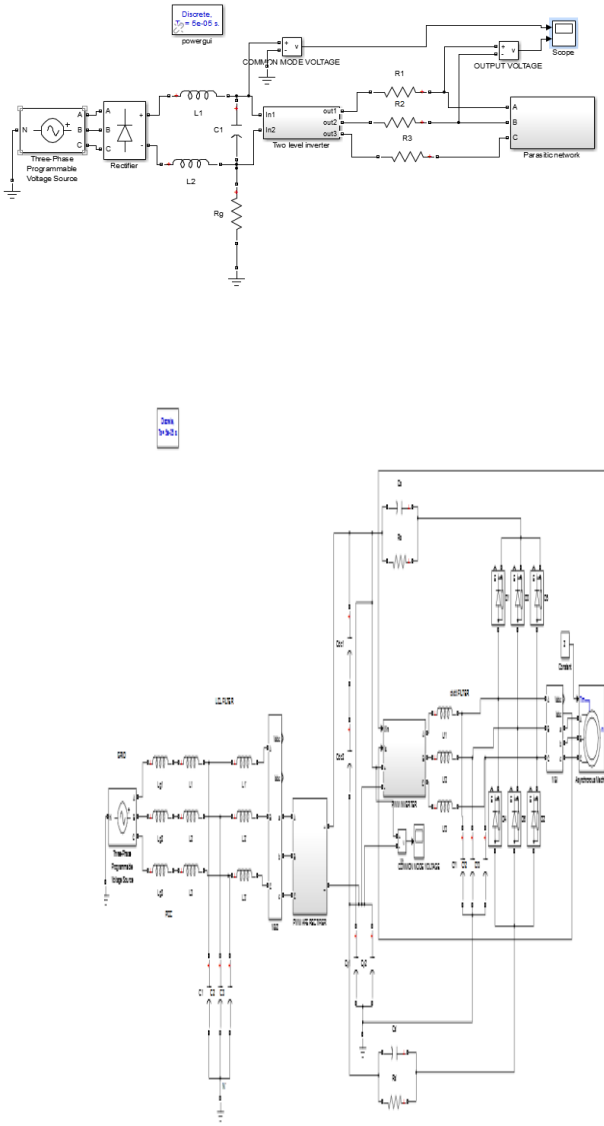

Fig 1.Schematics of an active front end motor drive with integrated LCL and DC bus common mode filter for grid and dv/dt filter at inverters terminal for motor.

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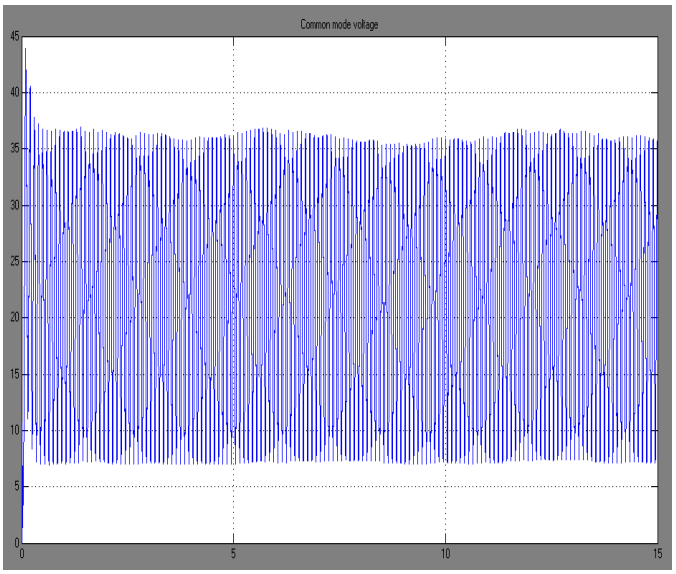

Fig.2 Reduction in Common mode voltage using an LCL filter topology

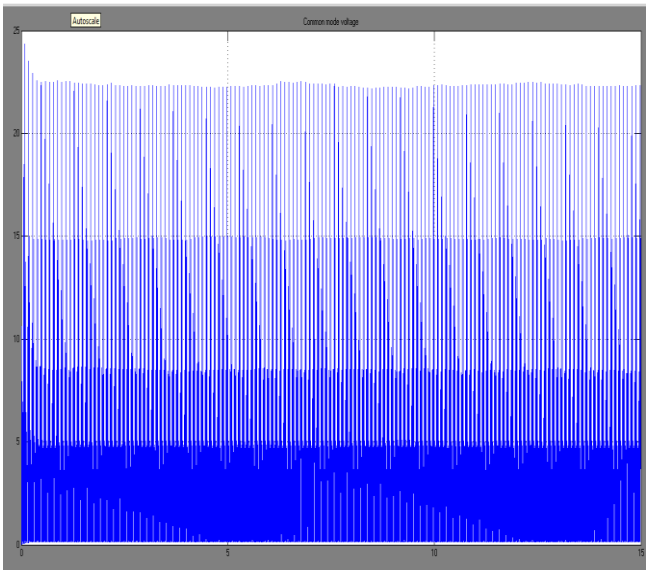

Fig.5 Reduction in Common mode voltage using an LCL filter & four leg inverter topology.

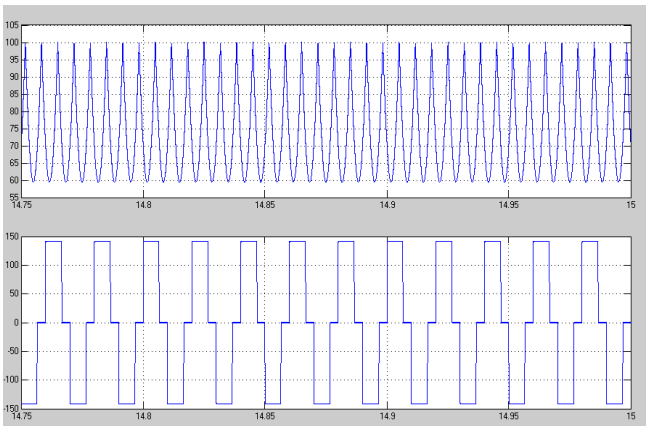

Fig. 3: Measurement of common mode voltage in two level inverter configuration

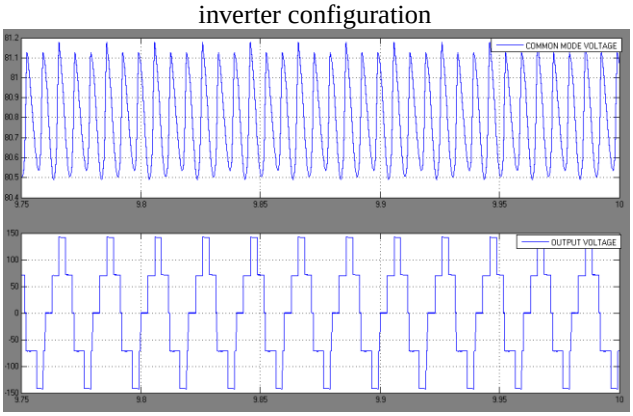

Fig. 4: Measurement of common mode voltage in multi level inverter configuration

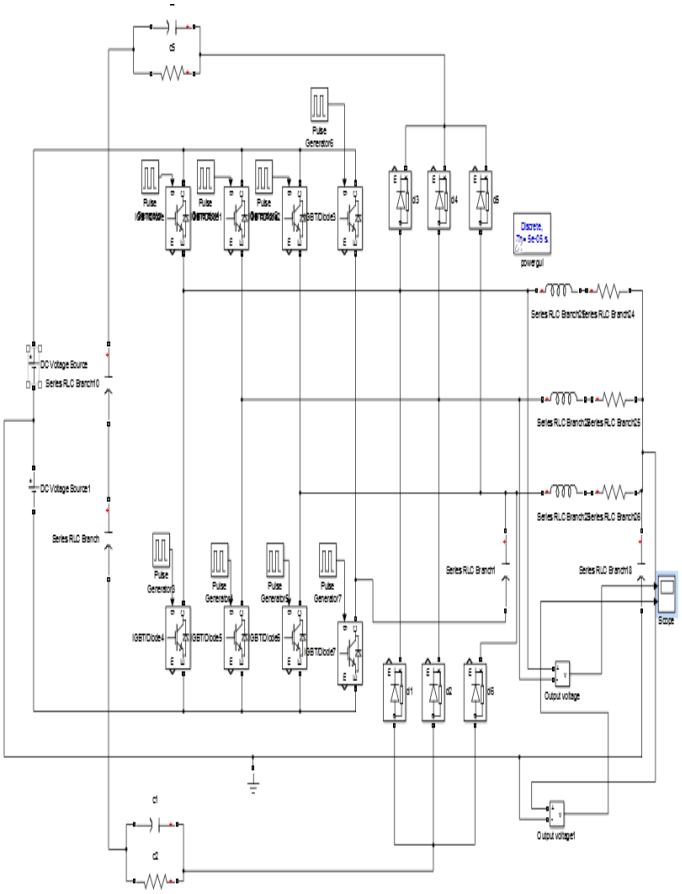

Fig.6 Incorporation of fourth leg inverter topology to reduce the CM Voltage.

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TABLE I: CM VOLTAGE IN VARIOUS METHODS EMPLOYED

Method	CM voltage
Three phase inverter fed induction motor drive	100volts
Multi level inverter fed induction motor drive	81 volts
Three phase inverter fed induction motor drive with LCL filter topology	36 volts
Three phase inverter fed induction motor drive with LCL filter & four leg inverter topology.	22 volts

V.CONCLUSION

The overall filter design procedure to address the CM voltages is outlined for a PWM rectifier-based ASD. Analysis of the filter with capacitors is discussed based on the CM equivalent circuit. The CM dc-bus filter restrains the high-frequency CM voltage, due to the PWM rectifier, from affecting the load. Variants of the filter topology are evaluated to check the effectiveness of the proposed solution. As the number of levels in the inverter increases the CM voltage is found to decrease. But the addition of components in each level is more comparing the other CM filter methods. Alternatively the addition of fourth leg to the three phase of the inverter helps to reduce the CM voltage considerably.This work can be extended to the selection of appropriate PWM methods in drives that have low CMV requirements.

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