PV PANEL WITH CIDBI (COUPLED INDUCTANCE DOUBLE BOOST TOPOLOGY) DC-AC INVERTER

Mr.Thivyamoorthy.S[1] ,Mrs.Bharanigha[2]

***Abstract*--In this paper the design and the control of an individual PV panel dc-ac converter based on a double coupled inductors boost topology are discussed. Also, the operation principle of the proposed inverter is discussed and the gain from DC to AC is deduced in detail. The main attribute of the CIDBI topology is the fact that it generates an AC output voltage larger than the dc input one, depending on the instantaneous duty cycle and turn ratio of the coupled inductor as well. This paper points out that the gain is proportional to the duty cycle approximately when the duty cycle is around 0.5.**

Index terms—Boost converter, CIDBI topology, grid connected, pv panel.

I. INTRODUCTION

The main purpose of this work is the optimal integration of photovoltaic energy resources in existing electrical distribution systems.In a conventional PV system many PV modules are connected in series to obtain a dc voltage suitable for ac utility line voltage. In series configuration, mismatch conditions could affect the PV system performance causing a lack of producible power. Usually in small-size applications the PV systems are affected by partial shading due to architectural and/or environmental issues. As a result, the total output power generated from the PV array decreases greatly, i.e. the efficiency of the generating electricity is lower.

To overcome this defect, a micro-inverter photovoltaic module system(MPMS) has been proposed.In this system, an AC module composed of a small power dc-ac utility interactive inverter is mounted on each individual PV module. Generally, the features of MPMS are small volume, flexible and that the maximum power pointdecrease the manufacturing and installation costs and raise the generating efficiency of the PV.

Generally, the features of MPMS are small volume, flexible and that the maximum power point tracking (MPPT) can control independly. So MPMS can decrease the manufacturing and installation costs and raise the generating efficiency of the PV. Here the AC module inverter should be of small volume, high efficiency and low cost.

Various approaches based on distributed dc-dc converters [1] or micro-inverter [2]-[4] have been proposed to address these issues by increasing power conversion. For lower DC voltage PV generating electricity, the existing technology mainly has the following two kinds: the single stage inverter generating AC utility line voltage by raising voltage transformer, another is two stage circuits, a dc-dc converter as font stage is used to get the sufficient DC-bus voltage for generating AC utility line voltage from the end stage inverter. In the former, the primary current of the transformer is larger so the switching loss is larger and the transformer itself produce power loss, hence, this system's efficiency is low too due to its two stage conversion. Besides, these two kinds of strategy result into big bulk. As a consequence they are not fit to MPMS.

Many works are aimed at single stage inverter without transformer, for example, the works [5], [6] present the double boost inverter which is composed of the two boost circuits in parallel. However, when the input DC voltage is much lower, i.ee duty cycle is too large, the performance of the boost converter can discount. In order to satisfy the above requirements for an AC module inverter, the CIDBI topology is introduced. The proposed CIDBI topology inherits the merits of the conventional double boost circuit such as high efficiency and high reliability.

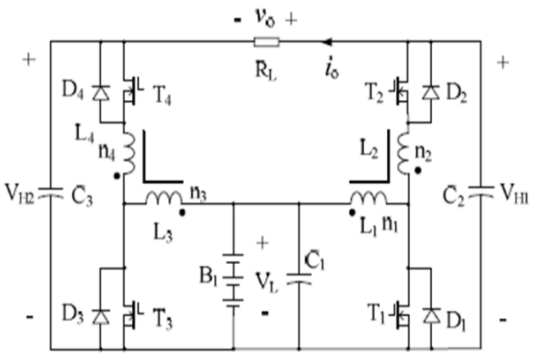

Fig 1. Proposed CIDBI topology

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II. CIDBI AND THE PRINCIPLE OF OPERATION

A. CIDBI TOPOLOGY

It is well known that the current of inverter can operate in quad quadrants, but the boost converter cannot satisfy this requirement. To solve this problem, the two coupled inductor-double boost converters should be connected in parallel as shown in fig 1. The load RL cross between the two outputs.

Fig 1. Shows that there is a DC source B_1, L_1 and L_2 commonly use a magnetic core, while L_3 and L_4 use another, so the two coupled inductors are constructed. One boost circuit consists of L_1, L_2, C_2 switches T_1, T_2 and their body diodes D_1, D_2, theother consists of L_3, L_4, C_3, switches T_3, T_4 and their body diodes D_3, D_4. It is clear that the right circuit and the left one represents dc-dc converters. These converters produce a dc-biased sine wave output, so that each source only produces a unipolar voltage. The modulation of each converter is 180 out of phase with the other, which maximizes the voltage excursion across the load. The load is connected differently across the load, with respect to ground, the differential dc voltage across the load is zero. The generating bipolar voltage at output is solved by push-pull arrangement. The driving signal for T_1 is the same as T_4, while the driving signal for T_2 is same as T_3, and the driving signals for T_1 and T_2 are 180 out of phase with the other. If SPWM is applied to CIDBI, we can get the following expressions:

$$V_{H1}= V_m \sin \omega t + V_{dc} \quad (1)$$

$$V_{H2}= -V_m \sin \omega t + V_{dc} \quad (2)$$

$$V_o=V_{H1} - V_{H2} = 2 V_m \sin \omega t \quad (3)$$

Where V_{DC} is a dc bias voltage at each end of the load, with respect to ground, V_m is AC output voltage magnitude added to V_{DC}.

From the expression (3), the AC output voltage can be got between the two outputs of boost circuits when in linear modulation area.

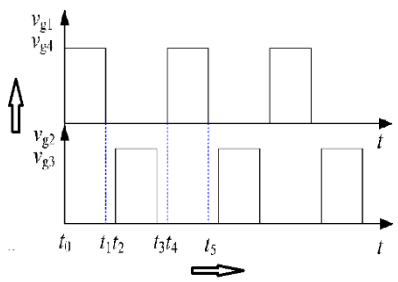

Fig 2. Timing diagram of the driving signal

B. Principle of operation of CIDBI

L_1 and L_2 are made in the same magnetic core to construct coupled inductor; we can define L_1 as primary winding, L_2 as secondary winding, L_1 has n_1 turns and L_2 has n_2 turns, L_3 and L_4 are the same as L_1 and L_2. The time scheme of driving signals are arranged in fig 2. V_{g1}, V_{g2}, V_{g3}, and V_{g4} are the driving signals assigned to T_1, T_2, T_3 and T_4 respectively. The deadtime may not be set for the switches T_1-T_4. However the delay time including switching ON and OFF exists in fact; hence, the deadtime is all the same presented in fig 2. Combined with the timing diagram in fig 2. The four operation modes within positive half period of ac output can be got.

1 [t_o-t_1]: The equivalent circuit is shown in fig. 3(a) where the driving signals V_g1 and V_g4 are high level, while V_{g2} and V_{g3} are low level; therefore the switches T_2 and T_3 are ON, and the currents i_{L1} and i_{L3} transmit from D_2 and D_3 to corresponding T_1 and T_4 respectively

2 [t_1-t_2]: fig 3(b) shows the operation circuit. In this period, v_{g1}-v_{g4} are low level; due to that, the current through inductor cannot reverse, i_{l1} and i_{L3} transmit to D_2 and D_3 respectively, to freewheel.

3 [t_2-t_3]: During this time interval, the equivalent circuit corresponds to fig. 3(c); V_{g1} and V_{g4} are low level, and V_{g2} and V_{g3} are high level. Although the current of the inductor cannot suddenly change direction, i_L1 and i_L3 are selected as MOSFET, its channel can conduct counter current, which helps to raise efficiency.

4 [t_3-t_4]: the equivalent circuit corresponds to fig. 3(d). where, V_{g1}-V_{g4} are all low level, and hence all switches are OFF. Although the current of the inductor cannot flow reversely, i_{L1} and i_{L3} still freewheel through D_2 and D_3, respectively. It's equivalent circuit is the same as that in [t_1-t_2].

5 After t_4, the operation states repeat.

The above is the operation principle when in the positive ac period, while negative half ac period is symmetric.

As shown in fig 3, it is concluded that the CIDBI's operation principle is the same as that of the dual-boost single stage dc/ac converter, which is discussed in [15] and [16]. The difference between the CIDBI and the configuration in the work [15], [16] mainly locates their boost inductor, the inductor in [15] and [16] is constructed by single winding, while the inductor in the CIDBI circuit is the coupled inductor composed of two windings. Just so, it makes the gain from input to o

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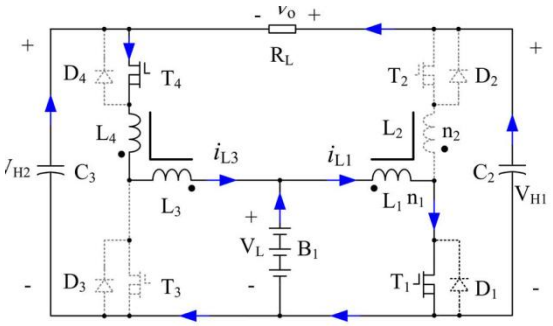

Fig 3 (a)

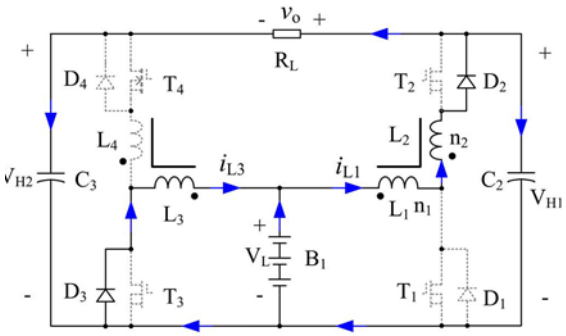

Fig 3 (b)

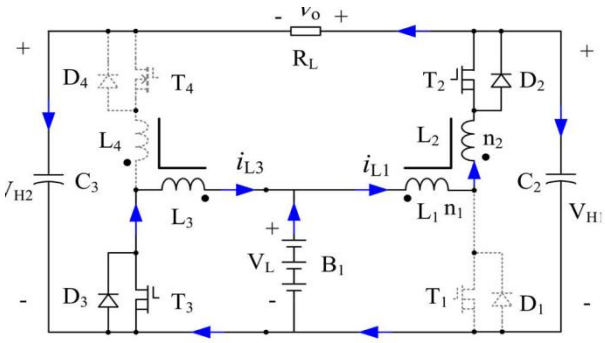

Fig 3 (c)

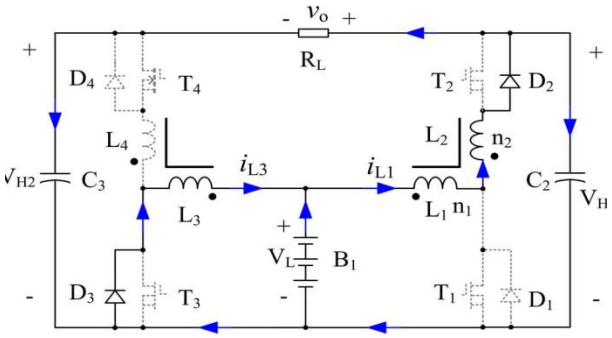

Fig 3 (d)

III. CONTROL STRATEGY

A. Duty cycle of coupled inductor boost circuit

We consider the right half boost circuit, we can define duty cycle and turns ratio N as follows:

$$D = \frac{T_{ON}}{T_{ON}+T_{OFF}} \qquad (4)$$

$$N = \frac{n_2}{n_1} \qquad (5)$$

Where, T_{ON} is switching ON time duration for T_1, at the same time, switching OFF time duration for D_2. While T_{OFF} is switching OFF time duration for T_1, and switching ON time for D_2.

Considering the aforementioned operation model analysis, volt-second product balancing can be applied to the inductor L_1 and L_2, the following expression:

$$\frac{V_L T_{ON}}{n_1} = \frac{(V_{H1}-V_L)T_{OFF}}{n_1+n_2} \qquad (6)$$

From (4), (5) and (6), the duty cycle D can be calculated in the following;

$$D = \frac{V_{H1}-V_L}{n_1+n_2} \qquad (7)$$

The duty cycle is as follows:

$$D = \frac{V_{H1}-V_L}{V_{H1}} \qquad (8)$$

Compared to the conventional calculation expression (8), there is an additional variable N to decide the duty cycle D in (7). As a consequence, the design of this kind of circuit is more flexible, especially when applied to lower dc-bus voltage situation. Based on (7), if the input and output voltages are determined, that is to say, the input-output voltage gain is settled, we can get relationship curve about D and N, as shown in fig 4. It is clear that the duty cycle D can decrease correspondingly when the turns ratio increases. In regard to the left half boost circuit, the situation is same. This is just the reason why the proposed CIDBI can be more appropriate to much lower dc-bus source, where we can choose the turn ratio N first to get the appropriate duty cycle D in order to meet the best PV power generation performance.

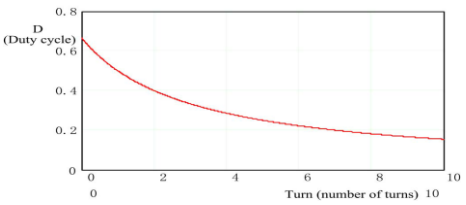

Fig 4 duty cycle versus no of turns

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B. Gain of CIDBI

As boost converter is concerned, its average voltage gain is as the following expression when it works in CCM:

$$V_O=V_{H1}-V_{H2}=V_L\frac{(1+N)(2D-1)}{(1-D)D} \quad (9)$$

As to CIDBI, if letting $V_{g1}=V_{g4}$ and $V_{g2}=V_{g3}$, the phase difference between v_{g1} and v_{g2} is 180° in electric angular based on its operation principle, we can get its output voltage as follows:

$$\frac{Vo}{V_L}=\frac{(1+N)(2D-1)}{(1-D)D} \quad (10)$$

Assuming that N is 4, the curves for the voltage gain versus D are drawn in fig 5. The voltage gain varies linearly approximately when the duty cycle D ranges from 0.3 to 0.7, i.e. the duty cycle is varied around 0.5, and$V_o$will be an AC voltage at the output terminal of CIDBI, if using SPWM

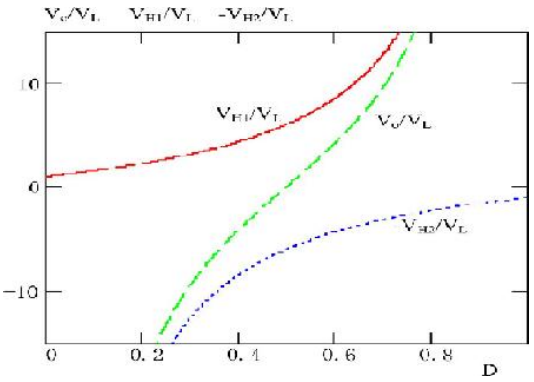

Fig 5 DC gain charactestic

C. PWM – Based control

If pwm is applied to CIDBI shown in fig 1, the duty cycle should follow the following the following equation according to symmetrical sampling rules:

$$D=\frac{1}{2}(1+M\sin(\omega t)) \quad (11)$$

Where, M is defined as modulation ratio. It must be noted that the modulation M cannot be designed too large, otherwise the duty cycle will exceed the maximum linear modulation scope.

In order to control the switches to modulate ac output voltage, the logic block diagram for PWM is shown in fig 6. As shown in fig 6, the logic method is the same as full bridge, V_{carry} is the triangle carrier waveform, V_{reg} is the sinusoidal modulation wave. Inputting this two signal to the input terminal of the PWM comparator, the output signal is shaved by driving circuit as switching signals, which are sent to switches according to fig 2. Here the design parameters are given as follows:

Dc input voltage is 25v, ac output voltage is 80v, the coupled inductor $L_1=L_3=95$ µH, their turns ratio choosen to be 4, and the output capacitor $C_2=C_3=4.4$ µF. Thus the gate driving signal is shown in fig 7.

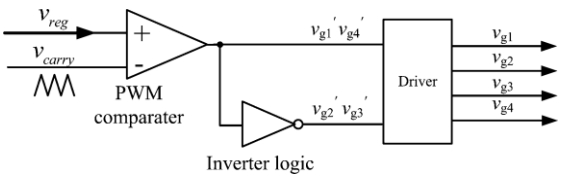

Fig 6. Logic block diagram for PWM

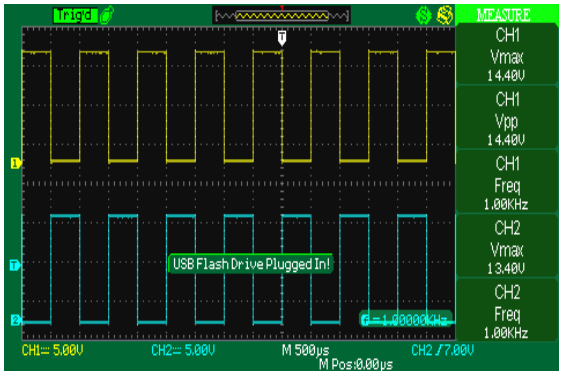

Fig 7. Gate signal.

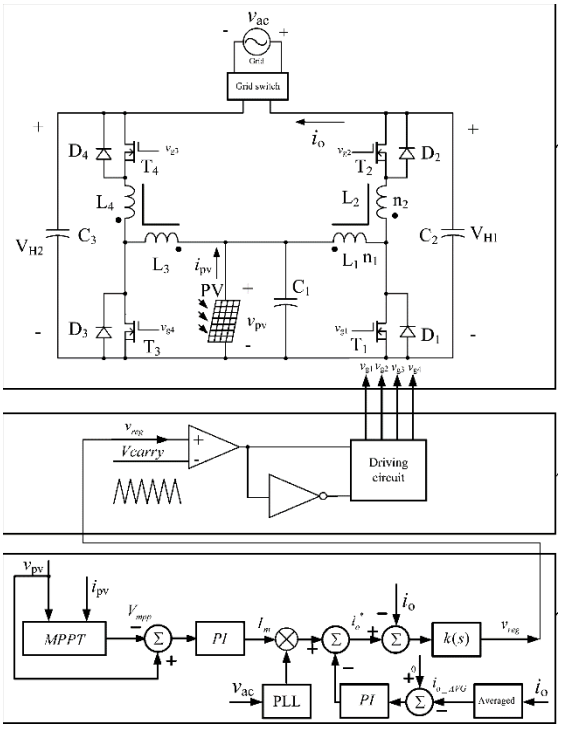

Fig 8. Schematic diagram for PV grid power

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IV.SIMULATION OUTPUT

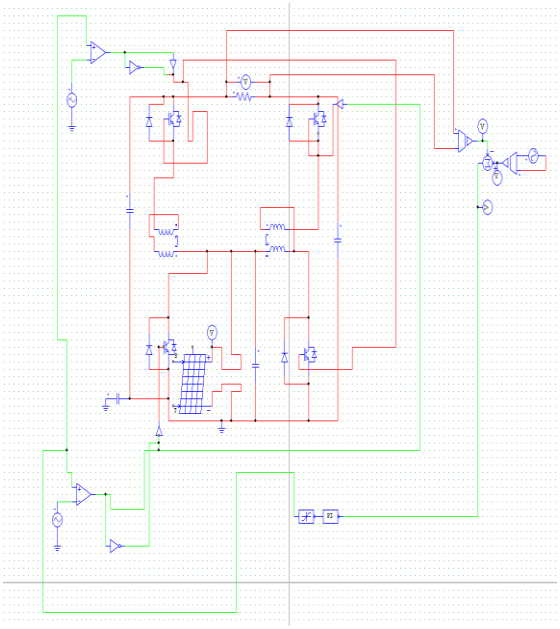

Fig 9. Simulation circuit

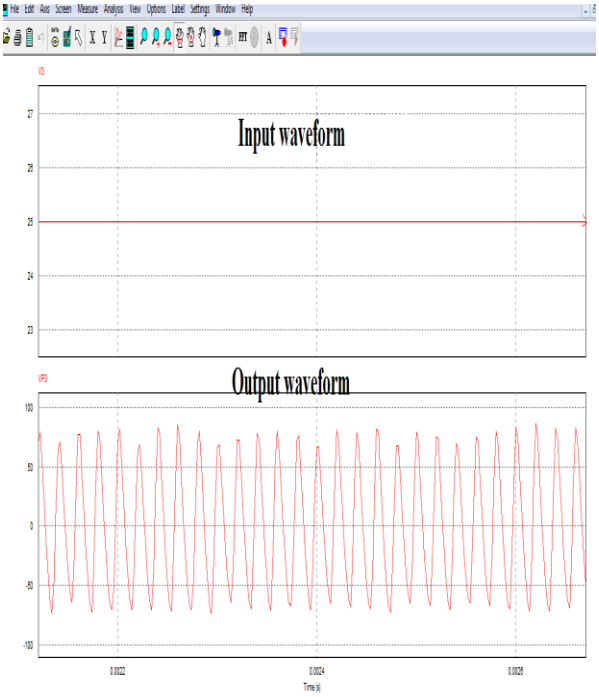

Fig 10. Output waveform

Aspower converter, and is used to implement singe-power stage grid generation, design parameters are the same as the aforementioned simulation parameters. Switches chooses 50 khz. Digital control also contains phase locked loop (PLL) control, MPPT, and anti-isolated island protection. MPPT is achieved by perturb & observe method (P & O) algorithm. The efficiency of CIDBI is more than 97.5%, the total harmonic distortion is less than 3%, and the power factor correction is not less than 0.99.

VI. CONCLUSION

This paper proposes the CIDBI topology, which is of simple structure and can generate an AC output voltage than the dc input one, depending not only on the instantaneous duty cycle but also on the number of turns of the coupled inductor and circuit is proposed.

V. EXPERIMENTAL RESULTS

Fig 8. Shows that the block scheme of CIDBI applied to MPMS, which is mainly composed of parts 1-3: part 1 is the CIDBI, part 2 is the PWM comparator, part 3 is the PV controller. A PV module is chosen as the input source. In this system, the proposed CIDBI is selected

The main features of the CIDBI are: 1) the volume is small and the control is simple; 2) the transmission efficiency is much higher due to topology based on boost converter; 3) the distortion caused from zero-crossing point is neglected because of an AC output plus dc bias.

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THIVYAMOORTHY.S Author. Received B.E. degree in Electrical & Electronics in Sri Sai Ram ENGG college and pursuing Master of Technology in Power Electronics & Drives at B.S.Abdurrahman university, vandalur, Chennai.

BHARANIGHA.V .is working as an Assistant professor in the Department of Electrical & Electronics at B.S. Adbur Rahman University. Her area of interest is in Converters, controlsystems , electrical machines. She attended many National and International level conference

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