A Single-Phase 21-Level Inverter with Reduced Switching Devices ACMLI for Different PWM Techniques

Pushpendra kaurav, Praveen bansal

Abstract— **Multilevel inverter is a power electronic device and that is become more or more popularize over the years in high-voltage high-power applications. Multilevel inverters have unique structure which makes it possible to reach high voltages with less harmonic content and lower EMI. The harmonic content of the output voltage waveform decreases as the number of output voltage increases. This paper presents a 21-level multi-level inverter with Asymmetrical cascaded MLI topology. This proposed multilevel inverter topology here is implemented in single-phase with different pulse width modulation (PWM) techniques, which requires less number of components, and gate drive circuit as compared to other multilevel inverters. A multicarrier PWM technique is used for multilevel inverter topology to generate 21-level output phase voltage. Finally simulation results of a 21-level multi-level inverter topology are carried out using MATLAB/Simulink R2013a software version.**

Index Terms— **Multi-level inverter (MLIs), Asymmetrical cascaded Voltage (ACMLI) topology and PWM techniques.**

I. INTRODUCTION

Multi-level power conversion is used to provide more than two voltage level to achieve smoother and less distorted dc to ac power conversion and it can generate a multiple-step voltage waveform with less distortion, less switching frequency and higher efficiency. Multilevel inverters have become more popular over the years in high-power high-voltage applications. Whereas conventional two level inverter have some limitations in high-power high-voltage applications due to switching losses and power ratings [1-3]. Multi-level inverter offers several advantages over two-level inverter: it improves the output voltage waveform, reduced (dv/dt) voltage stress on the load and also reduces electromagnetic interference problems, but it has some disadvantages when the number of voltage levels increases such as; complex PWM controlling method, voltage balancing problems are introduced and higher number of semiconductor switches are required. Each switch requires a separate gate driver circuit, therefore increasing the complexity and size of the overall circuit. For this problem, lower voltage rated switches can be used in multi-level inverter instead of higher number of semiconductor switches which can be used to minimized cost of the semiconductor switches as compared to two level inverters [4].

There are different conventional multi-level inverters topology mainly classified as Diode clamped multilevel inverter (DCMLI) [5], Flying capacitor inverter (FCMLI), cascaded H-bridge multilevel inverter (CHBMLI). In 1981 a three level diode clamped multilevel inverter schemes proposed by nabae [6]. The flying capacitor inverter structure is similar to that of diode clamped inverter but the main difference is that instead of clamping diodes, flying capacitors are used.

The control method of cascaded H Bridge multilevel is more convenient than other multilevel inverter because it doesn't have any clamping diode and flying capacitor. Cascaded multilevel inverter reaches higher reliability [7]. The cascaded inverter is used for large automotive electric drives. However, the requirement of more number of switches and separate dc source for each cell becomes a problem especially at higher level. Cascaded h-bridge multilevel inverter consists of separate dc links for each h-bridge cell so it is easily controllable. Cascaded h-bridge multilevel inverter has some drawback that by increasing the number of voltage levels numbers of switching devices given by 2(N+1) also increase [8].

This paper proposes a 21-level multi-level inverter with ACMIL topology which requires less number of switches and gate driver circuits as compared to conventional multilevel inverters. The proposed multilevel inverter topology [9] here is implemented in single-phase with different PWM techniques. The pulse-width modulation (PWM) control is the most efficient technique of controlling output voltage within the inverters. The carrier based PWM schemes used for multilevel inverters is the most efficient method, realized by the intersection of a modulating signal with triangular carrier waveform. The paper tries to prove that ACMIL topology is better than conventional multilevel inverters topology in terms of their number of components and THD.

II. PROPOSED TOPOLOGY

A single DC supply to output voltages two level 0 and V. It is used two switches S1 and S2. If switch S1 is ON, output voltage are V and switch S2 is ON output voltage are zero. Switches S1 and S2 are OFF simultaneously to avoid the occurrence of short circuit across the DC supply.

A three-phase asymmetrical n-level reduced devices cascading inverter shown in Fig.1 In this circuit, the DC-bus

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voltage is split into each cell. Which are connected in series and desired number of level can be achieved by series connection of switch.

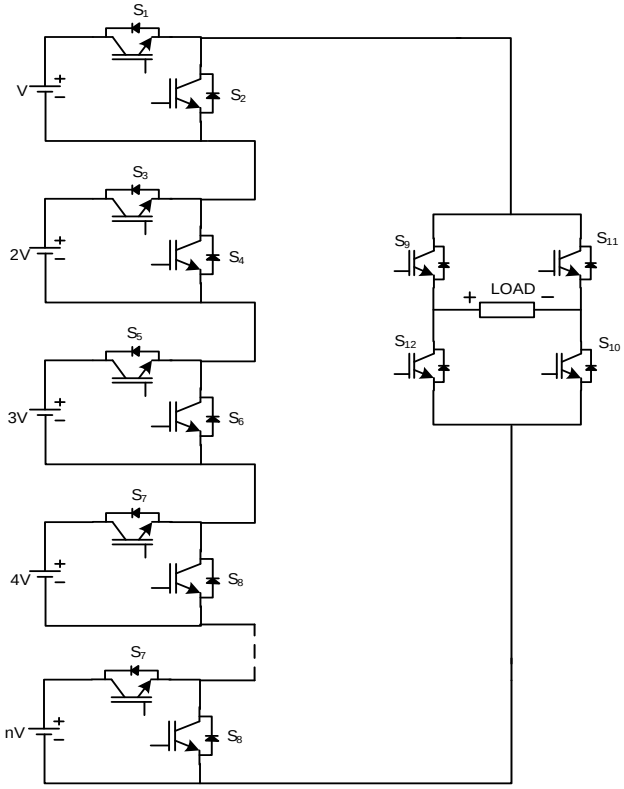

Fig.1 Proposed n-level asymmetrical reduced device cascaded MLI

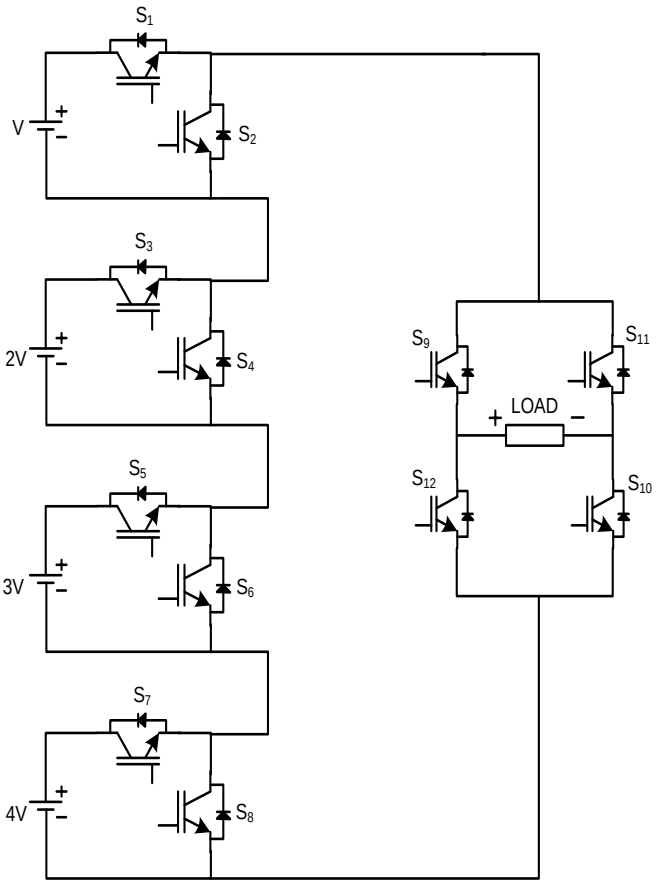

Fig.2 Proposed single-phase asymmetrical cascade 21-level inverter for line to ground voltages

The proposed ACMLI topology for 21-level inverter requires twelve semiconductor switches and four isolated dc sources shown in Fig 2 [9] which separates output voltage in two parts. One part is called level generation part (left side) and is responsible for level generating in positive polarity & negative polarity. The other part is called polarity generation part (right side) and is responsible for generating the polarity of the output voltage. This topology combines the two parts (left part and right part) to generate the multi-level output voltage waveform.

The main purpose of this proposed ACMLI topology is to control the EMI, minimize the total harmonic distortion with different PWM techniques and it also minimizes power semiconductor switches than conventional multilevel inverter. For a conventional single-phase 21-level inverter, it uses 40 switches, whereas the proposed topology uses only 12 switches.

Here proposed topology is also used for three-phase MLI with the same principle. The proposed topology is a symmetrical topology because all the values of all voltage sources are equal. Therefore, it does not have voltage-unbalancing due to fixed dc voltage values. In comparison with a cascade h-bridge inverter topology, proposed topology requires only one-third of isolated power supplies used in a cascade-type inverter [10]. The operation of the proposed topology has been discussed in detail and has been verified with the help of simulations [11].

A. OPERTION FOR THE PROPOSED TOPOLOGY

Operation of the proposed 21-level MLI with asymmetrical cascaded topology can be easily explained with the help of fig. 2 and table I. When switches S1, S3, S5 and S7 are turned "on" the output voltage will be "10Vdc" (i.e., level +10). The output voltage will be "9Vdc" (i.e., level +9) when switches S2, S3, S5 and S7 are turned "on". When S1, S4, S5 and S7 switches are turned "on" the output voltage will be "8Vdc" (i.e., level +8). When switches S2, S4, S5 and S7 are turned on the output voltage will be "7Vdc" (i.e., level +7). When switches S1, S3, S5 and S8 are turned "on" the output voltage will be "6Vdc" (i.e., level +6). The output voltage will be "5Vdc" (i.e., level +5) when switches S1, S4, S6 and S7 are turned "on". When S2, S4, S6 and S7 switches are turned "on" the output voltage will be "4Vdc" (i.e., level +4). When switches S1, S3, S6 and S8 are turned on the output voltage will be "3Vdc" (i.e., level +3). The output voltage will be "2Vdc" (i.e., level +2) when switches S2, S3, S6 and S8 are turned "on". When S1, S4, S6 and S8 switches are turned "on" the output voltage will be "Vdc" (i.e., level +1). When switches S2, S4, S6 and S8 are turned "on" the output voltage is zero (i.e., level 0). Switches S9, S10, S11 and S12 are used for a complementary pair. When S10 and S11 are turned "on" together, positive half cycle (level; +1, +2, +3, and +4) can be generated and when S9 and S12 are turned "on" together, negative half cycle (level; -1, -2, -3, and -4) can be generated across load.

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TABLE.I

VOLTAGE LEVEL	SWITCHING STATE												OUTPUT VOLTAGE
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	
+10	1	0	1	0	1	0	1	0	1	1	0	0	10V
+9	0	1	1	0	1	0	1	0	1	1	0	0	9V
+8	1	0	0	1	1	0	1	0	1	1	0	0	8V
+7	0	1	0	1	1	0	1	0	1	1	0	0	7V
+6	1	0	1	0	1	0	0	1	1	1	0	0	6V
+5	1	0	0	1	0	1	1	0	1	1	0	0	5V
+4	0	1	0	1	0	1	1	0	1	1	0	0	4V
+3	1	0	1	0	0	1	0	1	1	1	0	0	3V
+2	0	1	1	0	0	1	0	1	1	1	0	0	2V
+1	1	0	0	1	0	1	0	1	1	1	0	0	V
0	0	1	0	1	0	1	0	1	1	1	0	0	0
-1	1	0	0	1	0	1	0	1	0	0	1	1	-V
-2	0	1	1	0	0	1	0	1	0	0	1	1	-2V
-3	1	0	1	0	0	1	0	1	0	0	1	1	-3V
-4	0	1	0	1	0	1	1	0	0	0	1	1	-4V
-5	1	0	0	1	0	1	1	0	0	0	1	1	-5V
-6	1	0	1	0	1	0	0	1	0	0	1	1	-6V
-7	0	1	0	1	1	0	1	0	0	0	1	1	-7V
-8	1	0	0	1	1	0	1	0	0	0	1	1	-8V
-9	0	1	1	0	1	0	1	0	0	0	1	1	-9V
-10	1	0	1	0	1	0	1	0	0	0	1	1	-10V

B. Mode Of Operation

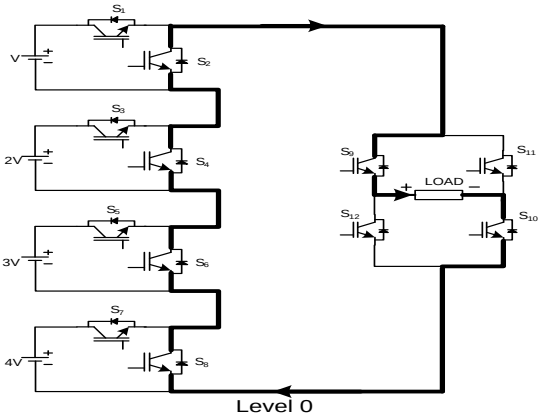

Fig (a)

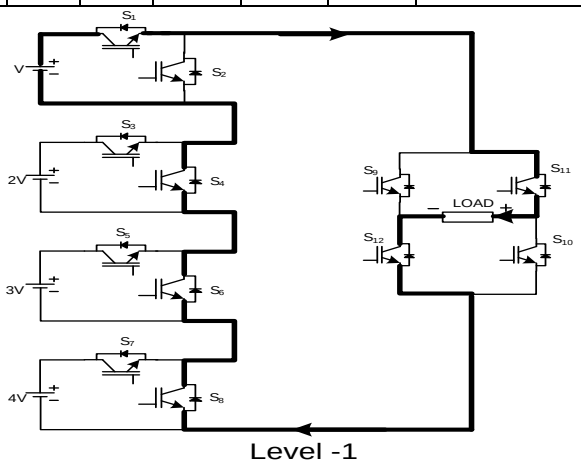

Fig (c)

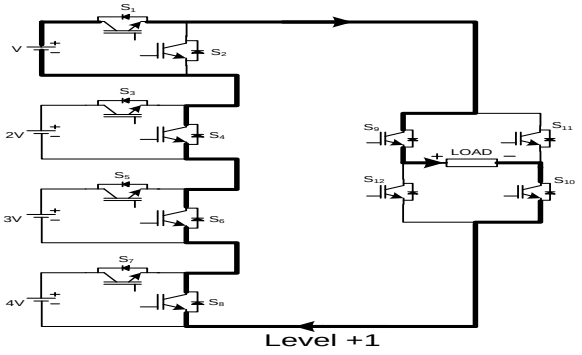

Fig (b)

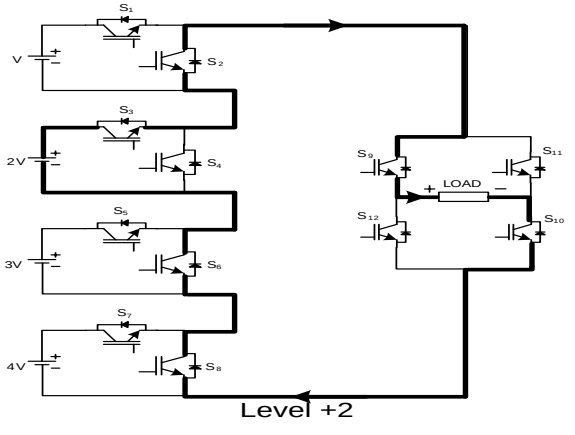

Fig (d)

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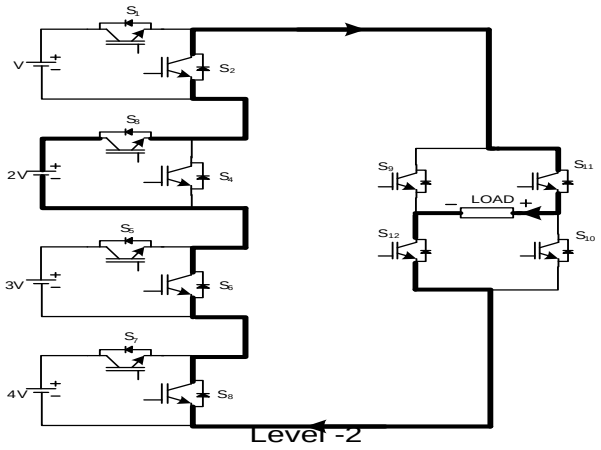


Fig (e)

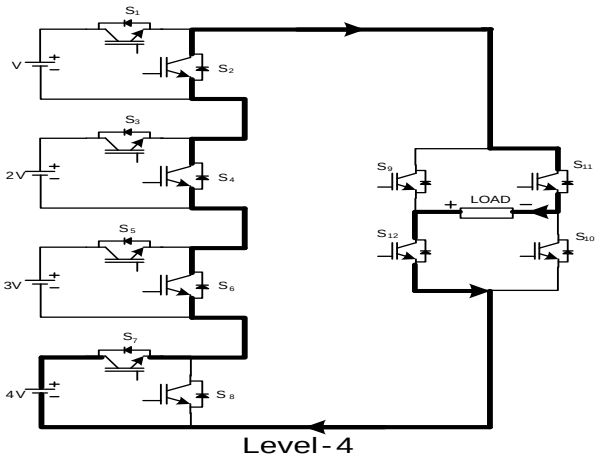


Fig (h)

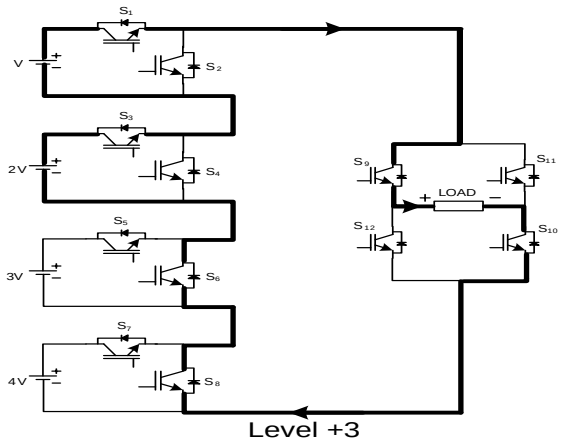


Fig (f)

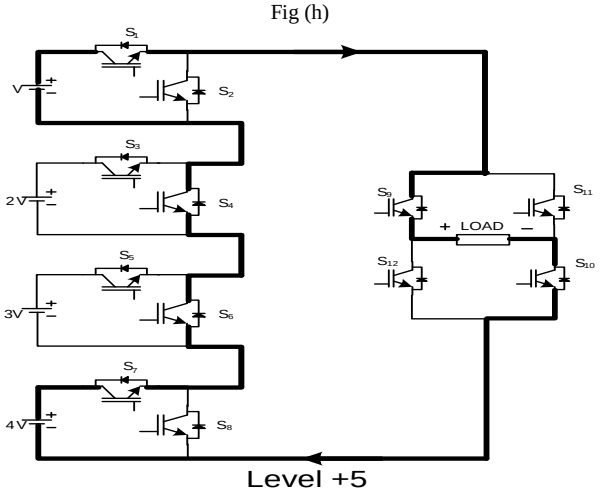


Fig (i)

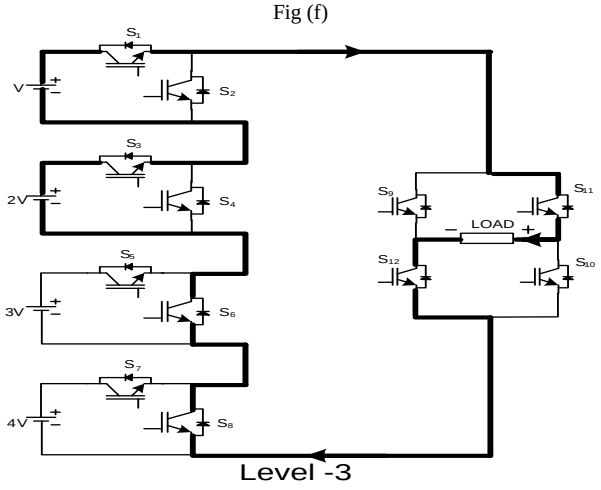
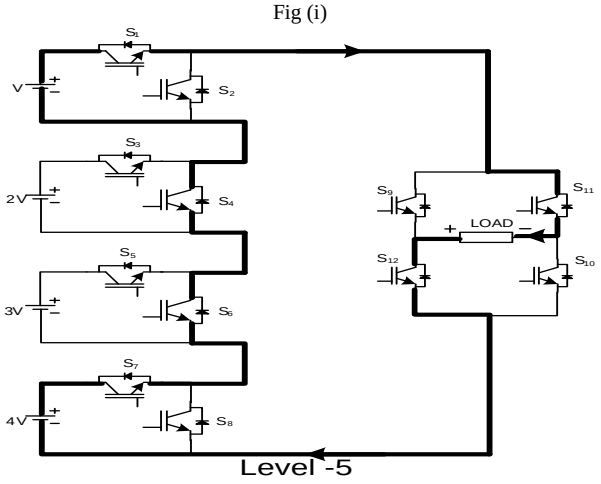


Fig (g)



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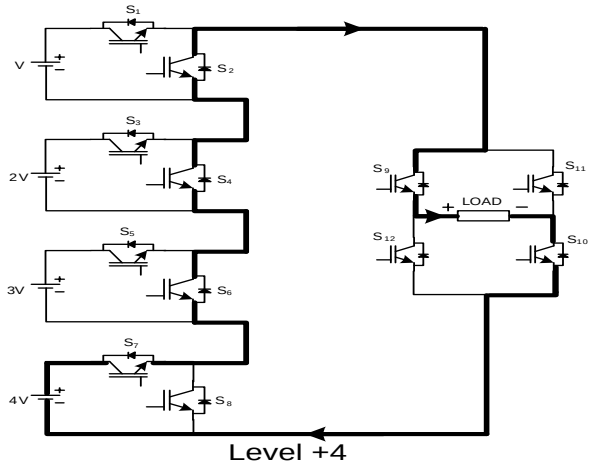

Fig (g)

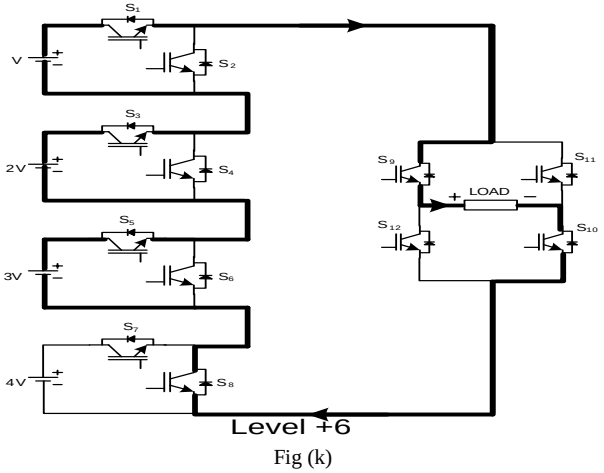

Fig (k)

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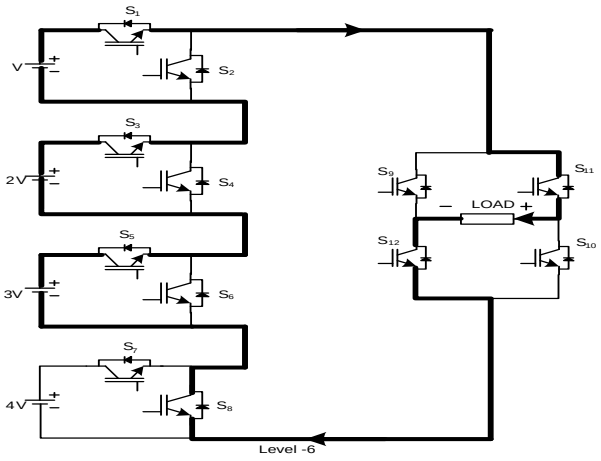

Fig (l)

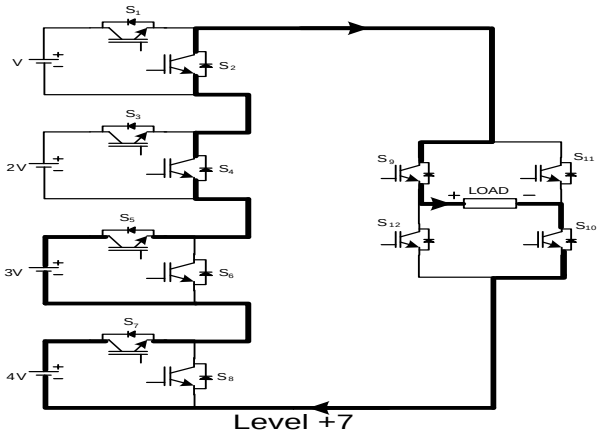

Fig (m)

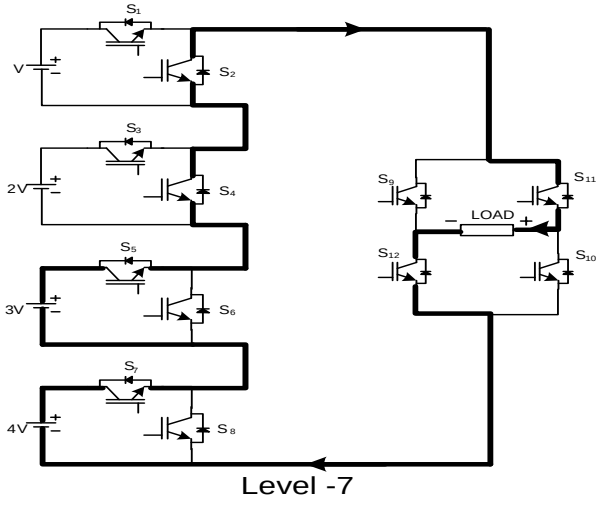

Fig (n)

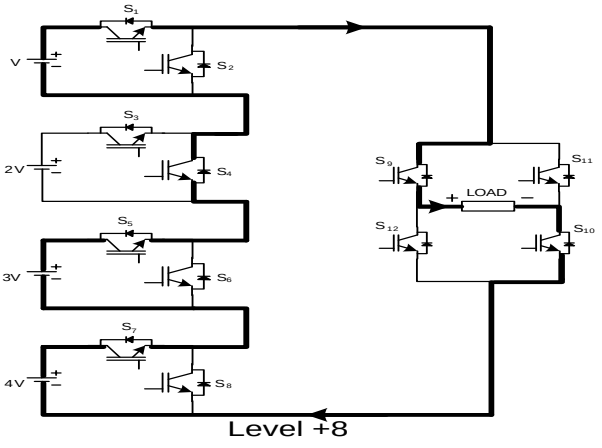

Fig (o)

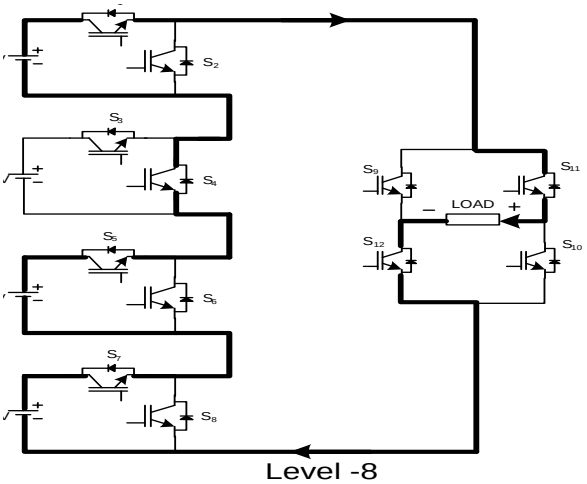

Fig (p)

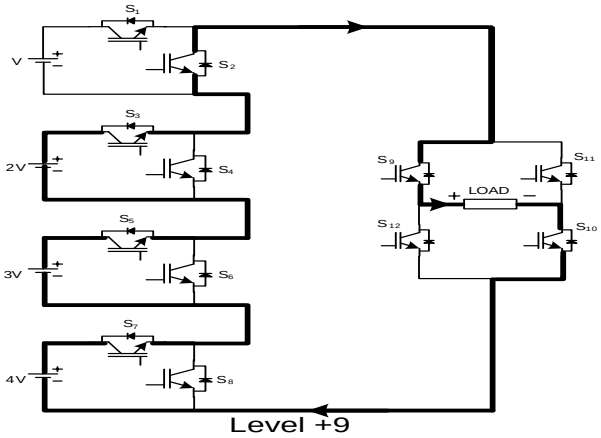

Fig (q)

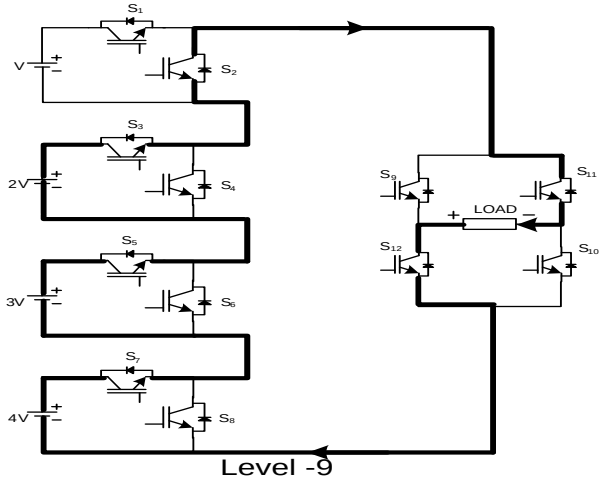

Fig (r)

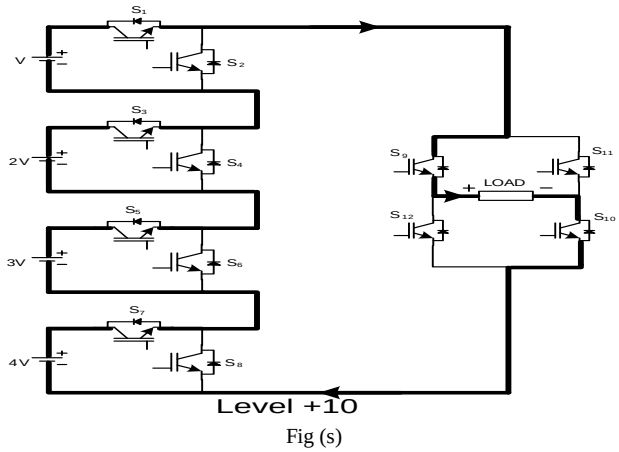

Fig (s)

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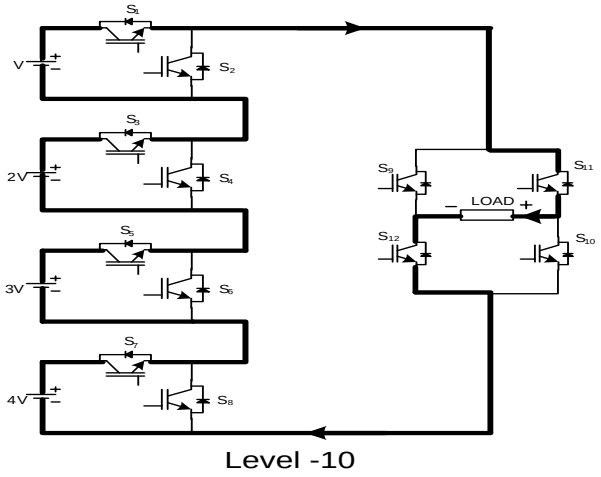
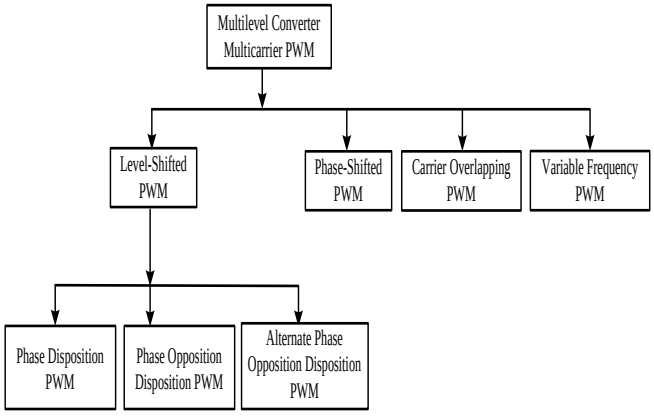


Fig (t)

Fig.3 Fig (a), Fig (b), Fig (c), Fig (d), Fig (e), Fig (f), Fig (g), Fig (h), and Fig (i), Fig (j), Fig (k), Fig (l), Fig (m), Fig (n), Fig (o), Fig (p), Fig (q), Fig (r), Fig (s), and Fig (t), are Switching combination of 21-level MLI.

III. MODULATION STRATEGIE



There are different pulse width modulation strategies as given below [12-13].

A. Phase disposition pulse width modulation (PD PWM):- In phase disposition pulse width modulation strategy, where all carrier waveforms are in same phase.

B. *Phase opposition disposition pulse width modulation (POD PWM):-* In phase opposition disposition pulse width modulation strategy, where all carrier waveforms above zero reference are in phase and below zero reference are 1800 out of phase.

C. *Alternate phase opposition disposition pulse width modulation (APOD PWM):-* In alternate phase opposition disposition PWM scheme where every carrier waveform is in out of phase with its neighbor carrier by 1800.

D. *Phase-shifted pulse width modulation (PS PWM):-* A carrier phase shifted PWM for multi-level inverter is used to generate the stepped multi-level output voltage waveform with lower % THD. In proposed, before implementing the Multicarrier PWM Techniques, the gating signals of multi-level inverter switches are generated by comparing sinusoidal reference wave with triangular carrier waves at specific intervals of time producing the characteristic multistep output waveform. MLI with N levels requires (N-1) triangular carriers. In phase shifted PWM, all the triangular carriers have same frequency and same peak to peak amplitude.

IV. SIMULATION RESULTS

The Fig.1 & 2 shows the proposed topology model of single-phase n-level & single-phase 21-level ACMLI. Table II shows THD comparison between different PWM techniques. The simulation parameters are as following R = 10 ohms, L = 10mH, and dc source voltage is 400V; Carrier signal frequency is 1 kHz. In this paper, four PWM techniques are used PD, POD, APOD, PS, VF and CO with different modulation index (Ma). For Ma = 1.0, and Mf = 20, corresponding (%) THD are PS = 5.54, PD = 5.78, POD = 6.01, APOD = 5.10, shown in Fig. 6.1 – 6.6. The harmonic spectrum is carried out by using the FFT analysis in MATLAB/Simulink.

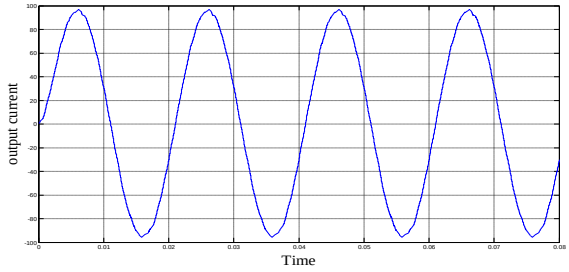


Fig.4 Single-Phase current by PSPWM for 24-level inverter with R-L load

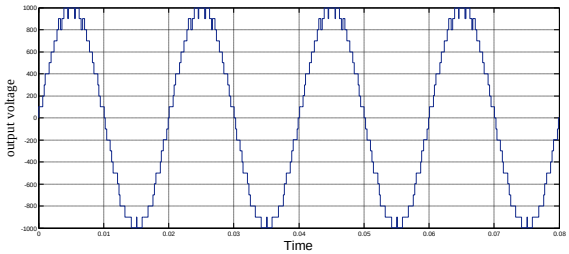


Fig.5 Single-Phase Voltage by PSPWM for 24-level inverter with R-L load

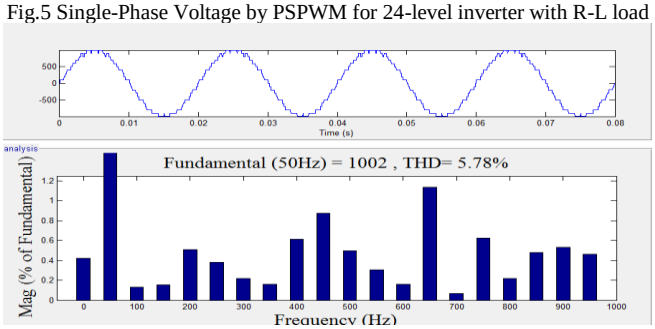


Fig. 6.1: FFT analysis by PDPWM for R-L load (Ma=1.0, Mf=20).

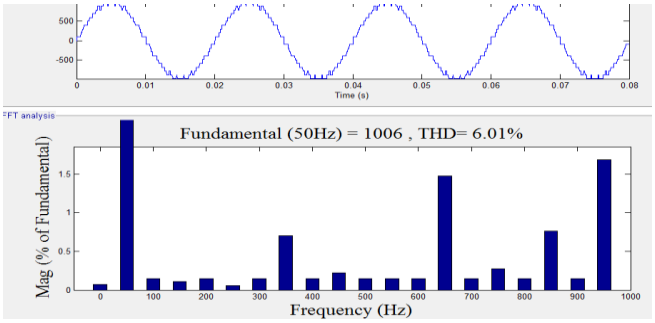


Fig. 6.2.: FFT analysis by PODPWM for R-L load (Ma=1.0, Mf=20).

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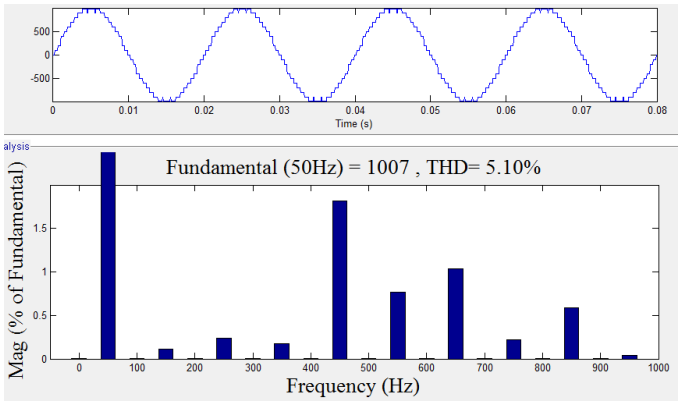

Fig. 6.3: FFT analysis by APODPWM for R-L load (Ma=1.0, Mf=20).

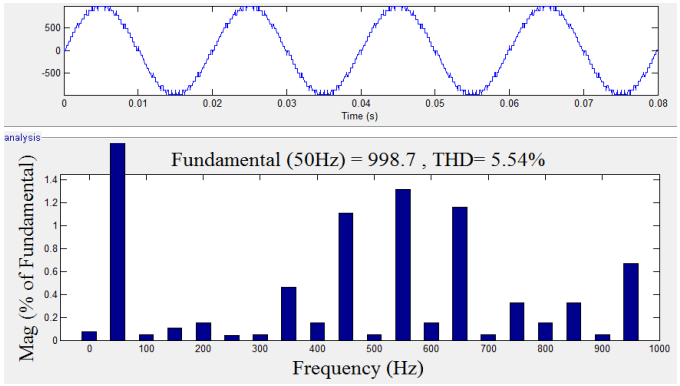

Fig. 6.4: FFT analysis by PSPWM for R-L load (Ma=1.0, Mf=20).

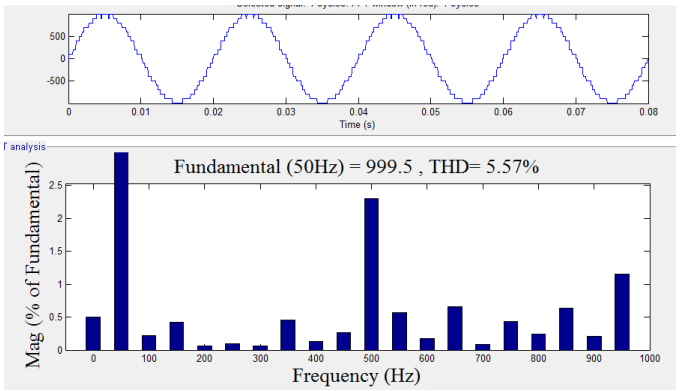

Fig. 6.5: FFT analysis by VFPWM for R-L load (Ma=1.0, Mf=20).

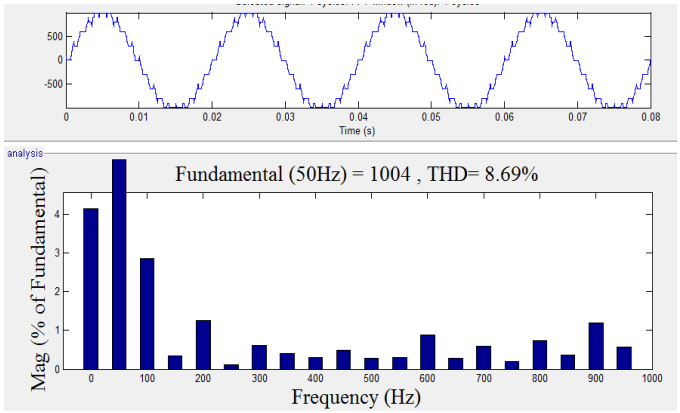

Fig. 6.6: FFT analysis by COPWM for R-L load (Ma=1.0, Mf=20).

TABLE. II THD ANALYSIS B/W DIFFERENT PWM TECHNIQUES FOR 21-LEVEL MLI

Modulation Index	PS PWM %THD	PD PWM %THD	POD PWM %THD	APOD PWM %THD	VF PWM %THD	CO PWM %THD
1.1	6.24	5.75	5.75	4.70	5.70	8.09
1.0	5.54	5.78	6.01	5.10	5.57	8.69
0.9	6.43	6.12	5.99	6.28	6.23	10.20
0.8	7.31	6.99	6.82	6.44	6.60	11.97

TABLE. III COMPARISON OF THE PROPOSED AND CONVENTIONAL MLI

	DCMIL	FCMLI	Proposed Inverter
main switching Devices	40	40	12
diodes	40	40	12
DC bus	20	20	4
balancing capacitors	0	200	0

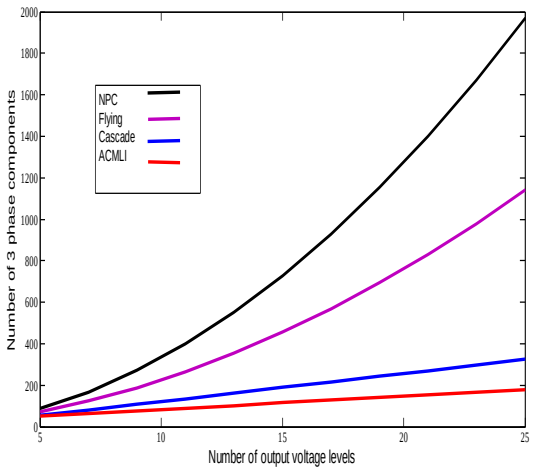

Fig.7 Required number of single phase components for different multi-level inverter topologies.

Fig. 7 shows the required number of single phase components for different multilevel inverter topologies. So it is clearly shows that the proposed ACMLI topology is requires less number of components than other conventional topologies so as the voltage level increases the number of components will decreases particularly for higher voltage levels [14-15].

V. CONCLUSION

In this paper, a 21-level multi-level inverter using Asymmetrical cascaded MLI topology is proposed with different PWM techniques and proposed MLI topology with different PWM techniques is used to generate 21-level output phase voltage. It is proved that, the proposed work of Single phase 21-level MLI output voltage total harmonics distortion is reduced and improve the efficiency of system compare with different conventional topologies of single phase and three-phase 21-level MLI. Harmonic analysis carried out using Mat Lab R2013a version software. This proposed MLI topology requires less number of components as compared to

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conventional MLI inverters. Simulation results show the performance of single-phase MLI with different PWM techniques.

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