Design and Implementation of Different types of Comparator

Prof. Bharat H. Nagpara[1], Mr. Godhakiya Santosh M.[2], Mr. Nagar Jay V.[3]

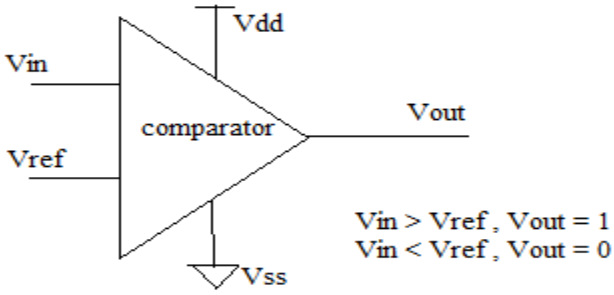
Abstract— **Comparators are mostly used in analog-to-digital converter (ADCs). In the conversion process, first the input signal is sampled. Then the sampled signal is applied to a number of comparators to determine the digital equivalent of the analog value. Apart from that, comparators are used in peak detectors, zero crossing detectors, switching power regulators. Different types of comparators are studied and the circuits are simulated in LTspice-IV using PTM 45nm technology. The circuits are simulated with 1 Volt DC supply voltage. Different static and dynamic characteristics of all the comparators are studied and compared. Their advantages and disadvantages were also discussed. Test structures of the comparators, designed in PTM 45 nm technology are measured to determine power dissipation and delay with 1 V are compared and the superior features of the proposed comparator are established.**

Keyword- **Comparator, open-loop comparator, pre-amplifier based comparator, simulation.**

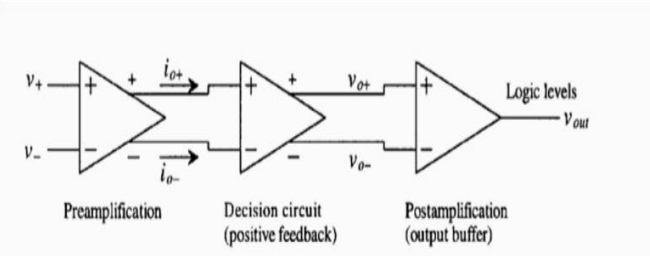
I. INTRODUCTION

In electronics, Operational amplifier is designed to be used with negative feedback and also used as comparator in open loop configuration. Comparator is especially designed for open loop configuration without any feedback. So it is the second most widely used device in electronic circuits after Opamp .Comparator is one of the main fundamental blocks in analog-to-digital (ADC) converters. Since they are decision making circuits that interface the ADCs signals, the accuracy, which is often find out by its input referred offset voltage, is required for the resolution of high-performance ADCs.

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary (0 or 1) signal based on the comparison. If Vin > Vref, the output of the comparator is a logic 1, but when the Vin is at a potential less than the Vref terminal, the output of the comparator is at logic 0. We will discuss practical comparator design and analysis where propagation Delay and Power Dissipation are important.



A block diagram of a high-performance comparator is shown in below fig. The comparator consists of three stages such as input preamplifier, a positive feedback or decision stage, & an output buffer. The preamp stage (or stages) amplifies the input signal to improve the comparator sensitivity i.e., increases the minimum input signal with which the



comparator can make a decision and isolates the input of the comparator from switching noise coming from the positive feedback stage *(it is important).*

II. ARCHITECTURE OF COMPARATOR

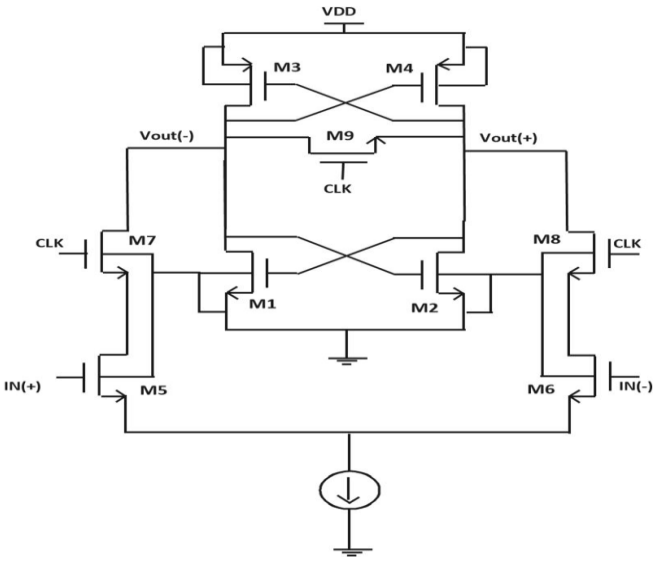
Reset and regeneration are the 2-Ø for comparison cycle of the comparator. In the reset phase, VCC is applied at the gates of the transistor M9, M7 and M8. M9 short circuits the differential nodes when M7 and M8 provide a connection of input and the differential nodes of the latch.

RESETPHASE:

Reset phase is regarded as due to when clock is high. In this phase M7 and M8 are switched 'ON', connecting the output of the pre-amplifier to the differential nodes of the latch through transistor M5 and M6 respectively. Also the transistor M9 is switched 'ON' which short circuits the node Vout (-) and Vout (+) to a DC level of 1.65 Volts. The benefits of having this reset phase is, first, that the differential nodes are set to a certain DC value which removes the

ISSN: 2278 – 7798

memory effect in the latch & secondly, that the charge imbalance is created at the differential nodes of the latch.

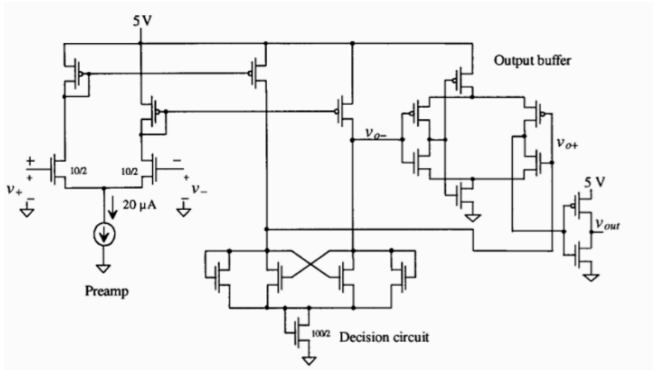


REGENERATION PHASE:

Regeneration phase starts whenever the clock turns from high to low. In this phase the M7, M8 and M9 turn 'OFF' and then the inverter pair moves the either of the Vout (+) and Vout (-) nodes to VDD or GND depending upon the charge imbalance created due to the difference in the input signal. The speed of voltage transition depends upon the gain of the inverter, biasing current, and sizes of the transistors.

III. BASIC COMPARATOR

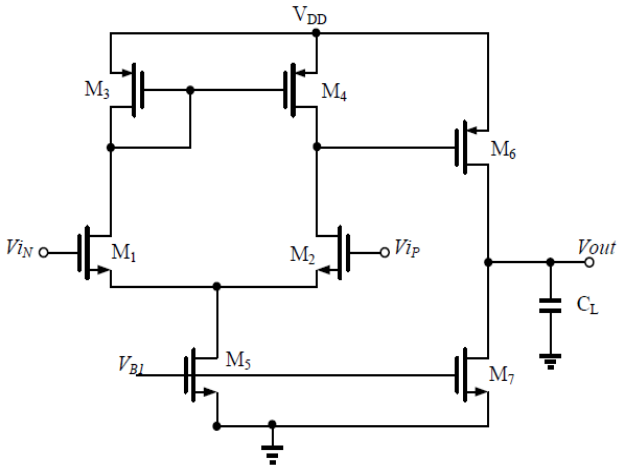
The most basic version of the Comparator is the source follower. It is a common drain amplifier circuit with unity voltage gain.



It is a common drain amplifier circuit with unity voltage gain. The output at the source terminal follows the input applied at the gate. The schematic of the circuit is shown in fig. It is designed with the NMOS, PMOS and ideal current source. Comparator can also be designed with the resistor connected between source & supply. But it does not permits a constant current flowing through the source terminal. It results into non-linearity in the output and we cannot achieve unity voltage gain (1) always. It also has high output impedance. Thus, resistive configuration is not used. We can use PMOS or NMOS as a load. But, the implementation with recently provides good results.

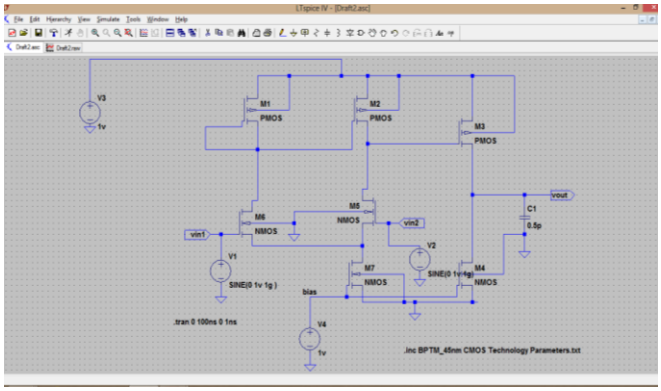
IV. OPEN LOOP COMPARATOR

Open-loop comparator is in fact a high gain amplifier with differential input & single ended output with large swing.

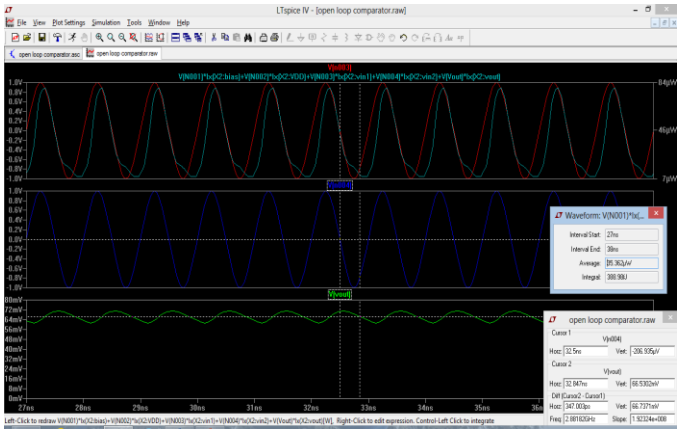


A two stage op-amp without compensation is an excellent realization of open-loop comparator which is illustrated in Figure. Since precise gain in not required in comparator, no compensation technique is needed. This comparator has two poles which compared to the one-pole implementation of the open loop comparator achieves higher speed. This configuration consumes more power; therefore this type of comparator is not suited for high speed A/D converters as well as low power ADCs.

V. SIMULATION

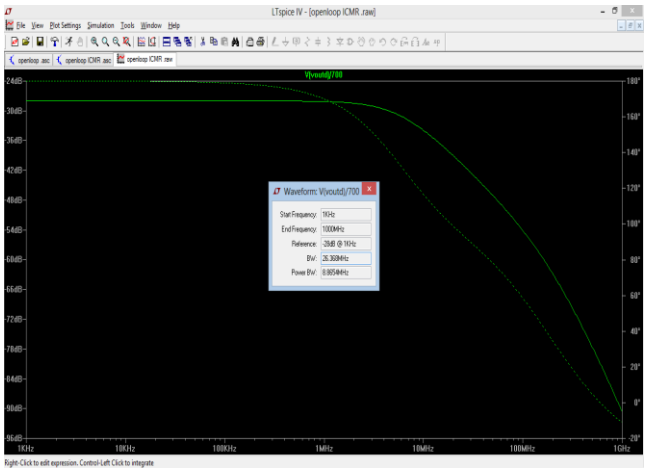


POWER DISSIPATION AND DELAY

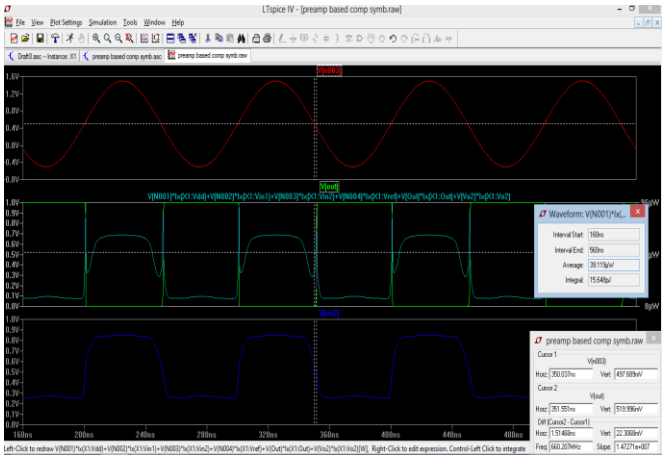


ISSN: 2278 – 7798

ICMR AND BANDWIDTH

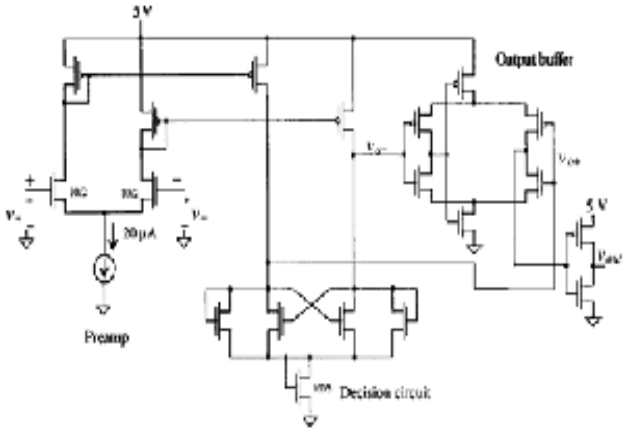


POWER DISSIPATION AND DELAY



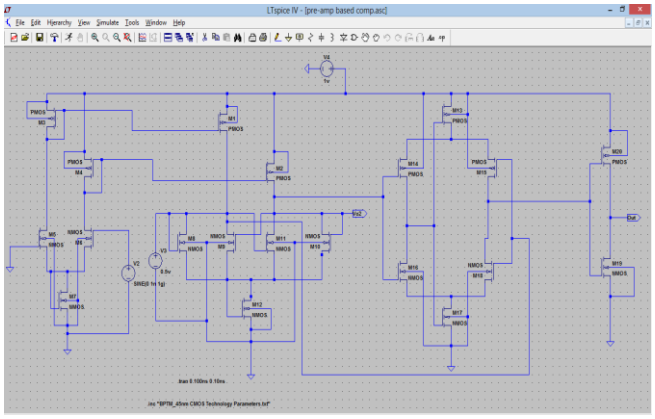
VI. PRE-AMPLIFIER BASED COMPARATOR

The complete schematic of the comparator is shown in fig. Here the input Voltage as a ref parameter. And sweep this parameter from 0 to 1 V.

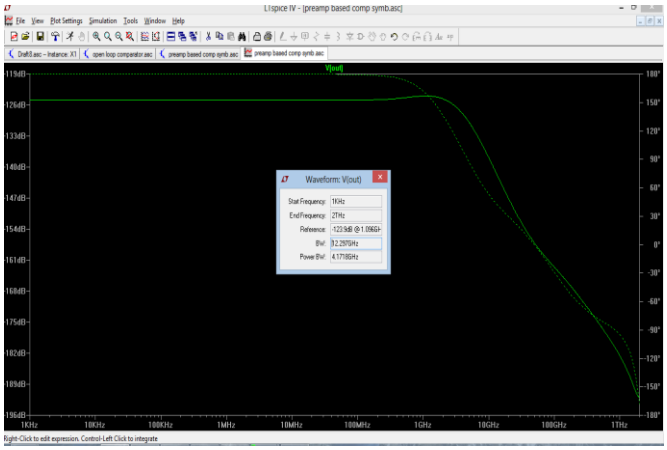


The reference Voltage as 0.5 Volt. Here the reference Voltage as 0.5V.So if the input Voltage is greater than reference Voltage it is giving output Voltage as logic 1.And if the Input Voltage is less than reference Voltage it gives the Output as logic 0.

VII. SIMULATION



BANDWIDTH AND GAIN



VIII. RESULT TABLE

COMPARISON RESULT OF COMPARATOR DESIGN

Parameters	180nm	90nm	45nm (open-loop comparator)	45nm (pre-amplifier based comparator)
Length	180nm	90nm	45nm	45nm
Voltage supply	1.8V	1V	1V	1V
Delay	1.59ns	0.035ns	347ps	1.51ns
Average power Dissipation	173.15 µW	69.81µW	35.36µW	39.11µW
Gain	-	-	20db	175db
ICMR	-	-	30db	125db
Offset voltage	-	-	0.14V	178µV
Bandwidth	-	-	26.368MHz	12.29GHz
Speed	-	-	2.88GHz	0.65GHz

ISSN: 2278 – 7798

IX. CONCLUSION

In this paper open loop comparator and preamplifier based comparator of CMOS is implemented in 45nm. Its simulation results and various parameters is compared for 180nm and 90nm technology the power consumption & delay of different types of CMOS comparators are compared at various supply voltages. Speed of the comparator which is implemented in 45nm is more than speed of comparator in 180nm and 90nm. Also less power Dissipation (35.36µW and 39.11µW), which is our most requirement. Hence it is concluded that in 45nm Comparator operate with higher speed and provide more stabilized Output compare to 90nm and 180nm.

ACKNOWLEDGMENT

First I would like to thank Mr. Bharat H. Nagpara sir, and the entire department of Electronic and Communication Engineering at Shri C.U.Shah College of Engineering and technology, Wadhwan which prepared me for this project.

I wish to personally thank Dr. K. H. Wandra sir, Principal of Shri C.U.Shah College of Engineering and technology, Wadhwan, Prof. D. N. Khandhar Head of Electronics and Communication Department, for giving me the opportunity to work on this very demanding and very rewarding project and for his devotion to this project. I wish to also personally Mr. Bharat H. Nagpara sir support and great advice and for being there during crunch time.

Our sincerest appreciation must be extended. We also want to thank faculties of the College. They have been very kind and helpful to us. We want to thank all teaching and non-teaching staff to support us**.** I also thankful my friends who directly or indirectly supported me for choosing this project for final year degree engineering. We would like to express our sincere gratitude to our Guides for their help during the course of the project right from selection of the project, their constant encouragement, expert academic and practical guidance.

REFERENCES

[1]R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, Third Edition, Wiley Publication, 1964, pp. 1-31, 931 1022.

[2]Ajay Vishwakarma, Different Parameter Analysis of CMOS Charge Sharing Latch Comparator using 90nm Technology, International Journal of Computer Applications (0975 – 8887) Volume 63– No.11, February 2013

[3]yahoui kong, shuzheng xu and huazong y, ―an ultra low output resistance and wide swing voltage follower‖, icccas 2007, pp. 1007-1010, july 2007.

[4]Aalay Kapadia, Analysis And Characterization of Different Comparator Topologies, international journal of scientific & technology research volume 1, issue 11, december 2012 issn 2277-8616

[5]J. Sexton, T. Tauqeer, M. Mohiuddin and M. Missous "GHz Class Low Power Flash ADC for Broadband Communications", the University of Manchester, School of Electrical and Electronic Engineering.

Godhakiya Santosh M. and Nagar Jay V. are pursuing B.E. (final year) Degree in Electronics and Communication Engineering from Gujarat Technological University, Ahmadabad

Prof. B. H. Nagpara received the Degree in Electronics and Communication Engineering from Saurashtra University, Rajkot & M.E. Degree in Electronics and Communication Engineering from Gujarat Technological University, Ahmadabad. Currently he is working as an Assistant Professor in Electronics & Communication at C. U. Shah University, Wadhwancity. His interests are in Digital System Design using VLSI/CMOS Technology, Analog and Mixed mode Designs.

ISSN: 2278 – 7798