# Asymmetrical 63 level Inverter with reduced switches and its switching scheme

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**Abstract—*This paper deals with reduced number of switches in multilevel inverter. Asymmetrical inverter has been used with the topology of cascading the fundamental unit. The grounds behind using multilevel is for enhancing the power quality and scaling down the distortions in waveforms. The output waveform attained is quite closer to sinusoidal waveform with a very low distortion. The switching is in a sequence and flexible for increasing or cutting down the voltage levels when desired. The switching methods with pulse width modulation have been discussed. And a comparative study of different topologies of symmetrical as well as asymmetrical inverter of different levels has been done. Lastly, the simulated results from Simulink/MATLAB is presented.***

***Keywords*—Multilevel inverter; Switching schemes, New topology, Cascaded H-Bridge multilevel inverter (CMLI); 63 level; PWM Pulse Width Modulation, asymmetrical**

## I. INTRODUCTION

Multilevel converters are being highly considered for their illustrious benefits such as higher efficiency and high voltage operation. The power quality is enhanced to a much greater extent. Distortion in waveforms is reduced and also the blocking voltage on the switches. With all these advantages, there are slight conditions that have to be reckoned such as - the increase in cost and reduction in reliability. Also the circuit gets a bit complex and losses in the devices increases to some extent [1]. The main motive behind the use of multilevel inverter is to enhance the power quality, when working on medium voltage high power drives. To attain this, power electronics and a wide variation of semiconductor switches are in use. The wide range of power from milliwatts to gigawatt can be easily obtained from power electronics converters. Now-a-days it is difficult to connect a single semiconductor switch directly to medium voltage grids which are in the range of kilovolts. That's why a novel family of multilevel has begun as a solution for working with higher voltage levels. In most of the medium voltage application drive, still, it's a fixed speed motor, for e.g. fan& pumps [2]. And due to this, the flow of air or liquid is controlled by mechanical methods which leads to a lot of power losses. Thus the power losses can be reduced to a greater extent if there is a use of adjustable drivers even in medium voltage applications. And that can be achieved by use of inverters, by varying the voltage and frequency at its output. With proper switching frequency, control methods and filters used, improved power quality can be attained.

To increase higher voltage level and voltage rating, multilevel inverter came into existence in 1981. Neutral point inverter of 3 level was the first multilevel inverter, which extended to higher level and is now named as Diode-clamped inverter [3]. Multilevel inverter when classified can be categorized into mainly of three topologies: CMLI, Diode clamped (DCMLI) and Flying capacitor multilevel inverter (FCMLI). FCMLI requires many bulk capacitors to clamp the voltage. That's why rarely used.

CMLI is the most widely used because of its simple circuit and less component [4]. Each H- Bridge or fundamental block is supplied with a different DC source or a storage capacitor. The output of each cell can be positive, zero or negative, i.e. if $V_n$ is the voltage in that cell, then the output of that cell can be V, 0 or –V. The output voltage of the inverter is the sum of the voltage level of each fundamental block. The number of levels of phase voltage k is decided by

$k= 2*\sum V_n +1$. For $1 < n < N$,

Where n= no. of sub-cell and $V_n$ = normalized DC voltage of each cell.

The topology of asymmetrical inverter is same as symmetrical inverter. Only the number of DC sources or DC links are reduced in it. Thus, in this, higher voltage level can be obtained as in comparison to symmetrical inverter, keeping the number of switches same [5]. Therefore the efficiency is increased as switching losses are reduced. Also with higher number of levels obtained in asymmetrical inverters, the size of filter required is reduced to a greater extent [6]. But switching schemes get complex in it.

The voltage across each device or switches may vary in asymmetrical inverter and also the switching frequency operation. Peak inverse voltage rating of the switches must be kept in mind before designing the circuit [7]. Switches must be used according to its application, such as IGBT (Insulated Gate Bipolar Transistor) in high voltage, low frequency application and use of MOSFET in low voltage high frequency application.

Research work and innovative ideas are being focused now-a-days on some new or hybrid topologies of multilevel inverter. Moreover, the main focus is on the type of switches, reduction of

  

switches, DC sources availability, power loss reduction, algorithms of switching schemes, number of voltage levels, harmonics content reduction, rate of change of voltage and voltage stress along the switches [8].
In this paper, advanced form of CMLI is designed so as to lower the number of switches. The switches in fundamental block are reduced to 2 instead of 4 switches in H-Bridge. The switching sequence is flexible and symmetric as to easily apply when the levels are altered.

## II. TOPOLOGIES OF OPERATION

### *i. First Method (Symmetrical Operaion)*

$V_{dc\,(k-1)} = V_{dc\,(k)} = V_{dc}$ k=1, 2…, n n= number of basic blocks
N level = 2*n + 1, $N_{level}$ represents no. of output voltage
$V_{max} = (N_{level}-1) / 2\ V_{dc}$
$N_{IGBT} = 4n+ 4$ $N_{IGBT}$ represents the number of required IGBTs
N sources = n N sources represents the number of series connected basic block.

Table 1: Number of IGBTs and Voltage levels for topology 1

| | Number of basic blocks | | | | |
|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** |
| Number of levels | 3 | 5 | 7 | 9 | 11 |
| Number of switches | 2+4 | 4+4 | 6+4 | 8+4 | 10+4 |
| $V_{max}$ | $V_{dc}$ | 2 $V_{dc}$ | 3 $V_{dc}$ | 4 $V_{dc}$ | 5 $V_{dc}$ |

For 5 sources, i.e. 5 basic block connected in series, the required DC sources will be
$V_{dc\,(1)} = V_{dc}$,$V_{dc\,(2)} = V_{dc}$
$V_{dc\,(3)} = V_{dc}V_{dc\,(4)} = V_{dc}$
$V_{dc\,(5)} = V_{dc}$

The number of levels obtained from this topology is 11, when five of the basic blocks are connected according to this topology.

### ii. Second Method:

$V_{dc\,(k)} = kV_{dc}$ k=1, 2…, n n= number of basic blocks

$N_{level} = n* (n+1) +1$
$V_{max} = (N_{level}-1) / 2\ V_{dc}$ n= Total number of employed fundamental block

$N_{IGBT} = 4n + 4$ $N_{IGBT}$ represents number of required IGBTs
$N_{sources} = n$ $N_{sources}$ represents number of series connected basic block.
For 5 sources i.e. 5 basic blocks connected in series, the required DC sources will be
$V_{dc\,(1)} = V_{dc}V_{dc\,(2)} = 2\ V_{dc}$
$V_{dc\,(3)} = 3\ V_{dc}V_{dc\,(4)} = 4\ V_{dc}$
$V_{dc\,(5)} = 5\ V_{dc}$
The number of level obtained from this topology is 31, when five of the basic blocks are connected according to this topology.

Table 2: Number of IGBTs and Voltage levels for topology 2

| | Number of basic blocks | | | | |
|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** |
| Number of levels | 3 | 7 | 13 | 21 | 31 |
| Number of switches | 2+4 | 4+4 | 6+4 | 8+4 | 10+4 |
| $V_n$ | $V_{dc}$ | 2 $V_{dc}$ | 3 $V_{dc}$ | 4 $V_{dc}$ | 5 $V_{dc}$ |

### iii. Third Method:

$V_{dc\,(k)} = 2^{(k-1)}V_{dc,}$ k = 1, 2……., 2n
$N_{level} = 2^{n+1} - 1$
$V_{max} = (N_{level} - 1)/2\ V_{dc}$
$N_{IGBT} = 6n$
$N_{source} = 2n$

Table 3: Number of IGBTs and Voltage levels for topology 3

| | Number of basic blocks | | | | |
|---|---|---|---|---|---|
| | **1** | **2** | **3** | **4** | **5** |
| Number of levels | 3 | 7 | 15 | 31 | 63 |
| Number of switches | 2+4 | 4+4 | 6+4 | 8+4 | 10+4 |
| $V_n$ | $V_{dc}$ | 2 $V_{dc}$ | 4 $V_{dc}$ | 8 $V_{dc}$ | 16 $V_{dc}$ |

For 5 sources i.e. 5 basic blocks connected in series, the required DC sources will be
$V_{dc\,1} = V_{dc}$, $V_{dc\,2} = 2\ V_{dc}V_{dc\,3} = 4\ V_{dc}$
$V_{dc\,4} = 8\ V_{dc}$ $V_{dc\,5} = 16\ V_{dc}$

  

The number of level obtained from this topology is 63, when five of the basic blocks are connected according to this topology.

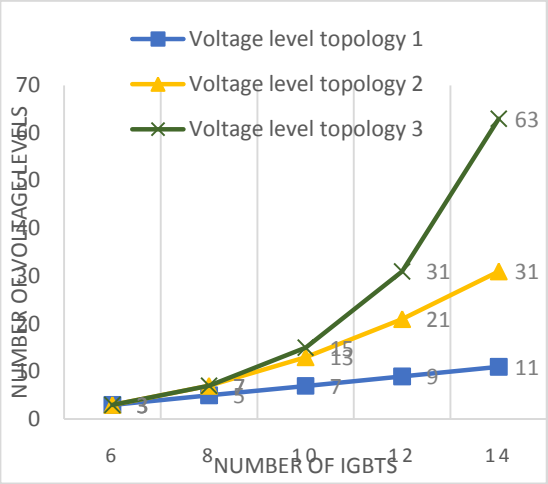


Figure 1: Number of IGBTs vs Voltage levels attained in the three topologies

## III. PROPOSED MULTILEVEL INVERTER TOPOLOGY

The proposed inverter is of the third topology arrangement of voltage in an advanced CMLI form. The proposed topology of reduced switch multilevel inverter as compared to symmetrical and asymmetrical topology as shown in fig. 1.. The circuit diagram is shown in Fig. 2. With more increase in voltage levels, considering the less number of switches, the PIV rating of the switches has to be increased [9]. Considering this, third topology has been used. It is an asymmetrical 63 level inverter. It contains of a cascaded form of fundamental unit of cells with two switches in each unit and a battery source. All the units are cascaded along with a full bridge converter. IGBT with anti-parallel diode is used as a switch. The two switches in each unit are complementary in operation to each other, such that when one is on, the other must be off. For e.g. IGBT1 is complementary to IGBT6 and so on. The voltage $V_{dc}$ denoted in the figure is the nominal voltage where $V_{dc}$ = 14 volts. The other voltage of source is in multiplication of the nominal voltages.

The voltage of sources is in geometric progression in order of 14 volt, 28 volt, 56 volt, 112 volt and 224 volt. For (2n+4) switches, the number of voltage level attained is $2^{(n-1)}$ (2n+4) switches = $2^{(n-1)}$ levels, and n = no. of voltage sources.

The voltage levels are in the form of binary series. By this form, on using 14 switches we have achieved 63 level of output voltage. The maximum and minimum voltage will be +31 $V_{dc}$ and -31 $V_{dc}$. Here the value of $V_{dc}$ is 14 volts.

The output voltage across the load is the summation of all the voltage across each fundamental unit.

$V_0 = V_{o1} + V_{02} + V_{03} + \ldots\ldots + V_{0k}$

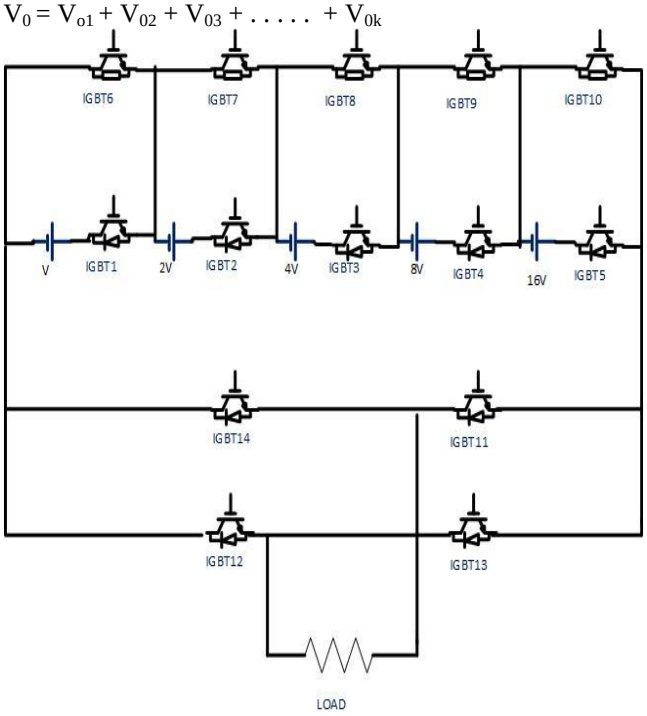


Figure 2: Proposed multilevel inverter topology

Different voltage sources are required in this topology which can be obtained from either renewable sources or storage devices as capacitor or batteries. Moreover, it can be attained by rectifying the available AC source through isolated transformer and rectifier [10]. This topology avoids the extra clamping diodes or balancing capacitors. That's why the components are reduced in the circuit as compared to DCMLI or FCMLI [11]. The variation in active power demand as a source can be balanced by 'charge balance method' [12]. The control methods mainly balances the supplied power. The main aim of this paper is to focus on its advanced and balanced controlling techniques to obtain optimal structures according to variousconditions. The circuit is proposed for three phase inverter. Three phase is obtained by combining the three single phase as shown in fig. 2. The switching is shifted by 120° for each phase. This phase is shifted in a sinusoidal wave given for Pulse width modulation.

  

## IV. CONTROL AND MODULATION STRATEGIES

### 3.1 Types of Modulation Techniques:

The harmonic content in output voltage depends on modulation methods. Since the number of switches are more in multilevel inverter. Therefore, complex switching. But it helps in improving modulation techniques, these areas: switching frequency is reduced, common mode voltage is minimized and/or DC link voltage is balanced.

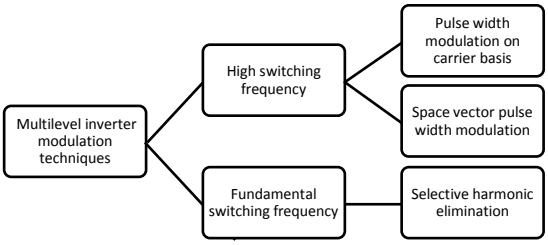


Fig. 3: Classification of Modulation Techniques

Switching can be basically be classified in two forms:

High Switching Frequency: More than once commutation in a cycle of each inverter. Ex. - Carrier based PWM, Space vector PWM
Fundamental Switching Frequency: Each inverter is commutated only once in each cycle. Ex. - Selective Harmonic Elimination (SHE)

The switching techniques are basically of three types:

i. Pulse width modulation on carrier basis: Pulses are obtained from comparison between the reference signal (generally sinusoidal wave) and carrier signal (generally triangular waves). This is most widely used switching schemes.
ii. Space Vector Pulse width modulation: Vector modulation is done with sampling the reference voltage in a sector division. Switching states are generated according to different voltage vectors, in which the reference signal is based on its closest signals.
iii. Selective Harmonic elimination: The specific harmonic is eliminated by calculating the duty ratio and switching angles. In this all switches are on and off only once in a cycle.

### 3.2 Multilevel Pulse Width Modulation

The carrier signal in PWM can be obtained with level shifting and phase shifting. For a level shifted PWM, the phase and pick to pick amplitude of the carrier are same and the carriers are in vertical positions to each other. While in a phase shifted PWM, the phase angle is shifted of each carrier, the angle calculation is done accordingly to reduce the

The PWM techniques for further can be classified as

i. Phase Disposition PWM (PD): All the carrier signal has same amplitude, frequency and phase.
ii. Alternate phase opposition disposition PWM (APOD): 180° phase shift in carrier signal from its neighbouring carrier.
iii. Phase opposition disposition PWM (POD): Carrier signal above the X-axis are in phase while below are out of phase.

Switching frequency optimal PWM (SFO-PWM): This is similar to POD in terms of the carrier signal. But the reference signal (sinusoidal) is changed by injecting third harmonics. The peak value of sine gets curved in a mirror image form. This is generally used in space vector. It is valid for three phases. In this, the average minimum and maximum instantaneous value of Va, Vb. Vc is subtracted from the reference voltage.

### 3.3 Effect of Modulation Index:

Modulation index is the ratio of the reference signal to that of peak carrier signal. All of these three PWM can be used for asymmetric inverter. Harmonic spectrum depends upon frequency modulation ratio $m_f$. The modulation index needs to be in a range which depends upon the level of carrier signals. For a 63 level inverter, the carrier signals above zero is 31. So, the amplitude of modulation index $m_a$ must be in the range of (1-1/31) to 1. Below this, there will be under-modulation and the upper carrier won't be compared with sinusoidal. Thus no switching to certain switch. And modulation index above 1 will lead to over-modulation, which increases the THD content.

In this paper the modulation index is taken as 0.98. The triangular carrier used is 31 of step 1 and values increasing for each. The min. carrier signal is from 0 to 1 and top carrier signal range is from

  

30 to 31. The peak value of reference sinusoidal signal is 0.98*31 = 30.38 volts.

## V. PROPOSED SWITCHING TECHNIQUES

PD-PWM (Phase Disposition) has been used as modulation to give pulse to the switches of fundamental unit. The modulation index for the proposed topology are: Amplitude modulation $m_a$=1 and Frequency modulation $m_f$=99. PD-PWM has been shown in fig. 4. Sinusoidal signal compared to zero to provide pulse signal to the full bridge converter.

Table 1: Switching Sequence

| | *IGBT1 S1* | *IGBT2 S2* | *IGBT3 S3* | *IGBT4 S4* | *IGBT5 S5* | *IGBT6 S1'* | *IGBT7 S2'* | *IGBT8 S3'* | *IGBT9 S4'* | *IGBT10 S5'* |
|---|---|---|---|---|---|---|---|---|---|---|
| *0V* | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| *1V* | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| *2V* | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| *3V* | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| *4V* | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| *5V* | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| *6V* | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| *7V* | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| *8V* | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| *9V* | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| *10V* | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| *11V* | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| *12V* | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| *13V* | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| *14V* | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| *15V* | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| *16V* | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| *17V* | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| *18V* | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| *19V* | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| *20V* | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| *21V* | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| *22V* | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| *23V* | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| *24V* | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| *25V* | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| *26V* | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| *27V* | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| *28V* | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| *29V* | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| *30V* | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| *31V* | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

  

The main advantage of the PD - PWM technique is phase voltage spectrum is substantial in its first carrier harmonic. This gives excellent line voltage performance. Carrier harmonic doesn't show up in line voltage. Because carrier harmonic is common-mode component in phase voltage, but gets cancelled out in line voltage. Therefore the remaining harmonic in line voltage is of less energy. Moreover, with even $m_f$ frequency modulation factor, both even as well odd harmonics are present in phase voltage. While with odd $m_f$, only odd harmonics are present in phase voltage. So here $m_f$=99 is taken which is odd.

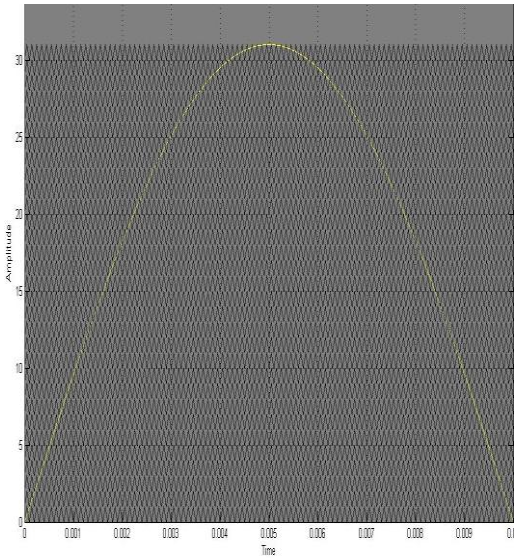


Fig. 4: Phase Disposition PWM with for 63 level inverter.

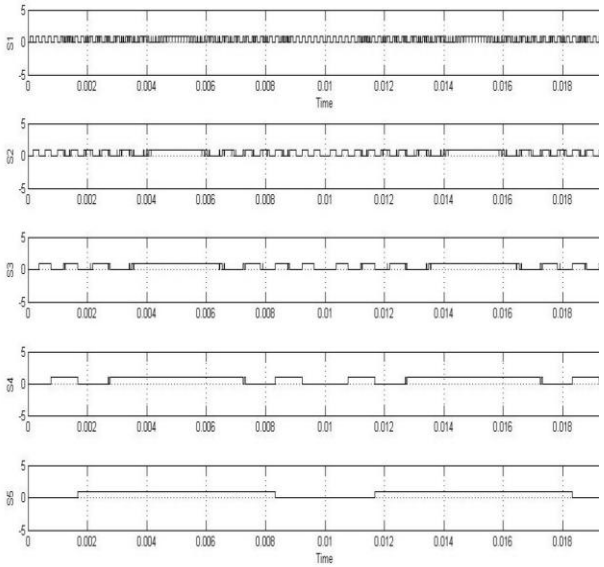


Figure 5: Switching pulses to base unit to five switches IGBT1, IGBT2, IGBT3, IGBT4 and IGBT5

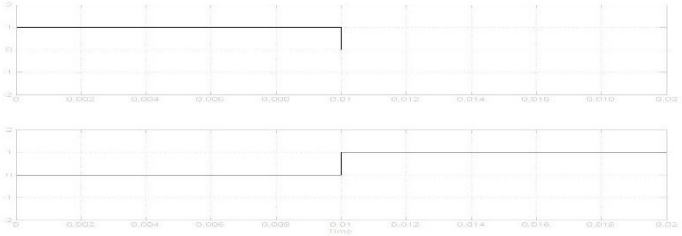

Figure 6: Switching of full bridge of the inverter.

## VI. CALCULATION OF LOSSES:

The losses in switches such as in diode and IGBT can be calculated as

1. Losses during conduction ($P_{cond}$): The losses in equivalent resistance of the switch and on-state voltage drop.

   Losses in switching (Psw): This is the losses because the switching doesn't take place as an ideal switch.

2. Blocking losses ($P_b$): During the off-state of the switch, if there is leakage of current in off-state.

Total power losses can be considered as:
$P_{losses} = P_{cond} + P_{sw}$
The losses depends on the number of switches. Thus for a designed circuit, the losses in symmetrical and asymmetrical type of inverter will remain same as the number of switches are same. The losses in switching depends on both, the semiconductor characteristics and switching algorithm

## VII. SIMULATION AND RESULTS

The observe performance of the proposed topology and advance switching action, a simulation is performed. The simulation is done in MATLAB. The output voltage, THD and power quality are examined of a 63 level inverter.
The circuit diagram of the inverter is shown in Fig.2. The number of voltage sources is 5, the nominal voltage $V_{dc}$=14 volts and other voltages are in G.P. Voltages in different fundamental units given are 14 , 28, 56. 112, 224 volts. The total number of IGBTs used are 14. The load is of R= 100 Ω and L= 20 mH in each branch. The load is star connected. This load is taken low as per to

  

meet motor circuits. Otherwise the simulation may be performed by taking higher values of R-L in the load. There are various modulation techniques that can be used for multilevel inverter. Here, Phase Disposition PWM switching technique has been used. Since the level is too high, so the THD content will be low on it. Therefore, no additional methods have been used for further reduction of THD or elimination of harmonics. Also, there is no need for the use of any filter for the load at which it has been simulated. The cascading of all fundamental unit gives the output in positive staircase with time period of 10 m.sec. The full bridge converter connected at the end terminal of the base unit, makes the final output in sinusoidal form with the frequency being 50 Hz. The switching sequence is shown in Table 4 and 5.

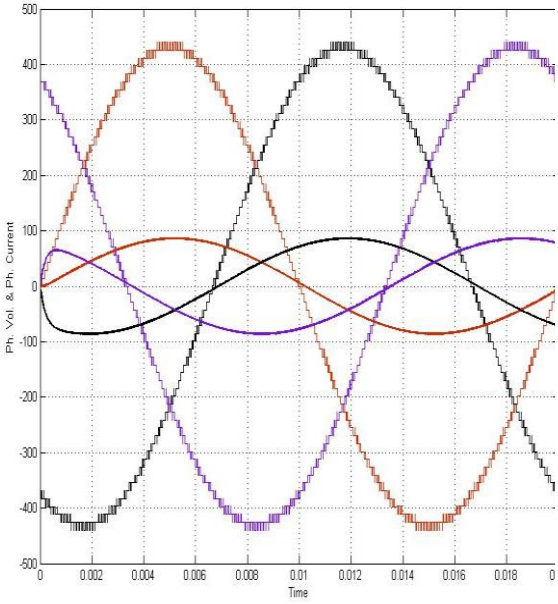


Figure 7: Output phase voltage and Phase current of 63 level 3 phase inverter

It should be noted that the voltage source are in a geometric progression series as $V_{dc}$ , 2 $V_{dc}$, 4 $V_{dc}$, 8 $V_{dc}$, 16 $V_{dc}$ where the value of $V_{dc}$is taken as 14 Volts. The output waveform simulated results are of phase voltage, phase current and line voltage. The peak value of phase voltage here is 14*31= 434Volts which means that the Root Mean Square value is nearly about 308 Volts. The total harmonic distortion of phase voltage and phase current are shown in Fig. 8 and Fig. 9. The calculated THD is 1.88 % for the phase voltage which is desirable. THD of the current waveform is 0.36% which is quite low and acceptable. The line to line voltage is calculated from the simulation result which has the peak value of 751 Volts.

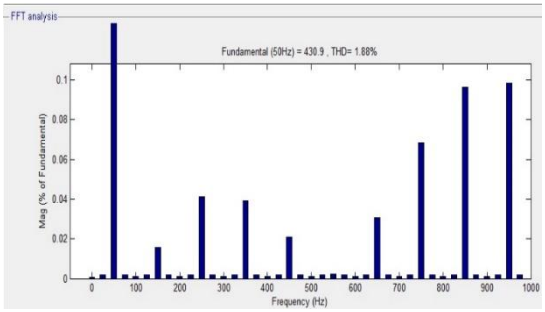


Figure 8: THD of phase voltage of 63 level inverter, THD= 1.88%

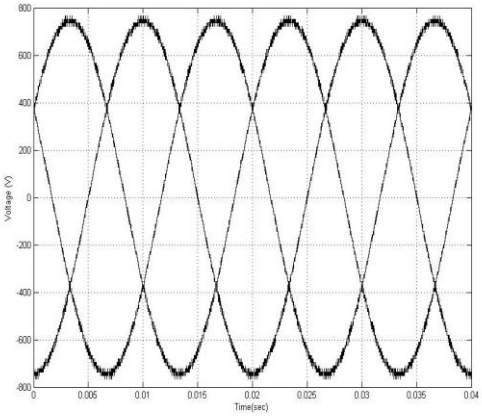


Fig. 10: Output line voltage of 3 phase 63 level inverter. Vmax (line) = 762.10 volts

The THD from the FFT analysis for line voltage is 1.77 %. With such a low harmonics content, the use of filter need not be necessary.

A comparative study of THD of all the level have been done through simulation. It has been performed on the same circuit as shown in fig. 2. The THD of level 5, 7 9……, 63 have been shown in fig. 12

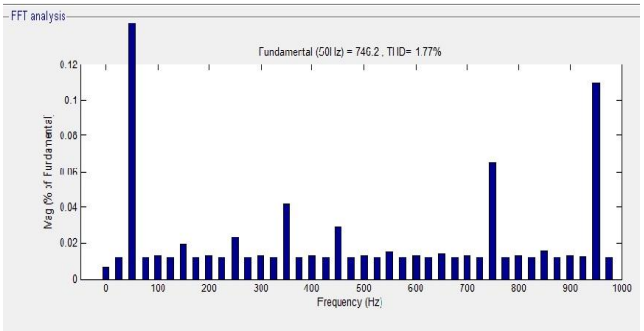


Figure 11: THD of line voltage of 63 level inverter. THD= 1.77 %

  

## VIII. CONCLUSION

The multilevel inverter proposed topology has quite better features over the conventional and other many circuits that has been published. The output result is better in terms of required switches, dc supplies, number of levels in output voltage, total power losses, cost and switching algorithm. The switching is done through PWM techniques, with a systematic sequence and at higher frequency that will enhance the output results. The figure 12 clearly shows the decrease in THD with increase in levels.

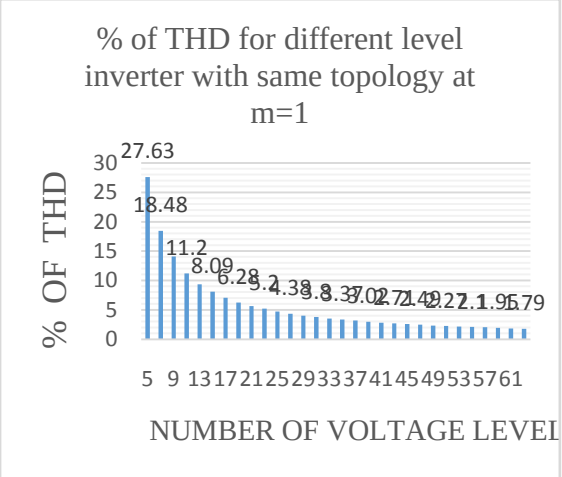


Figure 12: Comparative study of THD of different levels

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