

# SIMON 2.0 Simulation of Threshold Logic Gate Oriented Next Gen Nano Memory Cell

Dr. J. Gope, Gangesh Gulshan, Mahuya Panda, Kumar Sanni Sinha, Sanajy Bhadra

**Abstract**— The incorporation of advanced e-beam lithography technique augmented nano dimensional device research. Today's e-industry is aimed in increasing the memory capacity to terra byte and more. In this regard this short communication is made only to insight the performance analysis and its robustness. Monte Carlo based SIMON2.0 soft computing tool is used for simulation of the proposed memory cell.

**Index Terms**— Threshold Logic Gates, Single Electronics, SIMON 2.0, Memory Cell, Read-Write operation.

## I. INTRODUCTION

The incorporation of Threshold Logic Gates (TLG) to replace age old CMOS technology has ushered wonders to device Scientists and Researchers worldwide [1]. Many new devices have already rocked the market. Others are waiting for elegant solutions. But typically, memory cell with increased size has been a key topic of interest since its very inception. The reason is memory elements foster new scope of intensification for device research. The authors however here must admit that the increase in size of memory cell resembles its amplifying capacity of storing huge data bits and not the physical size expansion in length or width; rather with the blessings of scaling down of device technology the length-width compactness likewise other electronic devices is dwindling down. The shrinking of the physical size of memory is further augmented with the incorporation of nano technology; nonetheless its speed to read and write increased manifold i.e., several thousand times compared to CMOS counterparts.

The fundamental topology of increasing the memory size lies in its fabrication phenomena. With the increasing limitations of CMOS scaling more and more hindrances are mounting day by day. ITRS 2003 [2] has pondered over this issue in the last decade. This motivated Scientists to opt nano device modelling to design advanced nano electronic devices. But the doings were not as simple as sayings. The fabrication technology matured with veracity gradually [3-14]. This led

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to e-beam technology; a technology that is considered indispensable in today's fabrication regime. It is customary to use TLGs for Single Electronics operation. Here the authors are enthused to design and model TLGs using unconventional design tools like SIMON 2.0. It is worth saying that SIMON simulations of TLGs have favored the device Scientist to conceptualize every step of TLG configurations. As because nano device fabrication is utmost costly maneuver thus the nano device research technology is potentially restricted to device modeling using SIMON 2.0 or SILVACO like efficient nearly real time analytical tools. One such course of action has been enumerated here.

The authors here attempted to design highly efficient robust advanced nano memory cell. The following subsections describe the modus operandi of SIMON2.0 modeled TLG based nano memory cell.

## II. TLG GATES AND ITS IMPLEMENTATION USING SIMON

The authors here in this section empirically demonstrate TLG based simple ANDING of two input voltages. The metaphors A and B are two non identical voltages at the two inputs of the TLG AND circuit.

The SIMON simulated TLG AND gate in Fig. 1 comprises of five islands  $N_1 - N_5$  bounded by five tunnel junctions  $J_1 - J_5$  and nine capacitors  $C_1 - C_9$ . The junction resistance and capacitance of tunnel junctions  $J_1, J_2$  and  $J_5$  taken are  $10^5 \Omega$  and  $10^{-19} F$  respectively and for  $J_3$  and  $J_4$  are  $10^5 \Omega$  and  $0.5 aF$  whereas the supply voltage of the circuit  $V_b$  is made constant at 16 mV.

Architecturally, A and B are the two sequential inputs of TLG AND gate and Y provides the output of this circuit. The input voltages are fetched into the gate through the two identical capacitors  $C_1$ , and  $C_2$  having capacitances 0.5 aF. Consecutively, the gate output is gained across capacitor  $C_8$  or from island  $N_4$ . During simulation the authors made the inputs piece-wise constant and applied the combinations of logic '0' and logic '1'. Fig. 2 and Fig. 3 are the input voltages of A and B, and Fig. 4 is the obtained charge at output node. Fig.4 clearly reveals that the charge is positive only when the input vectors i.e., A and B are 1 & 1; it deviates to zero having the input vectors at 0 & 0, 0 & 1 and 1 & 0 respectively. Subsequently, the authors here find a match with the conventional AND logic output waveform and merely advocates for TLG AND gate that truly reflects the behavior of two input AND gate.

### III. SIMON DESIGNING OF MEMORY CELL

#### A. The Essential Elements

Followings are the list of articles with their parameters that were incorporated in this specific SIMON 2.0 based TLG memory cell. For simplicity a straight forward logic was made to maneuver during simulation.

Elements	Quantity
Capacitors	130
Tunnel Junctions	156
Voltage Source	26
Nodes	270
Grounds	9

Table1: Circuit Component List

#### B. Circuit Configuration

While depicting the circuit configuration one must ponder over the criticality of the circuit. It's worth noting that such circuit designing is not only painstaking but very time consuming. The question may arise about the macro modelling of this model; but TLG has some intrinsic advantages in next decade nano device research. This is why SIMON2.0 simulation software were earnestly adhered. The TLG memory cell is configured in Fig. 5.

Only to accomplish the anticipated read/write operation on this cell, the control points is made high i.e., 1. Here logic 0 is made by giving input voltage much less than 1mV and the logic 1 is provided by making the input voltage equal to 1mV. Thus the circuit functions in very low voltage.

#### C. Simulation of the Memory Circuit

As stated, the SIMON 2.0 based memory cell was constituted in a monolithic fashion. For simulation the authors adhered to piece-wise constant type simulation and applied the combinations of logic '0' and logic '1' into the inputs. The significance of such input handling is that it resembles more realistic approach compared to other available conventional tools. Several iterations were made before final results could be obtained.

### IV. RESULTS AND PERFORMANCE ANALYSIS

After several approximations the authors deliberate the following attributes of the proposed memory cell.

#### A. Write Operation

For writing data into this memory cell, the authors intuitively selected the following control signals.

$$X\text{-select} = 1$$

$$Y\text{-select} = 1$$

$$\overline{RD}/WR = 1$$

The electron transport phenomena for the 'Write' operation is synchronized with the positive edge of the clock pulse. Then the Coulomb Energy enhances manifold to overcome Coulomb Blockade. The potentiality to transfer the electrons increases in staircase like structure, if the graph of the same is considered.

The write operation is performed at least 2000 times faster compared to conventional topology.

#### B. Read Operation

For reading the data, the memory cell has to execute in the ensuing manoeuvre

$$X\text{-select} = 1$$

$$Y\text{-select} = 1$$

$$\overline{RD}/WR = 0$$

X-select and Y-select validates the two TLG ANDings in the mid-section of the proposed model, but the  $\overline{RD}/WR$  remains 0 i.e., it is disabled. Subsequently, the first three TLG AND gates are sporadically enabled and concurrently the same befalls for the last output driving TLG AND gate. This guarantees that the consecutive last two TLG AND gates is enabled and the output is physically driven at the data line. A detailed study of the robustness indicates that the reading operation can be accomplished at least 2000 time earlier than the conventional CMOS topology.

### V. CONCLUSION

This short communication is an ephemeral study of TLGs in nano electronic device research. The authors investigated the performance of TLG made nano memory cell using the simulation tool SIMON 2.0. It renders excellent performance when compared to conventional CMOS made memory cells. Thus the authors conclude that the same can be articulated in future nano device technology.

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LIST OF FIGURES

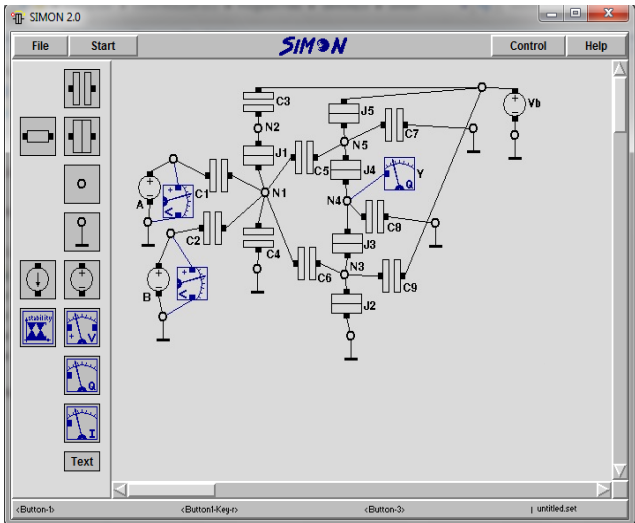


Fig.1: TLG ANDing using SIMON 2.0

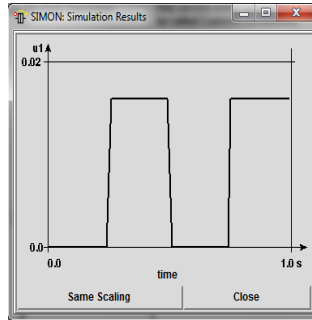


Fig.2: TLG AND A input

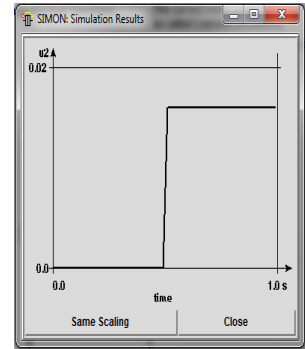


Fig.3: TLG AND B input

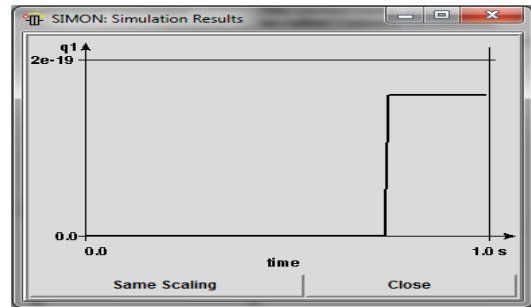


Fig.4: TLG AND gate Y output

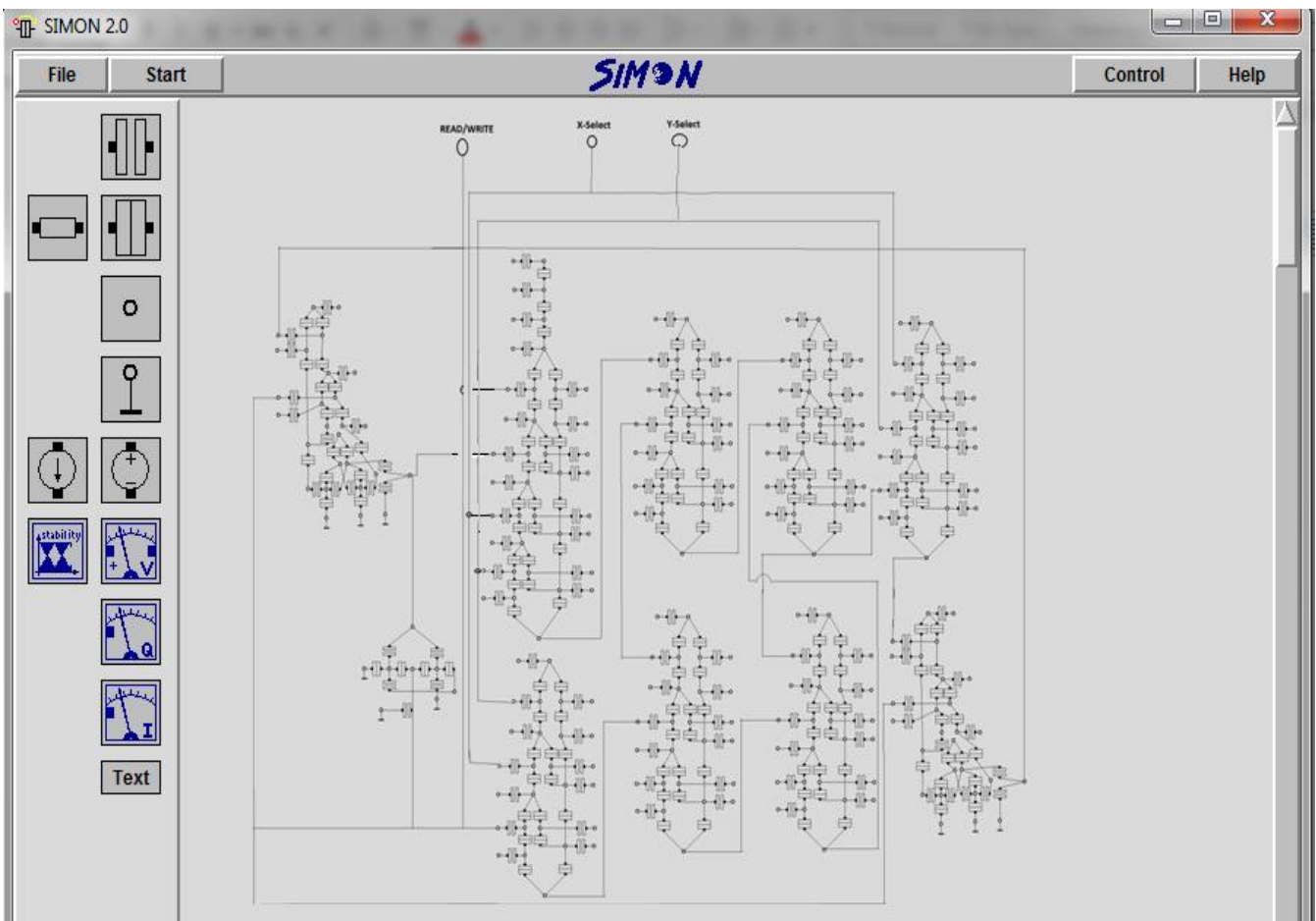


Fig.5: TLC based nano memory cell simulation using SIMON 2.0