Four Quadrant Operation of Chopper – Fed Separately Excited DC Motor by Decoupled PWM Control Using Digital Signal Processor

Ainee Ansaari, Hardik Mehta

***Abstract*— DC Motors are used extensively in adjustable speed drives and position control applications. This paper proposes a method to control the speed and direction control of a DC motor by using a four quadrant DC-DC chopper. The speed below the base speed can be controlled by armature voltage control method. IGBTs are used for the switching operation of the chopper. The gates of these IGBTs are given Pulse Width Modulation which provides the four quadrant operation. This Pulse Width Modulation is generated by programming the Digital Signal Processor using the Code Composer Software. The above model is simulated in MATLAB.**

***Index Terms*— Four quadrant DC-DC chopper, armature voltage control method, Pulse Width Modulation, Digital Signal Processor, Code Composer Software.**

I. INTRODUCTION

Developments of high performance motor drives are very essential for industrial applications. A high performance motor drive system must have good dynamic speed command tracking and load regulating response. DC motors provide excellent control of speed for acceleration and deceleration. The power supply of a DC motor connects directly to the field of the motor which allows for precise voltage control, and is necessary for speed and torque control applications.

DC drives, because of their simplicity, ease of application, reliability and favorable cost have long been a backbone of industrial applications. DC drives are less complex as compared to AC drives system. DC drives are normally less expensive for low horsepower ratings. DC regenerative drives are available for applications requiring continuous regeneration for overhauling loads. AC drives with this capability would be more complex and expensive. Maintenance of commutator is minimal. DC motors are capable of providing starting and accelerating torques in excess of 400% of rated [2].

DC motors have long been the primary means of electric traction. They are also used for mobile equipment such as golf carts, quarry and mining applications.

DC motor is considered as a SISO (Single Input and Single Output) system having torque/speed characteristics compatible with most mechanical loads. This makes a DC motor controllable over a wide range of speeds by proper adjustment of the terminal voltage. DC motors are always a good option for advanced control algorithm because the theory of dc motor speed control is extendable to other types of motors as well.

The speed control techniques in separately excited DC motor are [2]:

- By varying the armature voltage for below rated speed.
- By varying field flux should to achieve speed above the rated speed.

Different methods for speed control of DC motor:

- Traditional armature voltage control method using rheostatic method for low power DC motors.
- Use of Pulse Width Modulation Techniques.
- Neural Network Controllers.
- Constant power motor field weakening controller based on load-adaptive multi-input multi-output linearization technique (for high speed regimes).
- Single phase uniform PWM AC-DC buck-boost converter with only one switching device used for armature voltage control.
- Using NARMA-L2 (Non-linear Auto-regressive Moving Average) controller for the constant torque region.

Achieving speed control by using pulse-width modulation (PWM) decreases energy consumption, improve motor reliability and reduce acoustics while providing wider operational speed bandwidth.

PWM is the preferred approach to regulating motor speed for the following main reasons:

- It is energy efficient because it doesn't generate additional heat.
- It improves motor reliability because the motor doesn't run at full speed all the time. It improves the acoustics of the motor with high-frequency driving signals.
- It provides thermal engineers with added operational speed bandwidth because the motor can run at either high or remarkably low speeds.

The operation of the proposed circuit is explained in section II which includes the operation of four quadrant chopper, IGBT, interfacing circuit for ADC, Digital Signal Processor and gate driver circuit. The simulation models and results are represented in section III. The conclusion is provided in section IV and future cope in section V.

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II. Operation of the Proposed Circuit

A. Four Quadrant Chopper

A chopper is a static device that converts fixed DC input to a variable DC output voltage directly. A chopper may be thought of as an AC transformer since they behave in an identical manner. It's also known as DC-to-DC converter. It's widely used for motor control. It's also used in regenerative braking. Essentially, a chopper is an electronic switch that is used to interrupt one signal under the control of another [2].

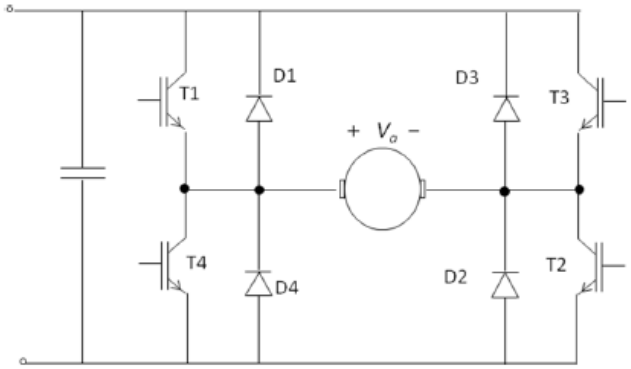

Fig.1. Four Quadrant Chopper Circuit

The switches in the four quadrant chopper can be switched in two different modes:

- The output voltage swings in both directions i.e. from $+V_{dc}$ to $-V_{dc}$. This mode of switching is referred to as PWM with bipolar voltage switching.
- The output voltage swings either from zero to $+V_{dc}$ or zero to $-V_{dc}$. This mode of switching is referred to as PWM with unipolar voltage switching.

The four quadrant chopper operates in the four quadrants in the following ways [4]:

(i) **Quadrant I**: In the first quadrant, the voltage and current are positive making the power is positive. In this case, the power flows from source to load. In this operation T1is ON, T4 is OFF, T2 is continuously ON and T3 is continuously OFF. T1 and T2 are conducting in this mode.
(ii) **Quadrant 2** : In the second quadrant, the voltage is still positive but the current is negative. Therefore, the power is negative. In this case, the power flows from load to source and this can happen if the load is inductive or back emf source such as a dc motor .Here T1 is OFF, T4 is ON,T2 is continuously ON and T3 is continuously OFF. As the inductor current cannot be changed instantaneously, D4 and T2 will be freewheeling the current.
(iii) **Quadrant 3** : In the third quadrant both the voltage and current are negative but the power is positive. In this case, the power flows from source to load. In this operation T3is ON, T2 is OFF, T4 is continuously ON and T1 is continuously OFF. T3 and T4 are conducting in this mode.
(iv) **Quadrant 4** : In the fourth quadrant voltage is negative but current is positive. The power is therefore negative. Here T3 is OFF, T2 is ON,T4 is continuously ON and T1 is continuously OFF . As the inductor current cannot be changed instantaneously, D2 and T4 will be freewheeling the current.

B. IGBT

The insulated-gate bipolar transistor (IGBT) is a three-terminal power semiconductor device primarily used as an electronic switch for combining high efficiency and fast switching. It switches electric power in many modern appliances: variable-frequency drives (VFDs), electric cars, trains, variable speed refrigerators, air-conditioners and even stereo systems with switching amplifiers. Since it is designed to turn on and off rapidly, amplifiers that use it often synthesize complex waveforms with pulse width modulation and low-pass filters [3].
The IGBT combines the simple gate-drive characteristics of the MOSFETs with the high-current and low-saturation-voltage capability of bipolar transistors. The IGBT combines an isolated gate FET for the control input, and a bipolar power transistor as a switch, in a single device. It has a very low on-state voltage drop due to conductivity modulation and has superior on-state current density. So smaller chip size is possible and the cost can be reduced. It has low driving power and a simple drive circuit due to the input MOS gate structure. It can be easily controlled as compared to current controlled devices (thyristor, BJT) in high voltage and high current applications. It has superior current conduction capability compared with the bipolar transistor. It also has excellent forward and reverse blocking capabilities because of its wide Safe Operating Area.
The main performance switching characteristics of power semiconductor switching devices are the turn-on and turn-off switching transients in addition to the safe operating area (SOA) of the device [5]-[6].

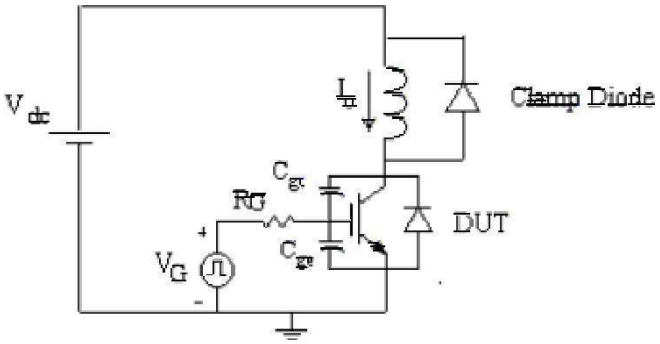

Fig.2. Inductive Load Circuit

(i) **Turn-ON transients**: The turn-on switching transient of an IGBT with an inductive load is shown in Fig. 3. With gate voltage applied across the gate to emitter terminals of the IGBT, the gate to emitter voltage rises up in an exponential fashion from zero to $V_{GE(th)}$ due to the circuit gate resistance (R_G) and the gate to emitter capacitance (C_{GE}). The Miller effect capacitance (C_{GC}) effect is very small due to the high voltage across the device terminals.
Beyond $V_{GE(th)}$, the gate to emitter voltage continues to rise as before and the drain current begins to increase linearly as shown above. Due to the clamp diode, the collector to emitter voltage remains at V_{dc} as the IGBT current is less than Io. Once the IGBT is carrying the full load current but is still in the active region, the gate to emitter voltage becomes

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temporarily clamped to $V_{GE,Io}$, which is the voltage required to maintain the IGBT current at Io. At this stage, the collector to emitter voltage starts decreasing in two distinctive intervals t_{fv1} and t_{fv2}. The first time interval corresponds to the traverse through the active region while the second time interval corresponds to the completion of the transient in the ohmic region.

During these intervals, the Miller capacitance becomes significant where it discharges to maintain the gate to source voltage constant. When the Miller capacitance is fully discharged, the gate to emitter voltage is allowed to charge up to V_G and the IGBT goes into deep saturation. The resultant turn on switching losses are shown in the above figure. The on energy loss is approximately estimated via,

$$E_{ON} = (V_{dc}I_O/2)t_{ON}$$

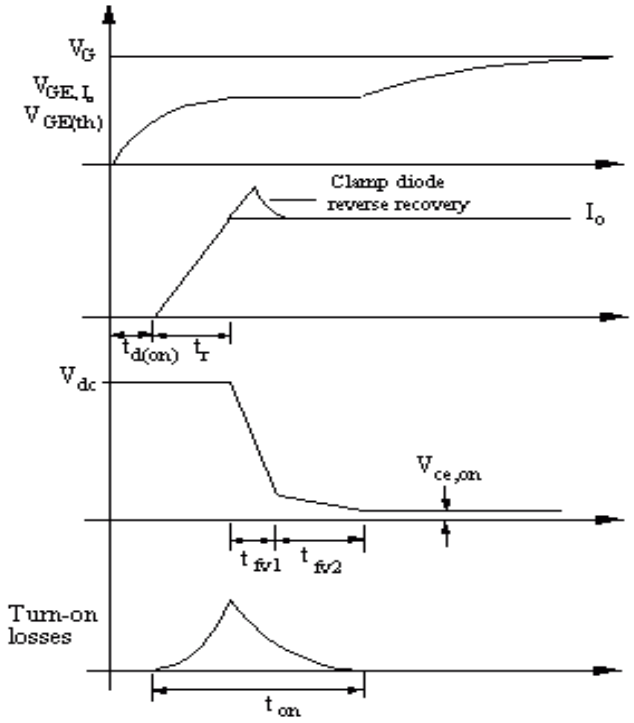

Fig. 3. IGBT turn-on switching transient with inductive load

The above switching waveforms are ideal in the since that the clamp diode reverse recovery effects are neglected. If these effects are included, an additional spike in the current waveform results as shown in the previous figure. As a result, additional energy losses will be incurred within the device.

(ii) **Turn-OFF transients**: The turn-off switching transients of an IGBT with an inductive load are shown in Fig. 3.5. When a negative gate signal is applied across the gate to emitter junction, the gate to emitter voltage starts decreasing in a linear fashion. Once the gate to emitter voltage drops below the threshold voltage ($V_{GE(th)}$), the collector to emitter voltage starts increasing linearly. The IGBT current remains constant during this mode since the clamp diode is off. When the collector to emitter voltage reaches the dc input voltage, the clamp diode starts conducting and the IGBT current falls down linearly. The rapid drop in the IGBT current occurs during the time interval tfi1, which corresponds, to the turn-off of the MOSFET part of the IGBT (Fig. 4). The tailing of the collector current during the second interval t_{fi2} is due to the stored charge in the n- drift region of the device. This is because the MOSFET is off and there is no reverse voltage applied to the IGBT terminals that could generate a negative drain current so as to remove the stored charge. The only way for stored charge removal is by recombination within the n- drift region. Since it is desirable that the excess carriers lifetime be large to reduce the on-state voltage drop, the duration of the tail current becomes long. This will result in additional switching losses within the device. This time increases also with temperature similar to the tailing effect in BJTs. Hence, a tradeoff between the on-state voltage drop and faster turn-off times must be made.

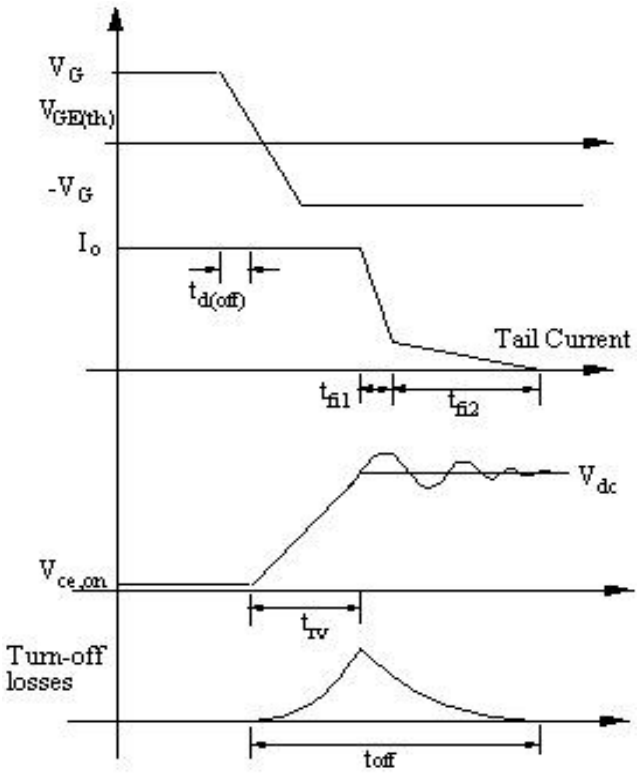

Fig. 4. IGBT turn-off switching transient with inductive load

(iii) **Safe Operating Area:** The safe operating area (SOA) of a power semiconductor device is a graphical representation of the maximum operational voltage and current limits (i-v) of the device subjected to various constraints. The forward bias safe operating area (FBSOA) and the reverse bias safe operating area (RBSOA) represent the device SOA with the gate emitter junction forward biased or reverse biased, respectively. The IGBT has robust SOA during both turn-on and turn off.

The upper half corner of the RBSOA is progressively cut out which reduces the RBSOA as the rate of change of the collector to emitter voltage across the device, dV_{ce}/dt, is increased. The RBSOA is reduced as the dV_{ce}/dt is increased to avoid latch up within the device. This condition exists when higher values of dV_{ce}/dt are applied may give to the rise to a pulse of forward decaying current in the body region of the device that acts as a pulse of gate current that can turn on the device. Fortunately, the dV_{ce}/dt values that would cause latch up in IGBTs are much higher compared to other devices.

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The maximum value of I_{CM} is set to avoid latch up which is determined based on the dynamic latch up condition. In addition, a maximum V_{GE} voltage is specified in order to limit the current during a fault condition to I_{CM} by forcing the device out of the on-state into the active region where the current becomes constant regardless of the drain to source voltage. The IGBT must be turned off under these conditions as quickly as possible to avoid excessive dissipation. The avoidance of latch up and the continuous gate control over the collector current are very desirable features.

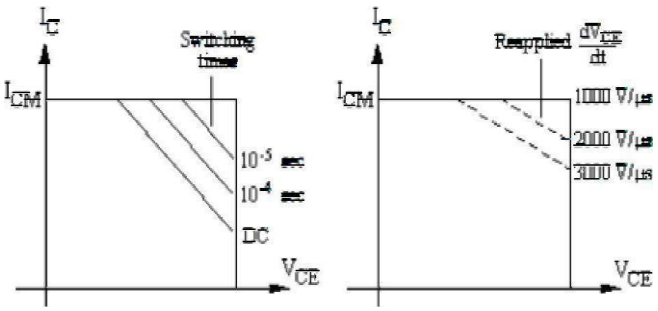

Fig. 5. FBSOA and RBSOA of an IGBT

(iv) **IGBT gate drive requirements:** IGBTs are voltage controlled devices and require gate voltage to establish collector-to-emitter conduction. Recommended gate drive circuitry includes substantial ion and off biasing.

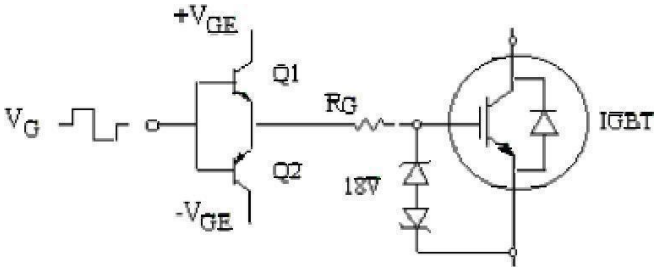

Fig. 6. Typical gate drive circuitry

The following should be considered for gate drive layout:
1. Minimize parasitic inductance between the driver output stage and the IGBT (minimizing the loop area).
2. Minimize noise coupling via proper shielding techniques.
3. Utilize gate clamp protections (TVS) to minimize over voltage across gate terminals .
4. Utilize twisted pairs, preferably shielded, for indirect connection between the driver and the IGBT.
5. With opto coupling isolation, a minimum of 10,000 V/ms transient immunity must be provided.

C. Interfacing Circuit for Analog to Digital Converter

For the Analog to Digital Converter we require a signal of 0-3.3V. An input of -10 to 10V is given to the interfacing circuit and we get an output of 0-3.3V . The circuit has four Operational Amplifiers, as seen in Fig. 7: One Operational Amplifier is for buffering, one Operational Amplifier is for inverting and two Operational Amplifiers for setting the voltage to the range 0-3.3V .

A pot is used to give the input of -10 to 10V to the interfacing circuit. We also require a power supply of 12V DC. To obtain this 12 V DC we design a rectifier circuit.

D. Digital Signal Processor

The Texas Instruments TMS320LF2407 DSP Controller (referred to as the LF2407 in this text) is a programmable digital controller. TMS320 DSP has an architecture designed especially for real-time signal processing and control system applications. It uses a 16-bit word-length along with 32-bit registers for storing intermediate results [1].
The LF2407 DSP controller offers 40 million instructions per second (MIPS) performance. This high processing speed of the C2xx CPU allows users to compute parameters in real time rather than look up approximations from tables stored in memory. This fast performance is well suited for processing control parameters in applications such as notch filters or sensor less motor control algorithms where a large amount of

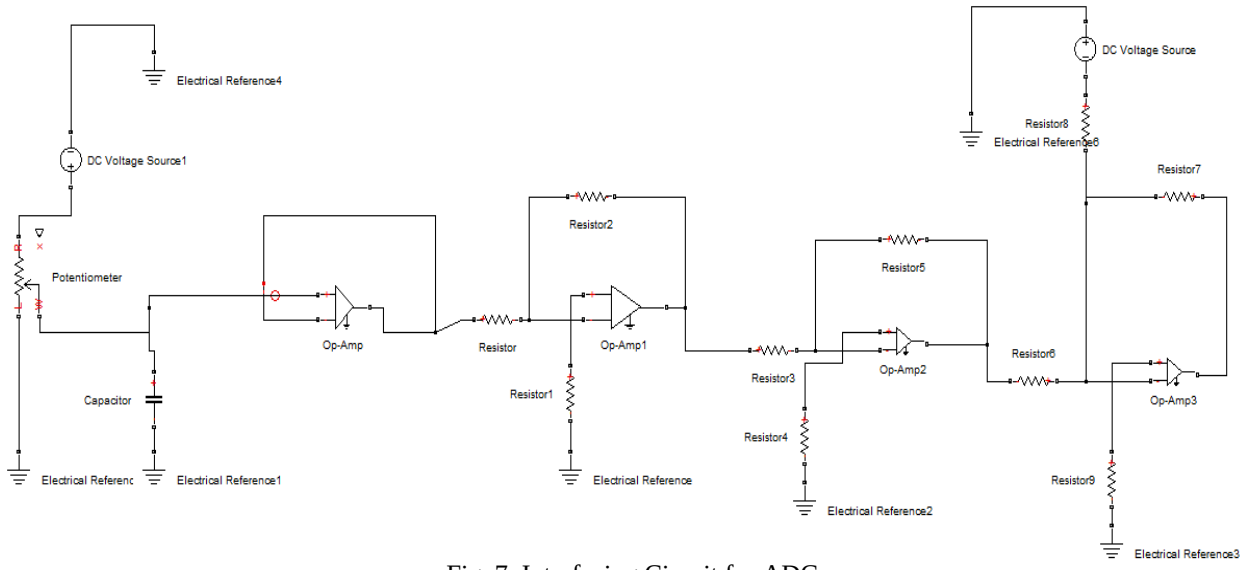

Fig. 7. Interfacing Circuit for ADC

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calculations must be computed quickly.
Its applications range from analog to digital conversion to pulse width modulation (PWM) generation.
The LF2407 peripheral set includes:

- Two Event Managers (A and B)
- General Purpose (GP) timers
- PWM generators for digital motor control
- Analog-to-digital converter
- Controller Area Network (CAN) interface
- Serial Peripheral Interface (SPI) – synchronous serial port
- Serial Communications Interface (SCI) – asynchronous serial port
- General-Purpose bi-directional digital I/O (GPIO) pins
- Watchdog Timer ("time-out" DSP reset device for system integrity)

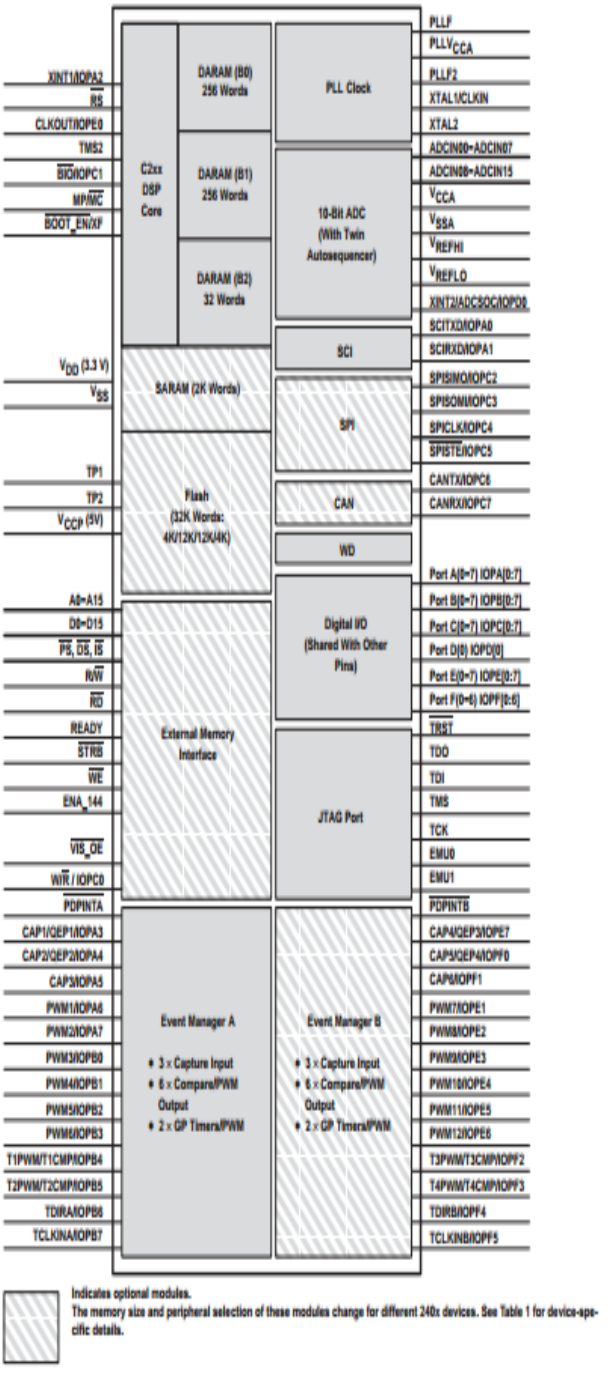

Fig. 8. Pin Diagram of Digital Signal Processor

(i) **Event Managers (EVA, EVB)**: There are two Event Managers on the LF2407, the EVA and EVB. The Event Manager is the most important peripheral in digital motor control. It contains the necessary functions needed to control electromechanical devices. Each EV is composed of functional "blocks" including timers, comparators, capture units for triggering on an event, PWM logic circuits, quadrature-encoder–pulse (QEP) circuits, and interrupt logic.
(ii) **The Analog-to-Digital Converter (ADC)**: The ADC on the LF2407 is used whenever an external analog signal needs to be sampled and converted to a digital number. Examples of ADC applications range from sampling a control signal for use in a digital notch filtering algorithm or using the ADC in a control feedback loop to monitor motor performance.
(iii) **The Control Area Network (CAN) Module**: The CAN module is used for multi-master serial communication between external hardware. The CAN bus has a high level of data integrity and is ideal for operation in noisy environments such as in an automobile, or industrial environments that require reliable communication and data integrity.
(iv) **Serial Peripheral Interface (SPI) and Serial Communications Interface (SCI)**: The SPI is a high-speed synchronous communication port that is mainly used for communicating between the DSP and external peripherals or another DSP device. Typical uses of the SPI include communication with external shift registers, display drivers, or ADCs.
The SCI is an asynchronous communication port that supports asynchronous serial (UART) digital communication between the CPU and other asynchronous peripherals that use the standard NRZ (non-return-to-zero) format. It is useful in communication between external devices and the DSP.
(v) **Watchdog Timer (WD)**: The Watchdog timer (WD) peripheral monitors software and hardware operations and asserts a system reset when its internal counter overflows. The WD timer (when enabled) will count for a specific amount of time. It is necessary for the user's software to reset the WD timer periodically so that an unwanted reset does not occur. If for some reason there is a CPU disruption, the watchdog will generate a system reset.
(vi) **General Purpose Bi-Directional Digital I/O (GPIO) Pins**: There are only a finite number of pins available on the LF2407 device, many of the pins are multiplexed to either their primary function or the secondary GPIO function. In most cases, a pin's second function will be as a general-purpose input/output pin. The GPIO capability of the LF2407 is very useful as a means of controlling the functionality of pins and also provides another method to input or output data to and from the device.
(vii) **Joint Test Action Group (JTAG) Port**: The JTAG port provides a standard method of interfacing a personal computer with the DSP controller for emulation and development. The JTAG module allows the PC to take full control over the DSP processor while Code Composer Studio is running.
(viii) **Phase Locked Loop (PLL) Clock Module**: The phase locked loop (PLL) module is basically an input clock multiplier that allows the user to control the input clocking frequency to the DSP core. External to the LF2407, a clock reference (can oscillator/crystal) is generated. This signal is fed into the LF2407 and is multiplied or divided by the PLL. This new (higher or lower frequency) clock signal is then used

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to clock the DSP core. The LF2407's PLL allows the user to select a multiplication factor ranging from 0.5X to 4X that of the external clock signal. The default value of the PLL is 4X.

(ix) **Memory Allocation Spaces**: The LF2407 DSP Controller has three different allocations of memory it can use: Data, Program, and I/O memory space. Data space is used for program calculations, look-up tables, and any other memory used by an algorithm. Data memory can be in the form of the on-chip random access memory (RAM) or external RAM. Program memory is the location of user's program code. I/O space is not really memory but a virtual memory address used to output data to peripherals external to the LF2407. For example, the digital-to-analog converter (DAC) on the Spectrum Digital evaluation module is accessed with I/O memory.

(x) **Triangular Carrier Wave Generation**: The continuous up/down counting mode is useful in generation symmetric PWM waveforms.

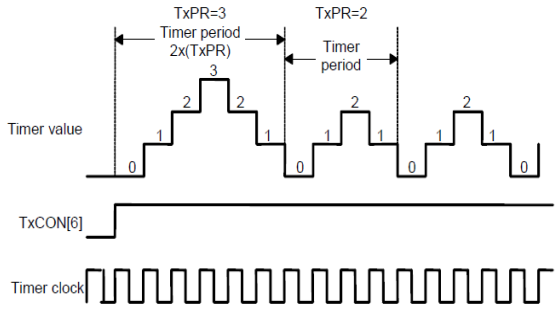

Fig. 9. Triangular Carrier Wave Generation

(xi) **The Compare Unit**: The ON and OFF time of the pulse is directly dependent on the value loaded into the compare unit register. Each compare unit has two associated PWM outputs that toggle on the same compare match.

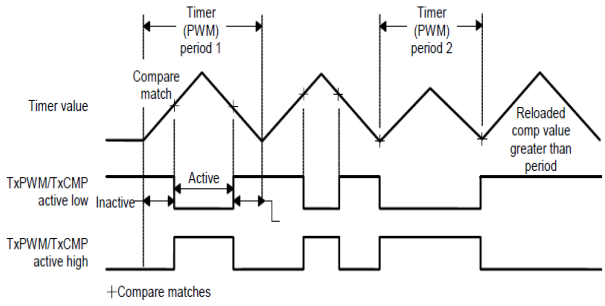

Fig. 10. The Compare Unit

(xii) **Dead Band Generation**: Unlike the GP Timer Compare PWM generation, the compare unit allows PWM outputs for a programmable dead band. It solves the problem of source getting short-circuited due to turn-off delay. Bits 8-11 in DBTCONx decide the amount of dead band to be given [7]-[9].

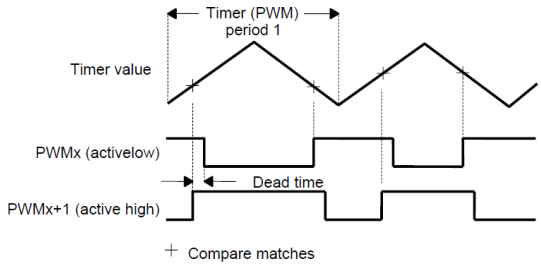

Fig. 11. Dead Band Generation

(xiii) **Scheduling of the process**:

- For decoupled control, two identical carrier waves are generated using one timer in each EVM.
- Compare unit register is loaded with digital value of speed command.
- For the left leg ,Timer 1 generates carrier wave of required frequency. Timer 1 Counter value is continuously compared with Compare Unit register (CMPR1).
- Similarly Timer 3 and CMPR4 for the right leg.
- After every carrier frequency cycle, interrupt is generated from Timer 1, which is used to give SOC for A/D conversion.
- The compare registers are shadowed, whenever they are written to, the value is automatically stored first into a buffer register and can be written to the real register at any time.
- We choose to write into real register when underflow occurs. This way, compare value is used for comparison one cycle after its computation.

E. Gate Drive Circuit

The Pulse Width Modulation obtained from the Digital Signal Processor (DSP) is weak and has a low voltage level. For the triggering of the gates of IGBTs we require rated gate triggering voltage. The obtained Pulse width Modulation signal should be boosted to an appropriate voltage level. To boost the Pulse Width Modulation signal we require the driver circuit. We need two gate drivers, one for each leg. The pulses from processor are only 3.3V in magnitude. The Gate driver boosts the pulses to +15V to -10V.The gate drivers produce complimentary pulses with a dead-band of 10 micro seconds. It also provides isolation of control circuit and power circuit. This circuit consists of hybrid driver IC m57962l, opto coupler IC MCT6, zener diodes and short circuit protection circuit.

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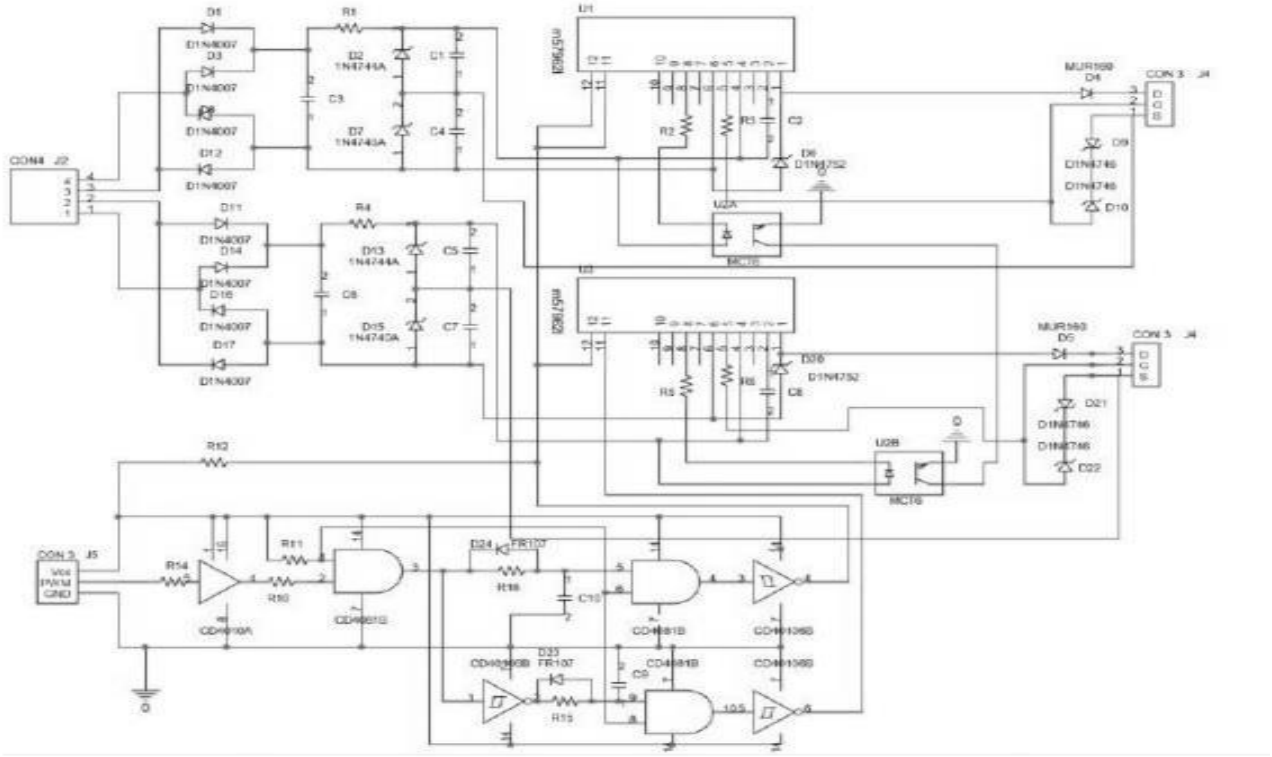

III. SIMULATION

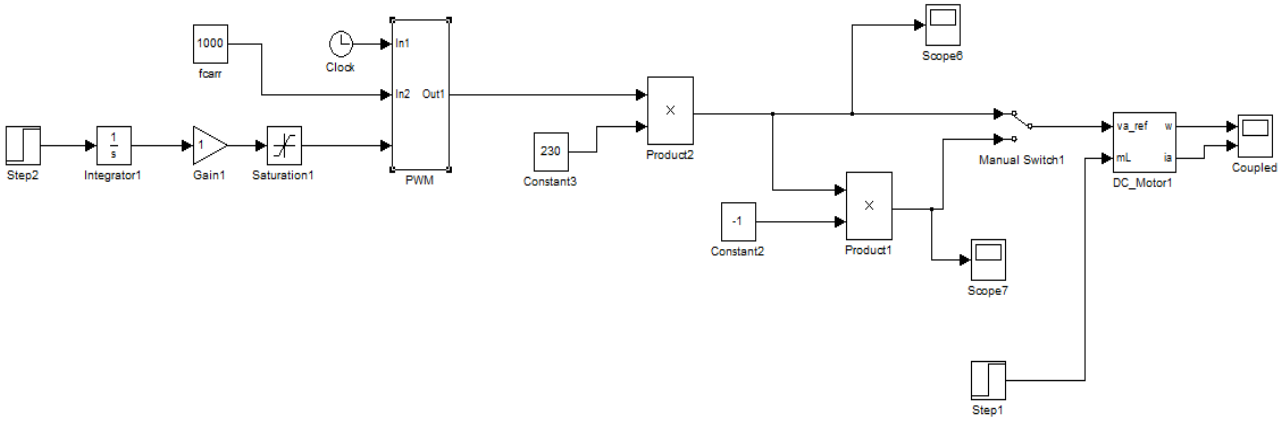

Fig. 13. Simulation Model of DC Motor Control Using Chopper Drive

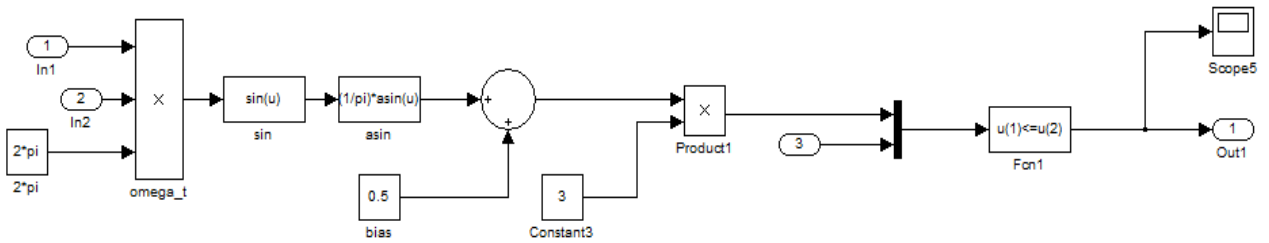

Fig. 14. Pulse Width Modulation Generation

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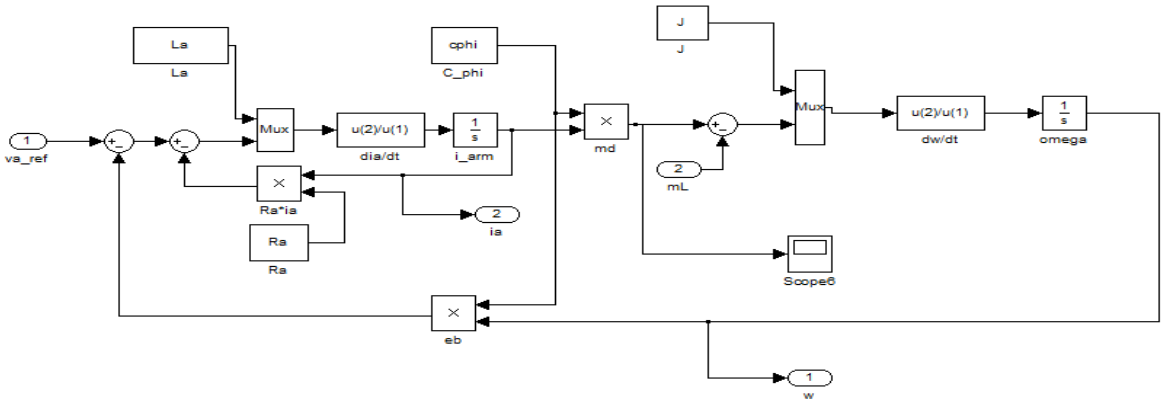

Fig. 15. DC Motor Model

(i) **Forward Motoring**: The output voltage of the chopper is varied from 0V to required voltage in 1 second. The modulating signal is varied from zero to its maximum value in 1 second. The transient period of the motor is 2 seconds. So we observe changes after 1st second and 2nd second .

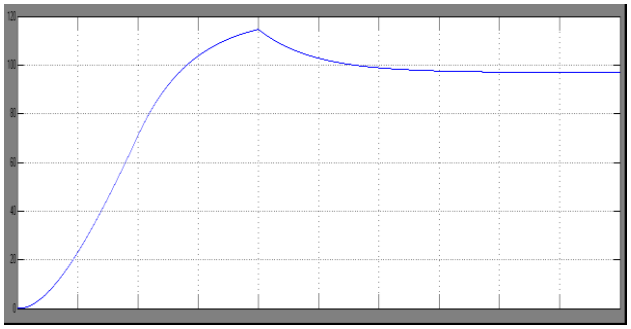

Fig. 16. Speed Characteristics for Forward Motoring

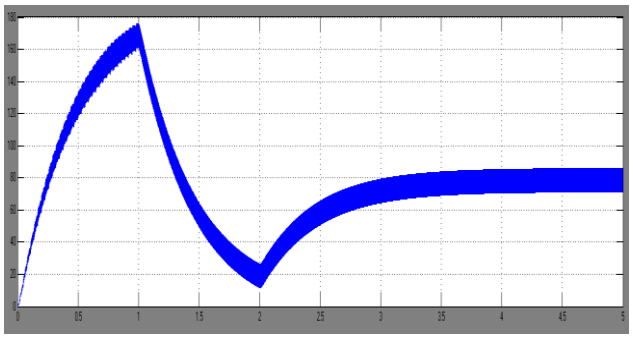

Fig. 17. Current Characteristics for Forward Motoring

(ii) **Reverse Motoring**: The output voltage of the chopper is varied from 0V to required voltage in 1 second. The modulating signal is varied from zero to its maximum value in 1 second. The transient period of the motor is 2 seconds. So we observe changes after 1st second and 2nd second .

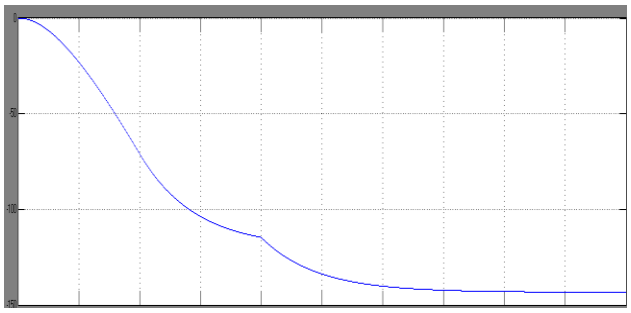

Fig. 18. Speed Characteristics for Reverse Motoring

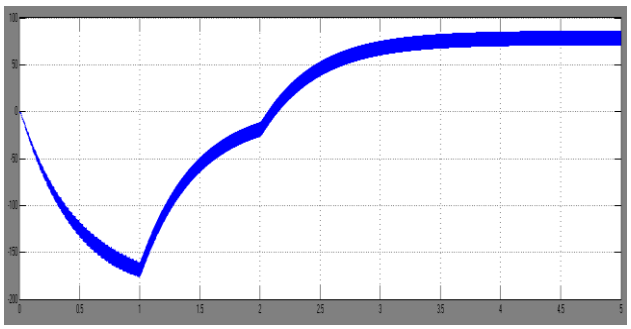

Fig. 19. Current Characteristics for Reverse Motoring

(iii) **Forward Motoring**: The output voltage of the chopper is varied from 0V to required voltage in 2 second. The modulating signal is varied from zero to its maximum value in 2 second. The transient period of the motor is 2 seconds. So we observe a change only after the 2nd second.

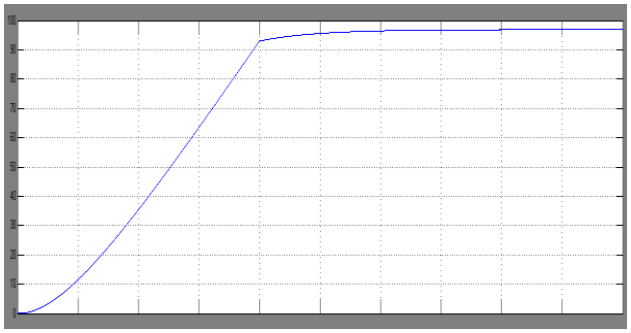

Fig. 20. Speed Characteristics for Forward Motoring

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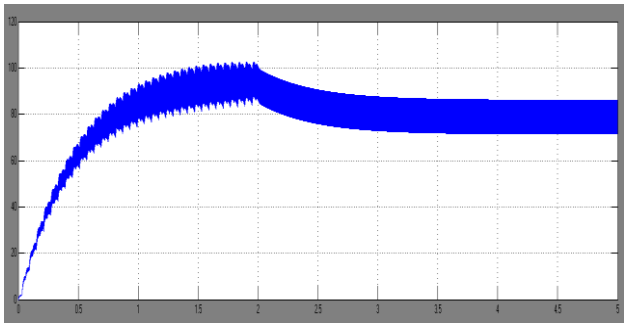

Fig. 20. Current Characteristics for Forward Motoring

(iv) **Reverse Motoring**: The output voltage of the chopper is varied from 0V to required voltage in 2 second. The modulating signal is varied from zero to its maximum value in 2 second. The transient period of the motor is 2 seconds. So we observe a change only after the 2nd second .

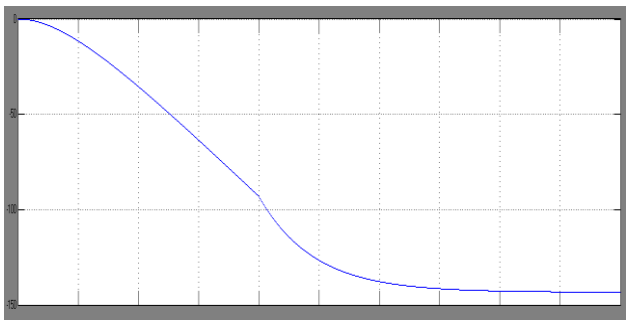

Fig. 21. Speed Characteristics for Reverse Motoring

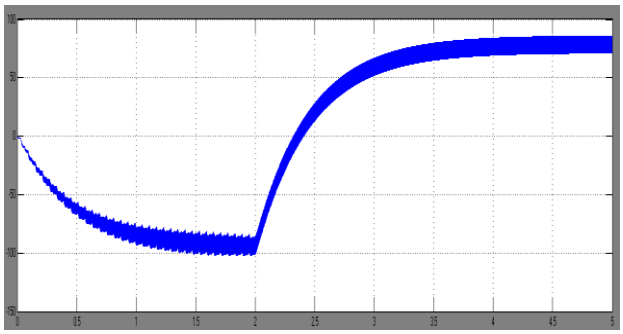

Fig. 22. Current Characteristics for Reverse Motoring

IV. HARDWARE RESULTS

Analog Control Input	Armature Voltage (at No Load)
0.11	-27.6
0.51	-20
0.72	-14.5
0.90	-10.2
1.32	-0.11
2.23	18.5
2.54	22.5
2.91	26.2
3.1	29.8

Table 1. Observed Armature Voltage at No Load

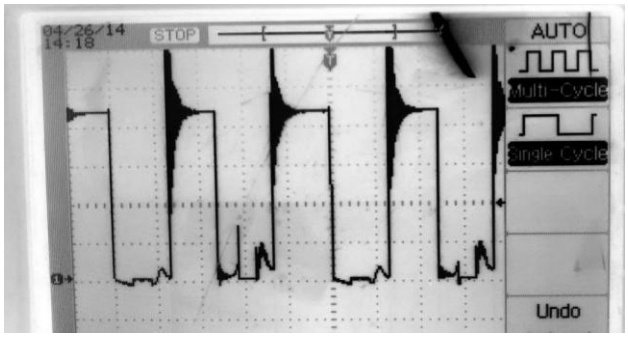

Fig. 23. Output for analog input of 1.54V

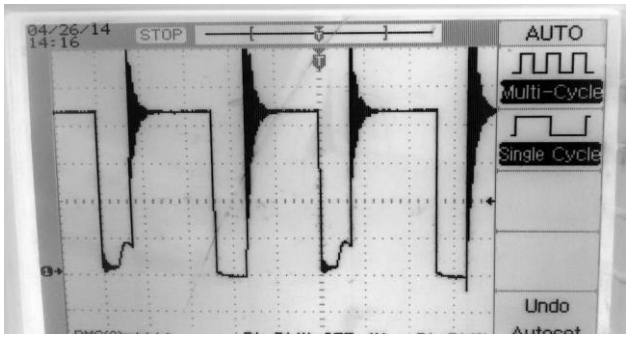

Fig. 24. Output for analog input of 2.2V

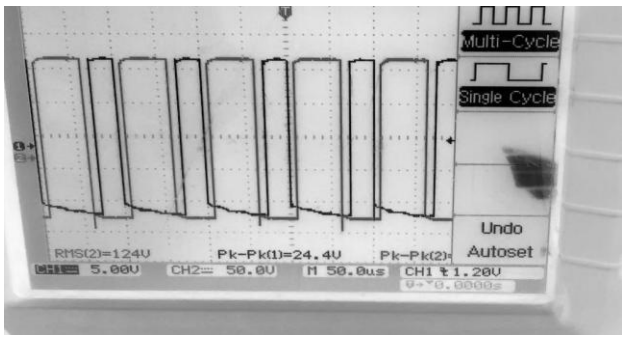

Fig. 25. Complementary pulses for input of 1.2V

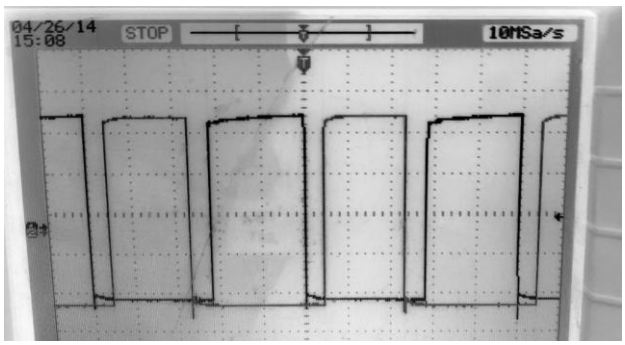

Fig. 26. Complementary pulses for input of 1.7V

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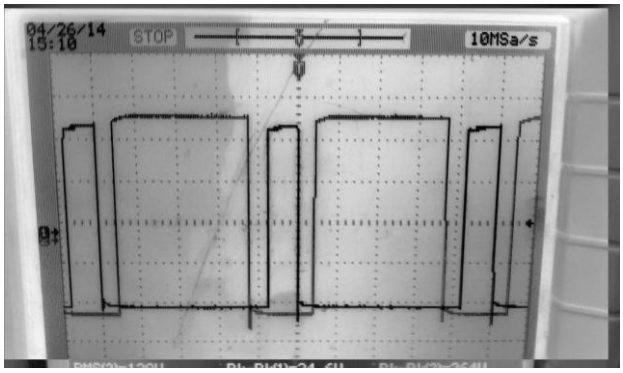

Fig. 27. Complementary pulses for input of 2.2V

V. Conclusion

Gate pulses for each of the four switching devices were obtained successfully. The duty ratio of those pulses varied finely when the analog control input was varied. Gate drivers successfully boosted the gate pulses to +15V and -10V. The power circuit and the control circuit were successfully isolated. Variable armature voltage was observed, which varied according to the control input. Negative as well as positive voltages were observed across terminals.

Future Scope

The speed of the motor has been varied successfully in an open loop manner in accordance with the change in duty ratio. Future scope is to control the speed of the motor in a closed loop manner by taking a feedback from the taco generator and giving it as a feedback to the DSP. Where in the DSP, it compares the desired value and the actual value and gives an error voltage which is given to the motor through an interface circuit. In this manner, the speed of the motor can be controlled as per the user.

Acknowledgment

We consider it a great privilege to express our deep gratitude to many respected personalities who guided, inspired and helped us in the successful completion of our project. First and foremost, we would like to express our deepest gratitude to our guide Prof. V. T. Somasekhar, Department of Electrical Engineering, National Institute of Technology, Warangal, for his constant supervision, guidance, suggestions and invaluable encouragement during this project. We are grateful to Prof. N. Subramanyam, Head, Department of Electrical Engineering, National Institute of Technology, Warangal, for his moral support to carry out this project. We wish to thank all the staff members in the department for their kind cooperation and support given throughout our project work. We are also thankful to all of our friends who have given valuable suggestions and assistance in all stages of the development of the project. Finally, we would like to dedicate this work to our parents who have provided support and encouragement during every part of our life.

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