# Hybrid CMOS-SET Decision Making Nano IC: A Case Study

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***Abstract*— Single Electron Transistor (SET) ascended as a novel switching device that requires controlled electron tunneling to amplify current. It offers current conduction features identical to CMOS switches. Researchers have proposed several hybrid CMOS-SET logic circuits in the last few years. This letter intends to enumerate hybrid CMOS-SET logic gates in designing advanced decision making nano ICs. Later the authors here extend to validate the proposed decision making nano IC by simulating it in different sections using SPICE simulator comprised of the physical device model of SET.**

***Index Terms*—Coulomb Blockade, SET, Hybrid CMOS SET, Transmission logic.**

## I. INTRODUCTION

The SET tunneling technology ushers new ventures in ICs owing to its small size and low power consumption topographies. This makes SETs a promising substitute in post CMOS era as per ITRS 2003 [….]. Undoubtedly, SET posses excellent merits in nano-scale feature; i.e., nano-size, simplistic and straight forward structure, robustness, high integration density, extreme low power consumption, exclusive Coulomb blockade oscillation features and moreover, they exhibit better possibilities in combining with CMOS [1]. To the contrary it suffers major drawbacks of poor current driving capabilities and cannot be functioned in room temperature. This leads to some uncertainty for SETs in wiping out CMOS entirely in very near future. Conversely, CMOS deliver high voltage gain, sizeable driving speed and also have high input impedance. Thus an equitable study on both reflects CMOS can compensate the intrinsic drawbacks of SET. Amid such, the proposition to construct the circuit in hybrid form by a combination of SET and conventional CMOS for LSI, MSI, VLSI and ULSI circuits has paved a new horizon in device research [2].

In this paper, initially the operation of hybrid CMOS-SET circuit is pondered over. Then after few different hybrid logic gates is studied. Subsequently the authors propose a hybrid CMOS-SET based decision making sub-system. Finally the proposed model is subdivided and periodically verified by means of SPICE simulation packages.

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## II. MANEUVER OF HYBRID CMOS-SET LOGIC GATES

The modeling of Single electron transmission gate using equivalent circuit was demonstrated by Yukinon Ono et al [7]. Fellow researchers conceptually articulated SET-MOS quaternary transmission gate intriguing the tunneling metaphor [8]. The orthodox design of the novel Hybrid CMOS-SET Transmission gate is depicted in fig. 1.

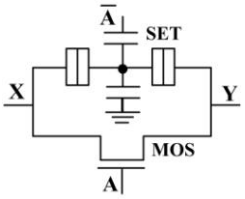


Figure 1. Simple Metaphor of Hybrid CMOS-SET Transmission Gate

The consequential hybrid logic circuits are premeditated based on the successive implementation of the functionality of this gate. The basis of such impressive design is having a pull-up / pull-down network operated by an electrical switch. Noticeably, the switching speed improves along with the gate fan-out and overall performance like characteristics [9,10]. The underlying tactic is to place the SET and an nMOS transistor in parallel and control it by a complementary switching signal. When the switch is closed A = 1 and open when A=0.

So, in turn the output obtained is $Y = A.X$ (1)

$$Y = \begin{cases} 0 & if \quad A = 0 \\ x & if \quad A = 1 \end{cases} \quad (2)$$



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The trend of amalgamating SET and CMOS motivated the Researchers at Delft University in Netherlands to develop a SPICE model SET circuit simulation package [11] using the same Orthodox theory.

*A. Design of Hybrid CMOS-SET Inverter, AND and, OR logic gates.*

The hybrid CMOS-SET based simple inverter realization [12] is simulated and its circuit diagram including the input-output waveforms are depicted in fig. 2 and 3 respectively. The circuits are designed and simulated by SPICE simulator and simulated waveforms are shown in fig. 7

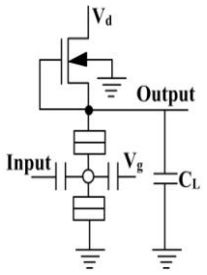
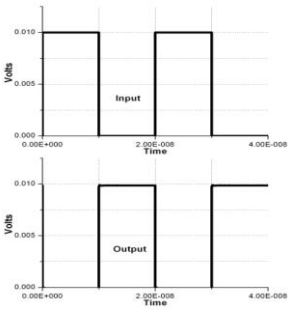



Figure 2. Hybrid CMOS-SET Inverter




.Figure 3. Hybrid CMOS-SET Inverter input output waveform

The same design rule is extended to surface the Hybrid CMOS-SET based two input AND gate and OR gate. Aptly, it is based on the principle of transmission gate as revealed in fig. 5 to 8 respectively. Both these circuits hold three SETs and sequentially three CMOS transistors. The supply voltage $V_d$ is kept sufficiently low, i.e., 0.01 volts only

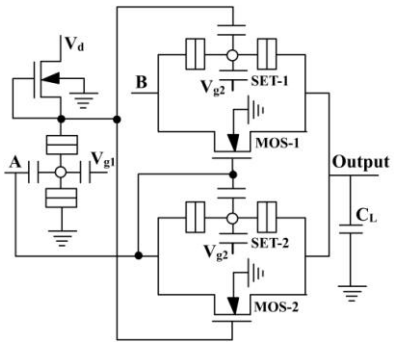



Figure 5, Hybrid CMOS-SET AND gate

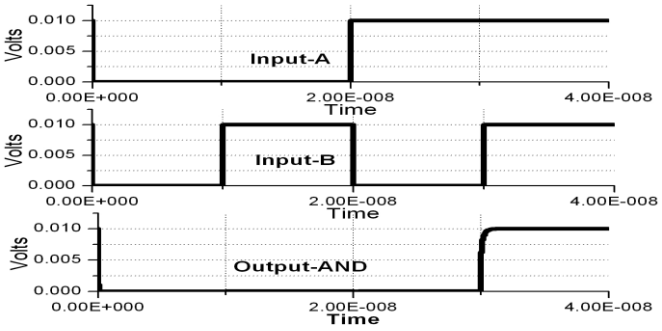



Figure 6. Hybrid CMOS-SET AND gate input output waveform

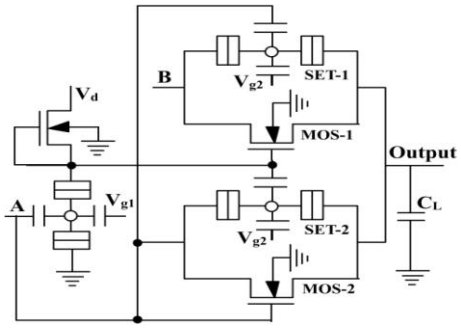



Figure 7. Hybrid CMOS-SET OR gate

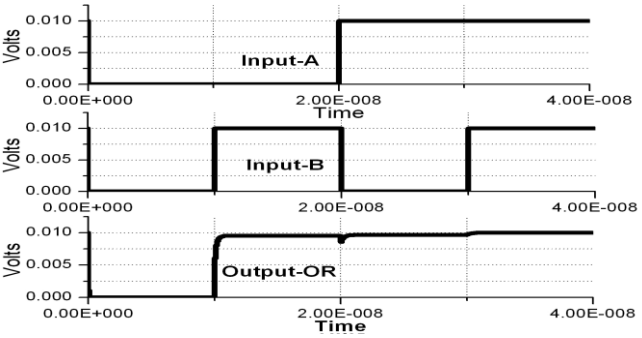



Figure 8. Hybrid CMOS-SET OR gate input output waveform

The AND gate which is driven by controlled switch turns CMOS-1 and SET-1 OFF when A=0 and simultaneously the CMOS-2 and SET-2 becomes ON; thereby replicating the value of A (i.e 0) at the output. Identically, in the next clock pulse when A=1, the CMOS-1 and SET-1 will be turned ON and CMOS-2 and SET-2 will be in OFF state. Apparently in the second case the value of B (either 0 or 1) gives the impression at the output. These chattels mimic the output of a logical AND.

Alike the Hybrid CMOS-SET AND gate, high speed switching occurs for Hybrid CMOS-SET OR gate also. With the first clock pulse i.e., when A=0 CMOS-1 and SET-1 is ON and CMOS-2 and SET-2 turns OFF. As a result, the output is correspondent to the value of B. Likewise in the next clock pulse when A=1 the CMOS-1 and SET-1 will go OFF and CMOS-2 and SET-2 turns ON. At the moment, the value of A = 1 will be achieved at the output. This potentially depicts similar properties of conventional CMOS OR gate



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## III. INCORPORATING HYBRID CMOS-SET LOGIC INTO DECISION MAKING

Here the authors attempted to construct a positive edge triggered decision making logical synthesis using hybrid CMOS-SET logic principle. It is keenly observed that decision making hardware is attracting Researchers worldwide due to its intrinsic capability of automation and robustness. The human thinking is articulated in simple logical ICs. Thus the man machine interface is achieved and that initiates brain mapping. Such tasks is not only fascinating but quite challenging. For simplicity the authors render simple automatic water sprinkling system. The working conditions are kept 'low profile' only to obtain modest output, but it is earnestly stated design complexity is not troublesome.

### *A. Working Conditions of Hybrid CMOS-SET Water Sprinkling System*

Here the season, moisture content of soil, the outside temperature and the Outside humidity is indicated by E, B, D and A respectively. The E remains 1 only for summer; however B, D and A remains 1 indicating a positive high. Integrating these diverse conditions the automatic water sprinkler turns on under any of the following circumstances.

a. The moisture content is low in winter.
b. The temperature is high and the moisture content is low in summer.
c. The temperature is high and the humidity is high in summer.
d. The temperature is low and the moisture content is low in summer.
e. The temperature is high and the humidity is low.

### *B. Logical Synthesis of Hybrid CMOS-SET Water Sprinkling System*

The authors here enumerate all the possible logic combinations involving the variables E, B, D and A for turning ON the automatic water sprinkler system. In other words the given situations to turn ON the sprinkler system are straight forward realizations of a, b, c, d and e; they are emphatically expressed in terms of the defined variables E, B, D, and A as BE, DEB, DAE, DBS, and DA, respectively. The Boolean expression is

$$f = E\bar{B} + E\bar{B}D + EDA + E\bar{B}\bar{T} + D\bar{A} \quad (3)$$

The expressions in terms of minterms and maxterms are obtained as-

$$o/p_1 = (\bar{B} + D)(E + \bar{B} + \bar{A}) \quad (4)$$

$$o/p_2 = \bar{B} + ED + D\bar{A} \quad (5)$$

### *C. Proposed Modeling of Hybrid CMOS-SET Water Sprinkling System*

The authors propose the modeling of automatic water sprinkler in fig. 9 and 10 respectively based on two successive equations 4 and 5. For validation of the circuit the authors sub-sectioned the circuits and then logically probed the intrinsic behaviors of the proposed model.

To cope up with the space limitation and conciseness issue the authors here only demonstrate few graphical electron transportations in fig. 11 and 12 for 'ED' and $(\bar{B} + D)$correspondingly.
The authors lastly phonates the success of working of the proposed model after analyzing each part in the same above stated way with a great liking.

## IV. COMPARATIVE ANALYSIS

These results reveal the calculated power dissipation and the power consumption of designed hybrid logic circuits as presented in table-I. Undoubtedly, they are extreme low compared to any conventional circuits.

TABLE I
POWER DISSIPATION OF SET-MOS HYBRIDCIRCUITS

| GATE | POWER CONSUMPTION | NO. OF MOS | NO. OF SET | POWER |
|---|---|---|---|---|
| AND | 0.01V | 3 | 3 | 1.02E-09 W |
| OR | 0.01V | 3 | 3 | 1.02E-09 W |
| NOT | 0.01V | 1 | 1 | 1.02E-09 W |

## V. CONCLUSION

This letter explored the implementation of Hybrid CMOS-SET nano logic gates in decision making logistics based on single electron MOS transmission. The modeling was articulated using conventional CMOS metaphor and the novel SET allegory. Later they were assimilated based on the Hybrid CMOS-SET Transmission logic. Then after for validation and endorsement of the proper functioning SPICE software was used to simulate the model. Nonetheless, for every clock pulse a step-wise route was monitored. Simulation output renders significant merits and a better trade off in designing such advanced nano ICs.


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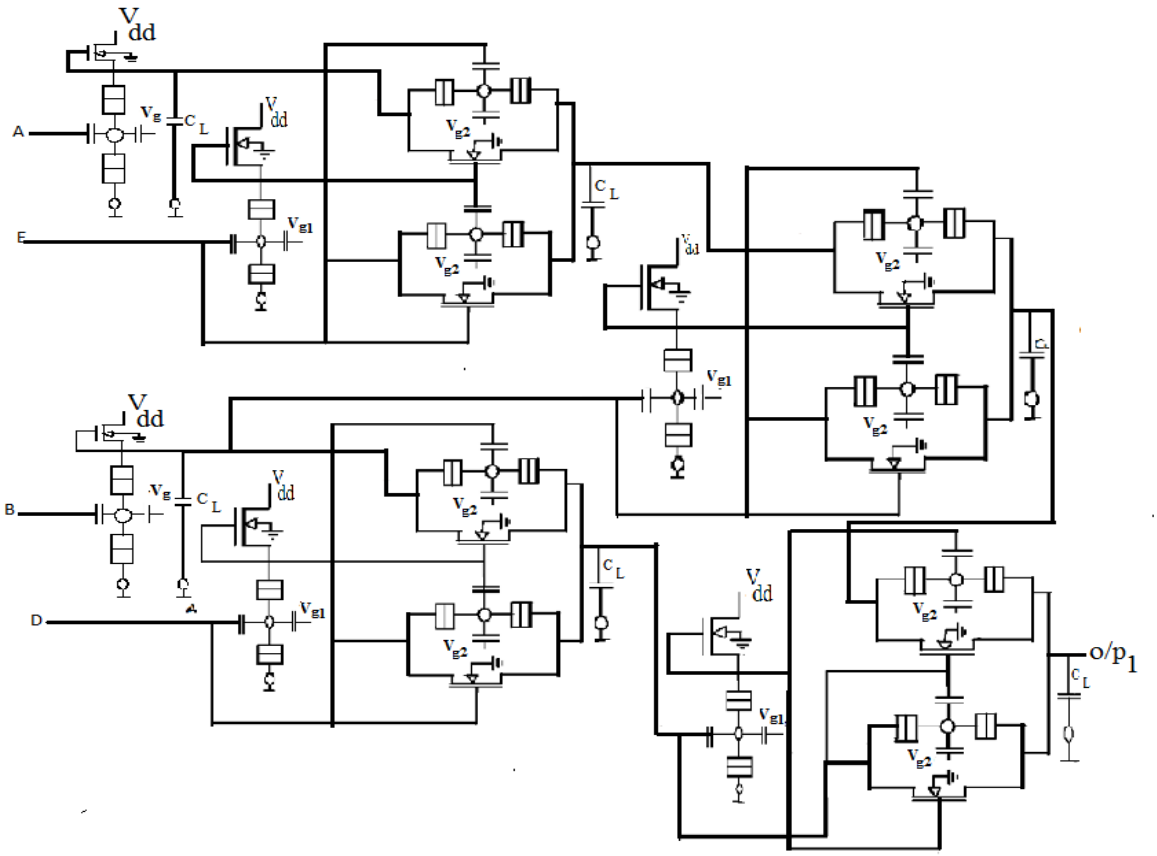


FIG 9: The modeling of hybrid CMOS-SET based automatic water sprinkler for equation (4)

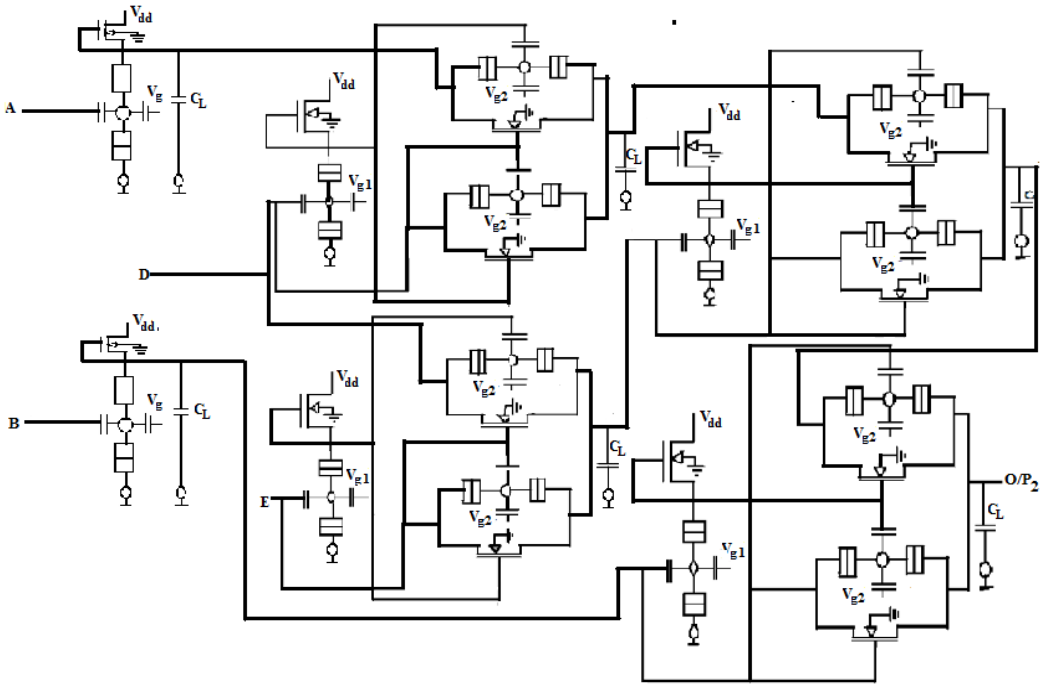


FIG 10:The modeling of hybrid CMOS-SET based automatic water sprinkler for equation (5)



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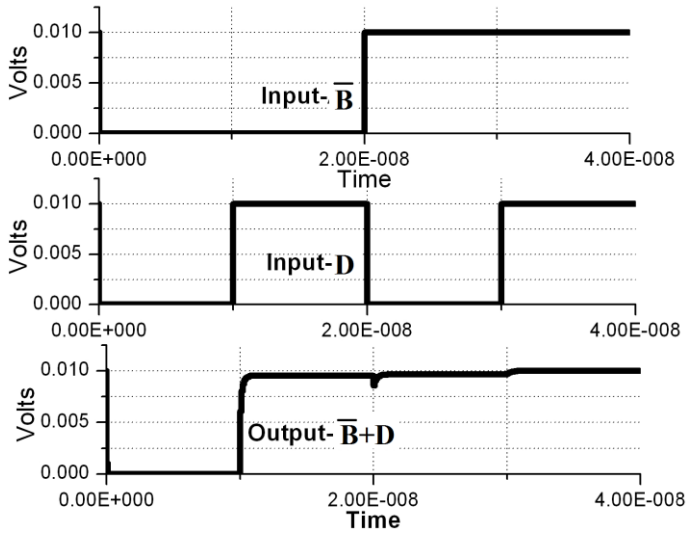


FIG 11: graphical electron transportations

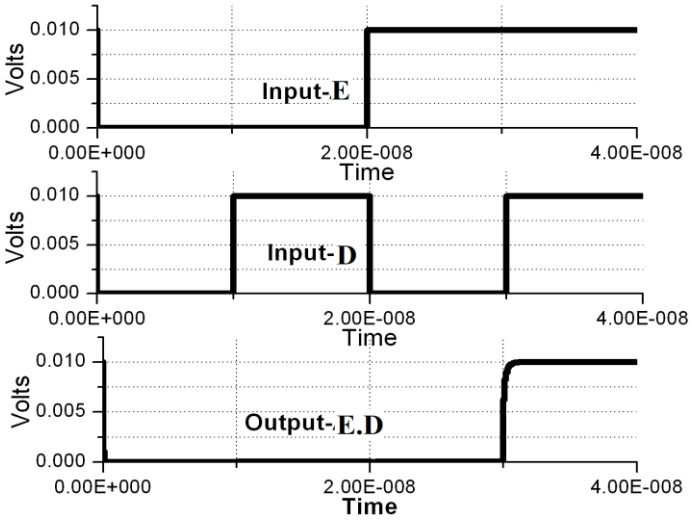


FIG 12: graphical electron transportations



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