

SHM Technique for CHB With Non-equal DC Link Voltages

K.Himaja¹, V. Pratapa Rao², N.Vishnu Vardhan³

¹M.Tech(PE) Student, Department of EEE , Sri sai institute of technology and science
JNTUA University, Anantapuram, AP, India¹

²Assistant professor &HOD, Department of EEE , Sri sai institute of technology and science
JNTUA University, Anantapuram ,AP, India²

³Assistant professor , Department of EEE , Sri sai institute of technology and science
JNTUA University, Anantapuram, AP, India³

Abstract—Multi level converters have received increased interest recently as a result of their ability to generate high quality output waveforms with a low switching frequency. This makes them very attractive for high-power applications. A cascaded H-bridge converter (CHB) is a multilevel topology which is formed from the series connection of H-bridge cells. Optimized pulse width modulation techniques such as selective harmonic elimination or selective harmonic mitigation (SHM-PWM) are capable of preprogramming the harmonic profile of the output waveform over a range of modulation indices. Such modulation methods may, however, not perform optimally if the dc links of the CHB are not balanced. This paper presents a new SHM-PWM control strategy which is capable of meeting grid codes even under non-equal dc link voltages. The method is based on the interpolation of different sets of angles obtained for specific situations of imbalance. Both simulation and experimental results are presented to validate the proposed control method.

Index Terms— Harmonic distortion, multilevel systems, optimization methods, pulse width modulation converters.

1. INTRODUCTION

Multilevel converters have become the focus of research in recent years as a result of their suitability for high - power applications . Amongst the available topologies are the neutral point clamped, flying capacitor, and cascaded H-bridge converters (CHB) . The latter is constructed from a series cascade of three-level H-bridges. This connection enables the converter to produce high quality, high voltage waveforms while utilizing low or medium voltage switching devices. This functionality makes this converter an attractive option for grid connected applications such uninterruptible power supplies, static reactive volt ampere compensators, series and shunt compensators, etc.

The use of power electronic converters at high-power levels usually demands a reduction in switching frequency in order to ensure that losses caused by the imperfect nature of practical switching devices does not significantly reduce the converter efficiency. Selective harmonic

elimination.(SHE-PWM), total harmonic distortion minimization, and selective harmonic mitigation (SHM-PWM) methods are known to produce waveforms with low switching frequency without compromising waveform quality. For these methods, mathematical functions can be derived using the Fourier analysis of a general switched converter waveform which may be solved to meet a certain predefined objective in the wave form. The waveform objectives may include complete elimination (SHE-PWM) or reduction (SHM-PWM) of certain harmonics in the generated waveform or an optimization of this waveform in order for it to meet a particular harmonic code for a certain application.

The derived functions, which are transcendental and nonlinear in nature, can be solved for a range of modulation indices using a variety of method. The solutions can be stored in lookup tables (LUTs) for use with an appropriate converter control scheme.

For CHB-based inverter applications, it may be desirable to ensure that each cell of the converter draws equal energy from the dc source that it is connected to. This can be achieved over a single or several fundamental cycles. This would ensure that these sources discharge at the same rate and that each cell of the cascade is utilized evenly. In applications where the dc sources are not exactly equal, distortion may be present in the converter waveform. This occurs because the switching angles for the modulation may have been derived assuming that the dc sources were equal, and therefore complete harmonic elimination or the required level of harmonic suppression no longer occurs. In , it was found that a large number of different waveform solutions are required in order to manipulate the power flow through a CHB converter while achieving optimal harmonic performance.

This large number of solutions can be avoided by decoupling the cells and independently controlling the modulation index of each cell separately. Unfortunately, this reduction in the number of required LUTs potentially reduces the waveform quality of the CHB converter as the degrees of freedom available in the multilevel converter waveform are not fully utilized.

This paper presents a SHM-PWM technique based on multilevel waveforms which enables the required control of power flow in a CHB converter while fully utilizing the waveform degrees of freedom. The method uses the interpolation of LUT based solutions for a number of imbalances to control the power flow through the H-bridges asymmetrically, thus avoiding the requirement of very large

Manuscript received May, 2015.

K.Himaja,M.Tech(PE), EEE(dept), SSITS,JNTUUniversity
Rayachoty,India, 9666547035,

V.Prathap Rao(HOD),Asst.prof&HOD of EEE dept,
SSITS,JNTUAUniversity,india,9441433911

N.Vishnuvardhan,Asst.prof,SSITS,JNTUA,india-9052465537

LUTs apparent in previous methods. Theoretical and simulated results are experimentally verified using a five level cascaded H-bridge topology operating as an inverter.

II. Cascaded H-Bridge converters

If different dc voltages are used, as is the case in an asymmetric CHB converter, the number of levels can be increased. For example, using two cells, up to nine levels may be achieved in the output waveform. This topology is presented in Fig. 1 where V_A is the dc voltage of the upper cell and V_B represents the voltage of the lower cell. However, this increase in voltage levels is achieved at a cost of reduced converter structure modularity.

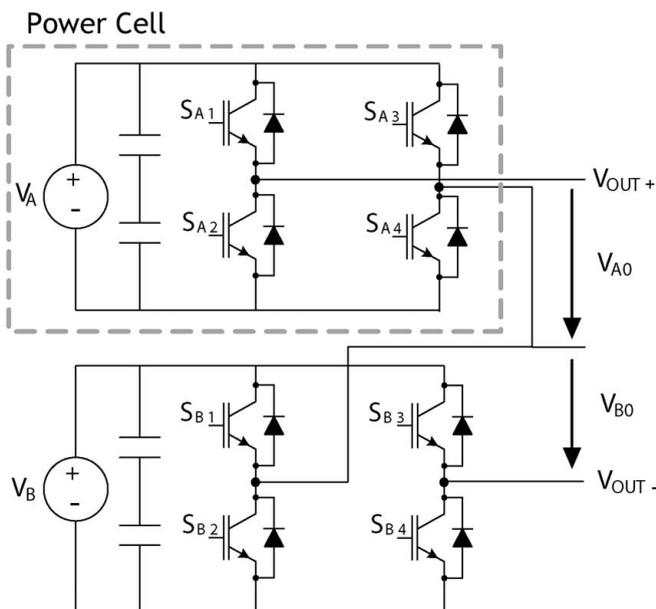


Fig. 1. Five-level cascaded H-bridge converter based on the series connection of two three-level power cells.

Several three-level power cells, formed using full H-bridges, can be series connected to build a converter with a higher number of levels as can be observed from Fig. 1. This can be extended to produce converters with as many levels as required for a particular application. In general, if n power cells are connected in series to build the converter and all the cells have the same dc voltage, the number of levels that can be achieved is $2n + 1$. This topology is named the n -cell CHB converter, and it presents a high level of modularity and redundancy as well as an ability to produce high quality output voltage waveforms

A. Problem of Imbalance

Each cell of a CHB converter must be fed from an isolated dc source to avoid short circuits. Divergences of the dc link voltages from the desired or assumed values will have an effect on the operation of the converter. If the converter is designed to operate with balanced dc link voltages and this is not the case, then the converter is said to be operating under non equal dc link voltages. Such operation may have an undesirable effect on the output voltage waveform of the converter. This is particularly the case when precomputed modulation strategies such as SHEPWM or SHM-PWM are

used as the angles may have been derived under the assumption that the dc link voltages are balanced. The SHE-PWM methods require special considerations when used in multilevel converters with non equal dc link voltages.

In many applications, it is desirable to share the power flow among all the cells equally in order to avoid overheating of some specific switching devices and consequently extend the lifetime of all the elements of the converter. Other, more complicated, CHB-based converter structures may require the power flow to be controlled asymmetrically through the converter cells as was required in. In both cases, assuming that the current is undistorted, the power flow from each cell of the converter can be determined by considering the fundamental frequency component of each cell only. It is possible to manipulate SHE-PWM and SHM-PWM techniques to control the power flow through a CHB converter.

The method considered the use of a low switching frequency SHE-PWM to control power flow through the cells of a CHB converter while still producing high quality waveforms. Unfortunately, a disadvantage of the approach presented in [19] is that a specific set of angles must be calculated for each possible imbalance scenario for the converter, and therefore a very large number of LUTs and a complicated LUT selection scheme would be required to practically implement the method. This paper presents a method which may overcome this disadvantage by attempting to interpolate between LUTs.

III. SHM-PWM PRINCIPLE

A. Three-Level Converters

Fourier analysis can be used to study a typical three level waveform with k switching angles $\alpha_i (i = 0, \dots, k - 1)$ (Fig. 2). The amplitude of each harmonic can be obtained using the following expression where H is the amplitude of the j th harmonic:

$$H_j = \frac{4}{j\pi} \sum_{i=0}^{k-1} [(-1)^i \sin(j\alpha_i)] \rightarrow (1)$$

This expression can be used to set a specific value for each harmonic amplitude using the switching angles as degrees of freedom. The well known SHE-PWM technique is based on this theory, i.e., the switching angles are used to set the amplitude of the fundamental harmonic and cancel a set of Specific harmonics.

The relationship between the dc link voltage of the converter and the amplitude of the generated fundamental component is called the modulation index (M_a) and can be defined as $M_a = H1\pi/4V_{dc}$. As a result of half wave symmetry in the waveform, even harmonics have zero amplitude so the chosen harmonic orders would be 3, 5, 7, . . . and upto $K-1$ harmonics can be canceled using k switching angles.

In balanced three-phase topologies without a neutral connection, the triplen harmonics are also canceled, and so it is possible to eliminate a very high number of the low-order

harmonics with a low switching frequency

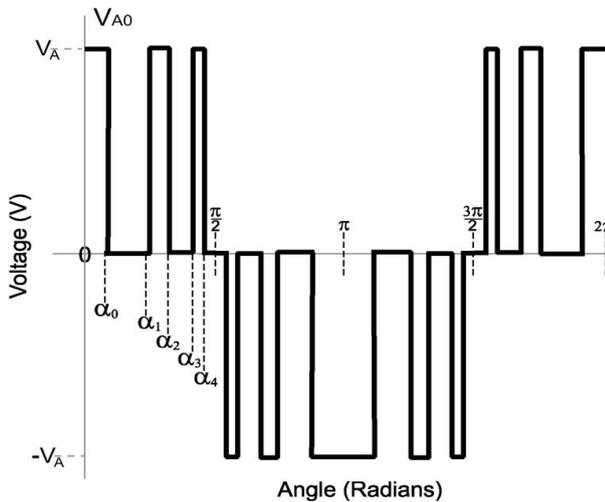


Fig. 2. Three-level preprogrammed PWM switching pattern with five switching angles ($\alpha_0, \alpha_1, \alpha_2, \alpha_3, \alpha_4$). Typical output waveform of the top power cell fig(1)

In balanced three-phase topologies without a neutral connection, the triplen harmonics are also canceled, and so it is possible to eliminate a very high number of the low-order harmonics with a low switching frequency.

Summarizing, the SHE-PWM technique for three-level converters is based on solving the following system of equations where q is the highest harmonic order that will be canceled:

$$H_1 = \frac{4}{\pi} \sum_{i=0}^{k-1} [(-1)^i \sin(\alpha_i - C_{cell-n})] \rightarrow (2)$$

Where $n= 1, 2, \dots, N$

$$0 = \frac{4}{j\pi} \left(V_1 \sin(j\alpha_0) + \sum_{i=1}^{k-1} [V_i [\sin(j\alpha_i) - \sin(j\alpha_{i-1})]] \right)$$

Where $j= 3, 5, 7, 9, 11, \dots, q$. $\rightarrow (3)$

The SHM-PWM technique was presented in and is based on the idea that it is not necessary to completely cancel the harmonics in the converter ac waveform. Instead, they just have to be reduced to levels where they can be considered acceptable.

The maximum harmonic content for a grid-connected inverter can be obtained from the limits specified in the actual grid codes (L_j represents the limit for the j th harmonic). The SHM-PWM technique can be formulated using a system of inequalities (3) which can be arranged into an objective function to be minimized using an optimization method

$$\left| \frac{4M_a V_{dc}}{\pi} - H_1 \right| \leq L_1, \quad \frac{1}{|H_1|} \frac{4}{j\pi} \sum_{i=0}^{k-1} [(-1)^i \sin(j\alpha_i)] \leq L_j$$

Where $j= 3, 5, 7, 9, 11, \dots, 49$. $\rightarrow (4)$

$$OF(\alpha_0, \dots, \alpha_{k-1}) = \sum_{i=1,3,5,\dots,49} c_i E_i^2 + c_{THD} THD \rightarrow (5)$$

The extra flexibility given by the SHM-PWM principle can be used for different objectives, for example reducing the THD, a higher number of harmonics using the same number of switching angles, or extending the modulation index range for the same set of valid solutions.

B. Extension to Converters With a Higher Number of Levels

Considering, for instance, a waveform similar to the pattern shown in Fig. 3 but with N levels and k switching angles. Fig. 3. Nine-level preprogrammed PWM switching pattern with ten switching angles ($\alpha_i, i = 0, \dots, 9$). The waveform is symmetrical in order to eliminate the even harmonics. angles $\alpha_i (i = 0, \dots, k - 1)$ the Fourier analysis gives

$$H_j = \frac{4}{j\pi} \left(V_1 \sin(\alpha_0) + \sum_{i=1}^{k-1} [V_i [\sin(j\alpha_i) - \sin(j\alpha_{i-1})]] \right) \rightarrow (6)$$

$\alpha_i (i = 0, \dots, k - 1)$ the Fourier analysis gives

$$H_j = \frac{4}{j\pi} \left(V_1 \sin(\alpha_0) + \sum_{i=1}^{k-1} [V_i [\sin(j\alpha_i) - \sin(j\alpha_{i-1})]] \right)$$

$$H_j = 0 \quad \text{where } j=3,5,7,9,11,\dots,q). \rightarrow (7)$$

The SHE-PWM can be applied with this kind of waveform.

Again, solving the equations, the fundamental harmonic can be set to the desired value and $k - 1$ harmonics can be reduced to zero ($H_j = 0$ where $j = 3, 5, 7, 9, 11, \dots, q$).

In order to guarantee that all the cells are sharing the same power this system of equations needs to be modified. Instead of using the fundamental harmonic of the global waveform, the fundamental component generated by each cell is forced to be equal to the desired value. This way, for a N -cell converter working with k switching angles per cell only $N(k - 1)$ extra harmonics can be canceled. The new system of equations can be formed with (6) and (7) considering that in (7) it is assumed that the angles of all the cells are rearranged to generate the suitable multilevel global waveform

$$S1 = (0, 0, 0), \quad S2 = \left(-\frac{2X}{3}, \frac{X}{3}, \frac{X}{3} \right) \rightarrow (8)$$

$$S3 = \left(-\frac{X}{3}, -\frac{X}{3}, \frac{2X}{3} \right) \rightarrow (9)$$

$$AV_1 + B \frac{V_1}{(1 + \frac{2X}{3})} + C \frac{V_1}{(1 + \frac{X}{3})} = 1 \rightarrow (10)$$

$$AV_2 + B \frac{V_2}{(1 - \frac{X}{3})} + C \frac{V_2}{(1 + \frac{X}{3})} = 1 \rightarrow (11)$$

$$AV_3 + B \frac{V_3}{(1 - \frac{X}{3})} + C \frac{V_3}{(1 - \frac{2X}{3})} = 1. \rightarrow (12)$$

The SHM-PWM technique can also be applied to converters with more than three levels. Using the SHM-PWM principle, based on reducing the harmonic amplitudes to a reduced but nonzero value, the system of equations changes to the system of inequalities detailed in (8) and (9). Again, in (9), it is assumed that the angles of all the cells are used to generate a global waveform as in Fig. 3. The whole system of equations can be grouped in the same objective function (4) shown in

As in previous work, in this paper, the well known Simulated Annealing optimization method has been chosen because it can be adapted very easily to problems with many different constraints. In any case, it has to be noted that since the solutions are calculated only once and then are stored in LUTs for use with the power converter, the optimization method itself.

IV. SHM-PWM FOR BALANCING

Under unbalanced conditions, it is necessary to use a strategy to adjust the modulation index in order to share the power among all the cells. In [1], a method was presented based on the SHE-PWM technique that could tolerate any imbalance situation by decoupling all of the cells of the converter. Considering a multi cell cascaded converter, specific LUTs can be previously obtained for different unbalancing conditions. When the dc voltages of each cell are normalized, the imbalance of each cell can be referred as an increment or decrement with respect to the theoretical mean value. In the rest of the paper, the following nomenclature will be used to define the conditions of each LUT: (X_1, X_2, \dots, X_n) where X_n represents the imbalance of cell n , in percent, of the average desired voltage (perfect balanced situation). For example, considering a two-cell converter with a maximum tolerable imbalance of 3%, two LUTs, $S1(0, 0)$ and $S2(-3, 3)$ are required. Interpolation between the elements of these two LUTs can be used in order to find the required switching angles which achieve the required waveform objectives over this 0–3% imbalance range.

For higher imbalance conditions, extra LUTs could be added to extend the range. For instance, the range could be extended to tolerate an imbalance of up to 6% using $S3(-6, 6)$, or 9% using $S4(-9, 9)$, etc. The linear interpolation between the switching angles stored in the two LUTs can be achieved using the following equation on each element of the two LUTs:

$$\alpha_{(i)} = A\alpha_{LUT1(i)} + B\alpha_{LUT2(i)} \quad (13)$$

This interpolation method is advantageous when compared to other methods considered in literature as it limits the number of required LUTs that are needed to achieve the waveform objectives in the presence of a dc imbalance. For example, using the LUTs described above, for an imbalance of 1%, the constants would be $A = 1/3$ and $B = 2/3$.

A. Extension to Three-Cell Cascaded Converters:

For a three-cell converter, the imbalance may be shared among all of the cells in the converter. For this case, three

LUTs are required as shown in (11), where X represents the percentage imbalance (referred to the average voltage), as previously noted. The principle of the proposed method is based on exploiting the flexibility given by the SHM-PWM method to obtain a new set of solutions under different dc-link imbalance conditions but from a previous set of solutions in such a way that the switching angles are very similar. This leads with a very small variation from one table to the other allowing the use of linear interpolation between both tables to obtain all the unbalancing conditions not directly stored in the LUTs. These can be tolerated in this case as excessive values of X will inhibit the ability to linearly interpolate between LUTs (compared to low values of X). Now, the final set of angles would be obtained from the three tables. The interpolation constants can be obtained by solving the linear system of equations obtained by forcing the same amplitude in the fundamental harmonics generated by all the cells (this amplitude has been normalized to 1 for simplicity). The principle of the proposed method is based on exploiting the flexibility given by the SHM-PWM method to obtain a new set of solutions under different dc-link imbalance conditions but from a previous set of solutions in such a way that the switching angles are very similar. This leads with a very small variation from one table to the other allowing the use of linear interpolation between both tables to obtain all the unbalancing conditions not directly stored in the LUTs.

The principle of the proposed method is based on exploiting the flexibility given by the SHM-PWM method to obtain a new set of solutions under different dc-link imbalance conditions but from a previous set of solutions in such a way that the switching angles are very similar. This leads with a very small variation from one table to the other allowing the use of linear interpolation between both tables to obtain all the unbalancing conditions not directly stored in the LUTs.

The angles obtained from such similar sets of solutions should share the same characteristics in terms of power flow control and output spectrum. We are assuming that the amplitude of each harmonic component corresponds to the linear interpolating of the corresponding amplitudes of each set of solutions (based on the linear property of the discrete Fourier transform). It should be noted that the linear system of equations can be solved offline and the solution computed by a DSP on demand.

The next sections show some examples for both two and three-cell CHB converters. The angles obtained from such similar sets of solutions should share the same characteristics in terms of power flow control and output spectrum.

V. SIMULATION RESULTS

This section presents the simulation results that have been obtained using the SHM-PWM technique in a two and a three cell CHB converter. In order to obtain solutions which could be easily implemented in a real converter, real power semiconductors have been considered.

A minimum margin of 0.01 radians between two consecutive switching angles has been taken into account as a valid safe margin. In the computing process the limits specified in the EN 50160 and CIGRE WG 36-05 grid codes have been considered but any other could have been chosen.

These standards include specific limits for each harmonic up to 49th harmonic the waveform THD calculated up to 40th harmonic.

The methods presented have been experimentally support retarding a single phase, five-level cascaded H-bridge converter and three switching angles per cell. This converter is configured as an inverter feeding an RL load ($R= 360 \Omega$ and $L=15mH$).The H-bridges are constructed using Semi kron SK60GB128modules. The dc link for each H-bridge is fed from a separate dc value of200 V. The total imbalance range from 0% to 10% in steps of1% has been studied for the particular case of $Ma=0.70$.

A.SIMULINK MODEL

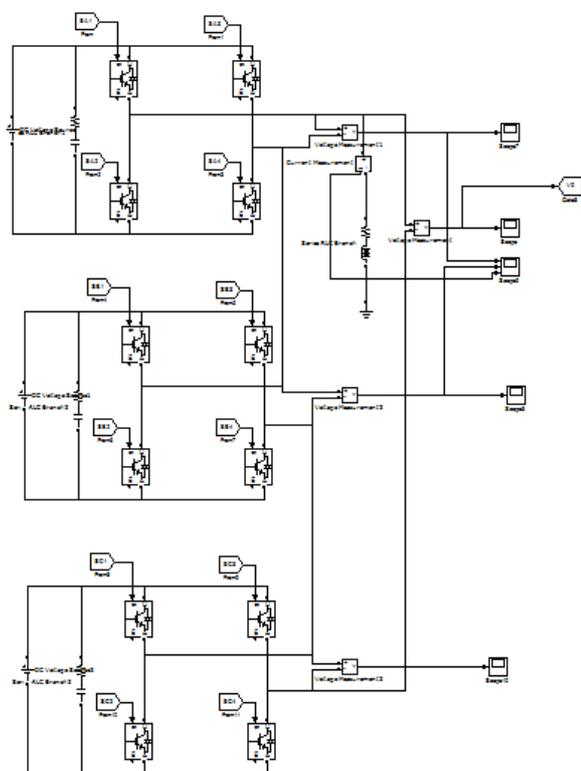
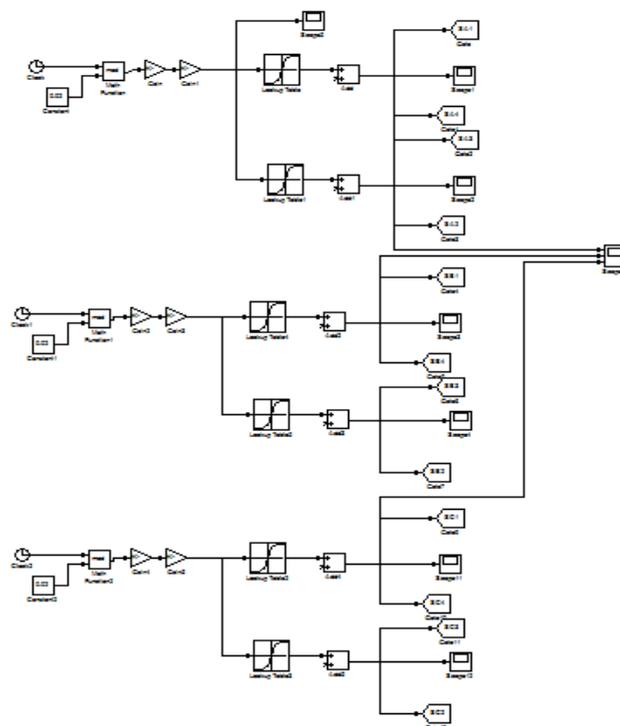


Fig3(a):Circuit diagram

to the limited availability of loads in the laboratory the currents have an important harmonic content similar to the voltage waveforms .Using a more practical load the harmonic content would be reduced .Table II shows a comparison between the theoretical values and the experimental results of the real balance obtained in the converter and the distortion levels of the global output under different imbalance conditions. From left to right, the table shows the forced dc-link imbalance, the amplitude of the fundamental harmonic of the global waveform, the different distortion levels of the global output and the finalH1imbalancebetween both cells obtained using the method for both the theoretical and the experimental results. The effects of using real switching.



(b) simulink model

A. Description of the Converter

The methods presented have been experimentally supported using a single phase, five-level cascaded H-bridge converter and three switching angles per cell. This converter is configured as an inverter feeding an RL load ($R= 360 \Omega$ and $L=15mH$).The H-bridges are constructed using Semikron SK60GB128modules.

B. Results

All the experimental data have been captured using a digital oscilloscope and post processed using Mat lab. Fig. 10 shows the voltages of both cells and the output current of the converter for a balanced situation. Fig. 11 shows the global output voltage and the current for an imbalance of 10%. Due

devices and drivers generate the small differences shown in the table. It can be observed that in all the cases ,the real balance achieved by the method is always below 1% which is a very good result considering the very low switching frequency that is being used. It must be also noted that the corresponding limits of the grid code for all the considered harmonics (up to 9th) are always met in the global output of t he converter. Fig. 4 shows the experimental results presented in the table and the grid code limits. The following shows the comparison between distortion and dc link imbalance voltages. As the order increases then the distortion decreases. The following shows the experimental results obtained using SHM-PWM for $Ma=0.7$ and 2 cells.

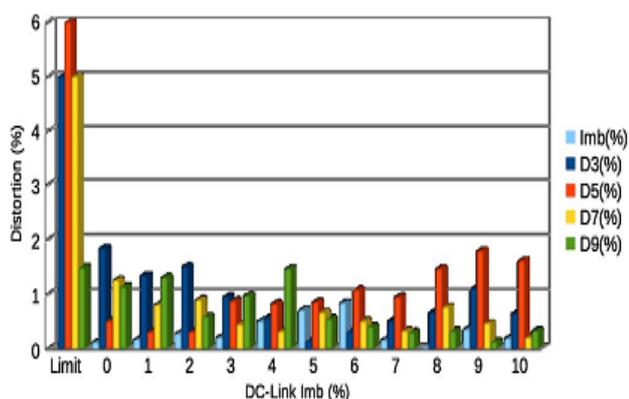


Fig 4.Experimental results presented and grid limits.

frequency. An example of an applications which may benefit from such a scheme is in a multilevel UPS. In this case, the technique could be able to meet grid voltage standards even when the batteries are charged to different voltages. Different simulation results for two and three-cell converters have been included to show the viability of the technique.

Experimental results supporting the method in a two-cell converter validating the technique for an imbalance range from 0% to 10% have been included fig(5). The following shows the output of Voltage of both cells and current(bottom) for an imbalance of 0% in fig(6) and Global output waveform and current(bottom) for an imbalance of 10%.

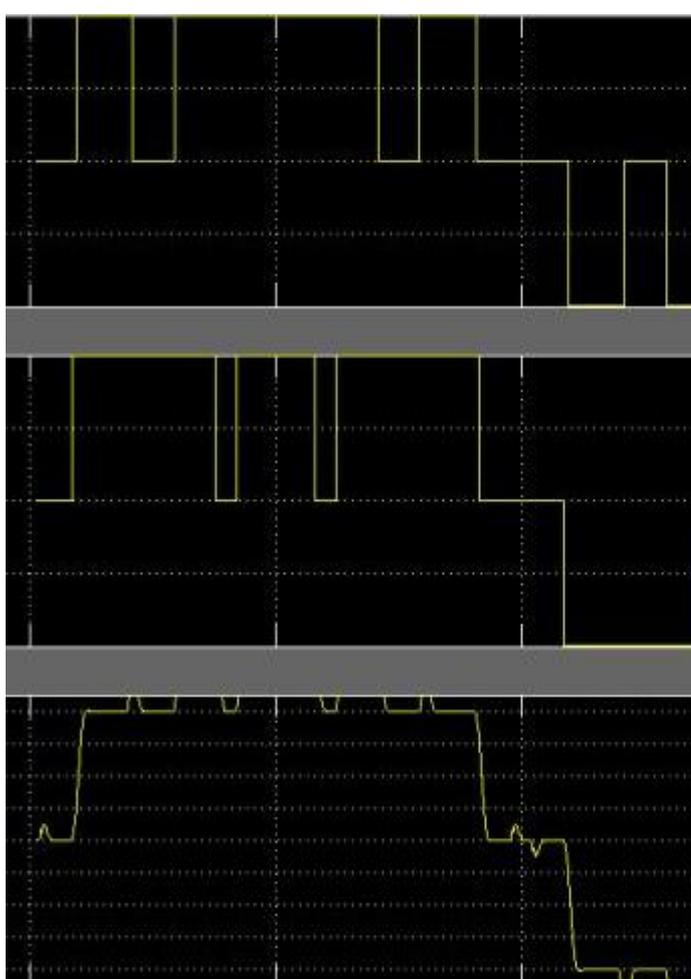


Fig (5). Voltage of both cells and current(bottom) for an imbalance of 0%. The scales are 200 V/div, 0.5 A/div, and 5 ms/div.

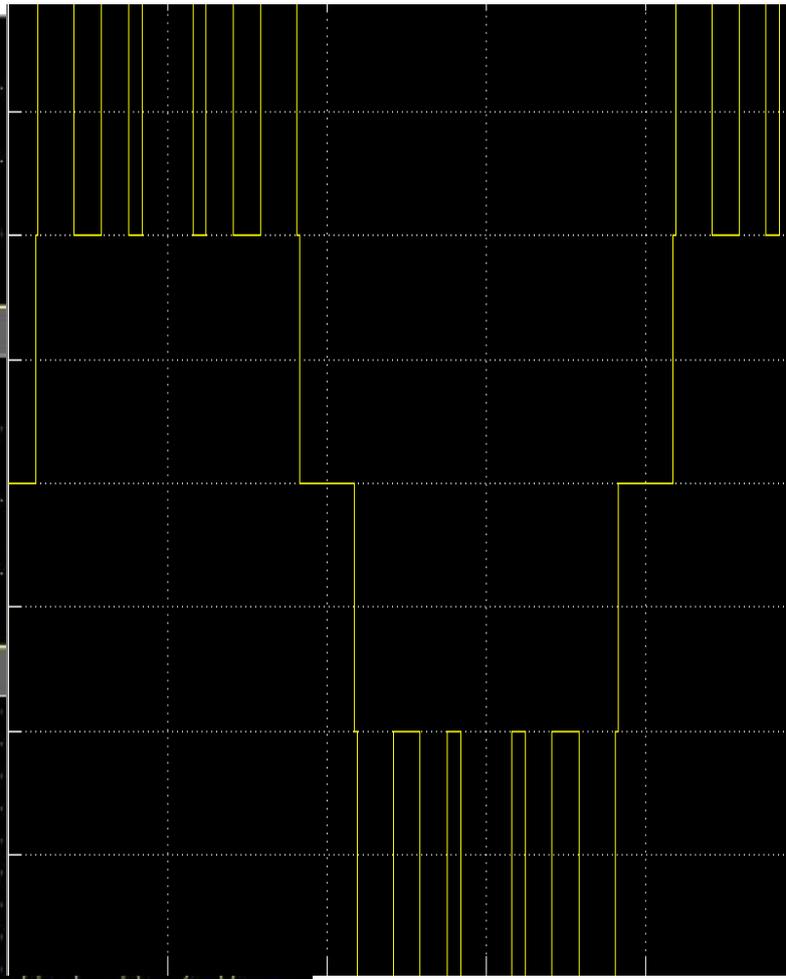


Fig. (6): Global output waveform and current(bottom) for an imbalance of 10%. The scales are 100 V/div, 0.25 A/div, and 5 ms/div.

VI.CONCLUSION

This paper presents a new control strategy, based on the SHM-PWM technique that can tolerate different capacitor voltage levels for cascaded H-bridge multilevel converters. In comparison with other techniques, in this case, it is possible to control the amplitude of each cell under balanced or unbalanced conditions with a reduced number of LUTs while still producing very high quality waveforms at low switching

REFERENCES

[1] H. S. Patel and R. G. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part II voltage control techniques," *IEEE Trans. Ind. Appl.*, vol. IA-10, no. 5, pp. 666–673, Sep. 1974.
 [2] L. G. Franquelo, J. Napoles, R. C. P. Guisado, J. I. Leon, and M. A. Aguirre, "A flexible selective harmonic mitigation technique to meet grid codes in three-level PWM

converters," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3022–3029, Dec. 2007.

[3] A. Mehrizi-Sani and S. Filizadeh, "An optimized space vector modulation sequence for improved harmonic performance," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 2894–2903, Aug. 2009.

[4] N. He, D. Xu, and L. Huang, "The application of particle swarm optimization to passive and hybrid active power filter design," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 2841–2851, Aug. 2009.

[5] L. M. Tolbert, J. N. Chiasson, Z. Du, and K. J. McKenzie, "Elimination of harmonics in a multilevel converter with nonequal DC sources," *IEEE Trans. Ind. Appl.*, vol. 41, no. 1, pp. 75–82, Jan./Feb. 2005.

[6] H. Taghizadeh and M. T. Hagh, "Harmonic elimination of multilevel inverters using particle swarm optimization," in *Proc. ISIE*, Cambridge, U.K., Jun./Jul. 2008, pp. 393–396.

[7] M. S. A. Dahidah and V. G. Agelidis, "Selective harmonic elimination PWM control for cascaded multilevel voltage source converters: A generalized formula," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1620–1630, Jul. 2008.

[8] A. J. Watson, P. W. Wheeler, and J. C. Clare, "A complete harmonic elimination approach to DC link voltage balancing for a cascaded multilevel rectifier," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2946–2953, Dec. 2007.

[9] C. Rech and J. R. Pinheiro, "Hybrid multilevel converters: Unified analysis and design considerations," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 1092–1104, Apr. 2007.

[10] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[11] D. Ahmadi and J. Wang, "Selective harmonic elimination for multilevel inverters with unbalanced DC inputs," in *Proc. IEEE VPPC*, Sep. 2009, pp. 773–778.

FIRST AUTHOR DETAILS:

K. HIMAJA currently pursuing *M.Tech in POWER ELECTRONICS* from *SRI SAI INSTITUTE OF TECHNOLOGY AND SCIENCE* affiliated *JNTUA*. she has done her *B.Tech degree* from *SRI SAI INSTITUTE OF TECHNOLOGY AND SCIENCE* affiliated *JNTUA* in 2013 and her field of interest includes *POWER ELECTRONICS*.

SECOND AUTHOR DETAILS:

V. PRATAPA RAO has completed his *B.Tech ELECTRICAL&ELECTRONICS ENGINEERING* in 2003 from *R.G.M college of engineering and technology* affiliated *JNTUH*. *M.Tech in power system* from *AITs Rajampet*, affiliated *JNTUA*, and presently he is interested to reach topics includes *power system especially in Electrical Distribution System*, working as *HOD of EEE department of SRI SAI INSTITUTE OF TECHNOLOGY AND SCIENCE* affiliated *JNTUA*. *Rayachoty, kadapa(dist).Andhra Pradesh,INDIA*.

THIRD AUTHOR DETAILS:

N.VISHNU VARDHAN, has completed his *B.Tech ELECTRICAL&ELECTRONICS ENGINEERING & M.Tech*

in power electronics from *VITS,NELLORE*, affiliated *JNTUA*, and presently he is interested to reach topics includes *power electronics,working as ASSISTANT PROFESSOR in EEE department of SRI SAI INSTITUTE OF TECHNOLOGY AND SCIENCE* affiliated *JNTUA*. *Rayachoty, kadapa(dist).Andhra Pradesh,INDIA*.