A Reversible Logic based Power Efficient N*1 Multiplexer Design using SRM Gate

Sathish K, Aswinkumar R, Theresal T, Bala Murugan T

***Abstract*— Reversible Logic plays a vital role in the field of Nanotechnology and quantum computing because of its Low power Consumption. Conventional circuits are irreversible. The Authors had proposed a new reversible gate named SRM which acts as a Multiplexer. It is compared to the existing circuits and proven to be optically good in Nature. Optisystem Software is used to Simulate the circuit and to verify the Output.**

***Index Terms*— Reversible Multiplexer, Reversible Logic, SRM Gate.**

I. INTRODUCTION

The advancement of reversible logic technologies had improved the performance of computer architectures. Conventional Logic is Irreversible. Reversible logic For Example XOR Gate is Irreversible as it possess unequal amount of Inputs and outputs. Researchers like Landauer have shown that for irreversible logic computations, each bit of information lost generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1]. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation.

II. BASIC DEFINITIONS

A. Reversible function

A function is said reversible if , given its output, it is always possible to determine back its input, which is the case when there is a one-to-one relationship between input and output states[3].

B. Reversible Logic gate

The logic gate which satisfies the reversible function is termed as reversible logic gates. Here always the number of inputs goes equal to the number of outputs. [4] It not only determines input from the output but also vice versa.

C. Ancilla Input

The unwanted or unused input in the gate or the circuit is known as Ancilla Input.

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D. Garbage output

The unwanted outputs in gate or circuit. Basically it is made used to attain the state of reversibility.

III. .MACH ZEHENDER INTERFEROMETER(MZI)

Mach Zehender interferometer is the basic structural and the functional unit of the Reversible logic gates in the optical domain. It is a simple device for demonstrating interference by division of the amplitude.

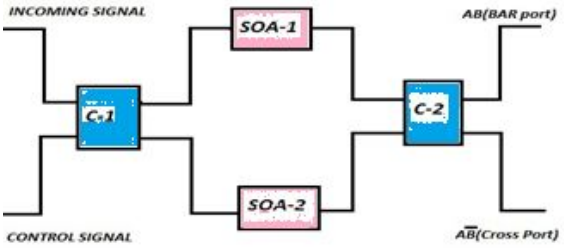

Figure 1Mach-Zehender Interferometer

It consist of a passive device called coupler which splits and also combines the beam. It also consists of Semiconductor Optical Amplifier. It consist of two port one is dot port and other is cross port. In MZI there are two inputs ports A and B and two output ports called as bar port and cross port respectively, as shown in Fig.1.

The working of the MZI [5] can be explained as:
(i) when there is an incoming signal at port A and the control signal at port B then there is a light present at the output bar port and there is no light present at the output cross port.
(ii) in the absence of control signal at input port B and incoming signal at input port A then the outputs of MZI are switched and results in the presence of light at the output cross port and no light at the bar port.

In this work, consider no light or absence of light is considered as the value 0. The above behavior of MZI based all optical switch can be written as Boolean functions having inputs to outputs mapping as (A, B) to (P=AB, Q = Abar B), where A (incoming signal), B (control signal) are the inputs of MZI and P (Bar Port), Q (Cross Port) are the outputs of MZI, respectively. The optical cost of the gate or the reversible circuit is determined by the number of parallel MZI. Setting delay for Mach Zehnder Interferometer is quite difficult job. The Mach-Zehnder interferometer based implementation of reversible logic gates provides significant advantages such as high speed, low power, fast switching time, and ease in the fabrication.

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IV. PROPOSED WORK

A. The Proposed SRM GATE

The inputs and the outputs of the proposed 3*3 reversible SRM Gate are A,B,C and P,Q,R respectively.
The simple block diagram of the proposed SRM Gate is shown in the figure 2.

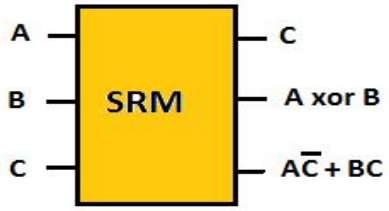

Figure 2 Block Diagram of the Proposed SRM Gate

B Truth Table of the Proposed SRM Gate

The truth table of the Proposed SRM Gate is given in the table 1.

INPUTS			OUTPUTS		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	1	0
0	1	1	1	1	1
1	0	0	0	1	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	0	1

Table 1 Truth Table of the Proposed SRM Gate

C. Optical Implementation

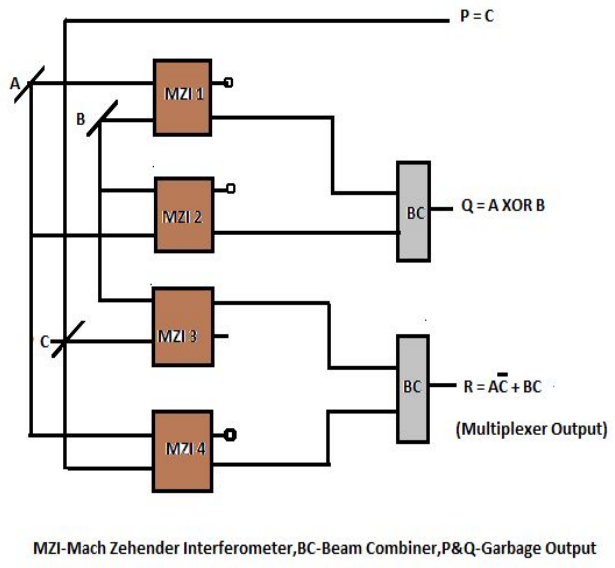

Figure 3 Optical Implementation of the Proposed SRM Gate

The Optical implementation of the proposed SRM gate preferred for the 2*1 Multiplexer is given in the figure 3.The Optical Implementation requires the Beam Splitter, Beam Combiner and the Mach Zehender Interferomter. The designed circuit can be implemented or simulated using the Optisystem Software.

V. N*1 MULTIPLEXER USING SRM GATE

The N*1 Multiplexer can be designed using the proposed Reversible SRM Gate. The proposed Reversible Logic SRM Gate itself represents as the 2*1 Multiplexer.

*A.4*1 Multiplexer using 2*1 Multiplexer*

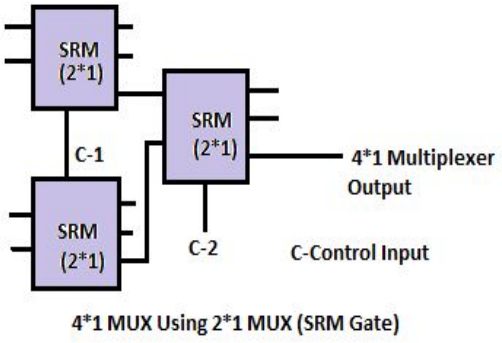

*Figure 4 Block Diagram of the 4*1 MUX Proposed SRM Gate*

Three SRM Gates are required to make the 4*1 Multiplexer. 3 SRM Gates are required to make the 4*1 Multiplexer. It consists of 4 ancilla inputs and 5 garbage outputs. Figure 5 represents the Reversible 4*1 Multiplexer using the 2*1 Multiplexer.

*B. 16*1 Multiplexer using 4*1 Multiplexer*

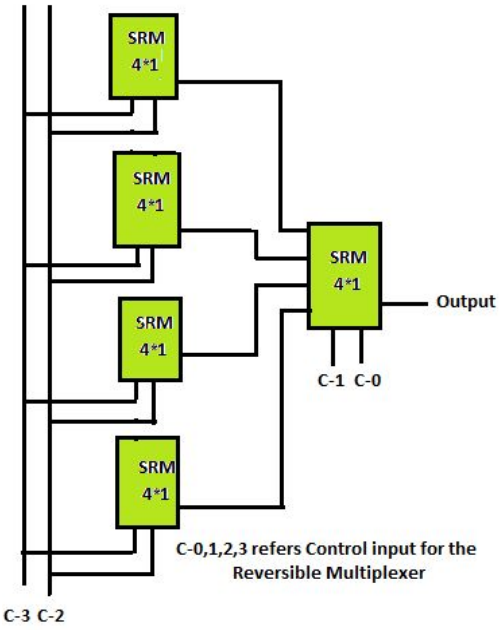

*Figure 5 Block Diagram of the 16*1 MUX Proposed SRM Gate*

15 SRM Gates are required to make the 16*1 Multiplexer. It consists of 20 ancilla inputs and 10 garbage outputs. Figure 5 represents the Reversible 16*1 Multiplexer using the 4*1 Multiplexer.

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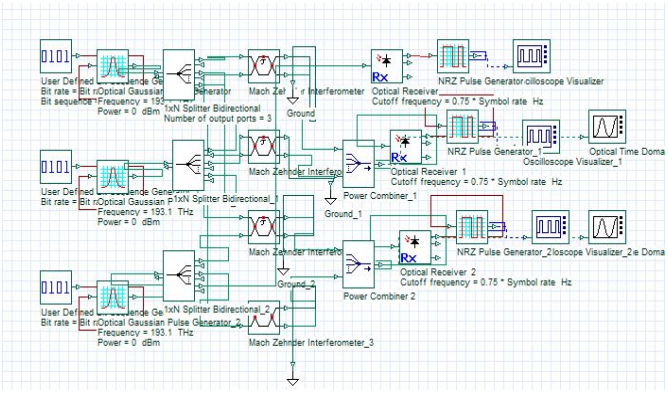
Similarly we can design any no. of Input to Single Output Multiplexer using the proposed SRM gate

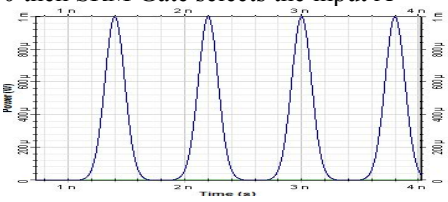
VI. CIRCUIT SIMULATION

The circuit is simulated using Optisystem Sofware

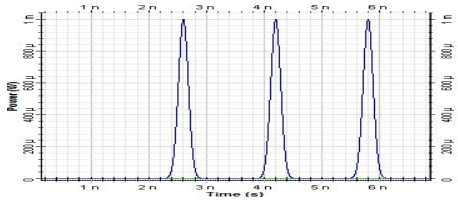


If the inputs are A=01010101 and B=00101010 then for the two cases of the control.

Case 1: If C=0 then SRM Gate selects the input A



Case 2: If C=1 then SRM Gate selects the input B



VII. COMPARISON

The proposed Reversible SRM Multiplexer is more efficient than the existing Multiplexers. The following Comparative Chart clearly proves SRM Multiplexers Efficiency.

A. Comparative Chart with respect to Existing Multiplexer [6]

Comparing the SRM Multiplexer With the Existing One in terms of its Ancilla Inputs, Garbage Outputs, Optical Cost and the Gate Count.

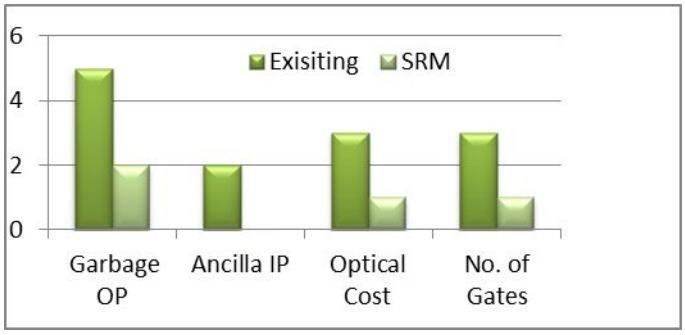


Chart 1 Comparison based on Entity

B. Comparative Chart with respect to Existing Multiplexer [7]

Comparing with Optical Implementation SRM Multiplexer With the Existing One in terms of its No. of Power splitters, Power Combiners ,Inputs, Outputs etc .

Chart 2 Comparison based on Optical Implementation

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VIII. CONCLUSION

In this paper, the Reversible SRM Gate is proposed for the improvised and the efficient performance of the Multiplexer. One of the major constrains in the reversible Logic to reduce the number of the gates. This is achieved for the Multiplexer through the proposed SRM Gate.

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